How to Optimize a Power Over Ethernet (PoE) PD Design

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What is Power over Ethernet (PoE)?

Power over Ethernet (PoE) solutions enable Ethernet cables to transmit DC power while simultaneously transmitting data in parallel to IP terminal devices — all without changing the existing wire connections set by the Ethernet standard. Transmitting power and data in one cable simplifies installation, enhances reliability, and reduces cost by eliminating the need for a power and Ethernet line, which makes PoE devices a popular choice for equipment rooms and offices, as well as older buildings where it may be inconvenient to install new power lines.

This article will provide an overview of PoE PD design, discuss challenges faced by designers implementing these systems, and describe how to optimize a PoE PD design using the MP8017 — an integrated PoE PD and flyback power converter — to verify the recommendations.

PoE Evolution

In 1999, the IEEE and Ethernet Alliance endeavored to standardize PoE, with the goal of ensuring interoperability across a broader range of connected powered devices (PDs) and power sourcing equipment (PSE). The first of these standards, IEEE 802.3af, was ratified in 2003. This standard specified that the power must be able to be carried by either spare pairs or data pairs within a single cable. Today's PoE standard is the IEEE802.3bt (90W), which covers additional applications such as 5G small cells, display units, and AP routers. Figure 1 shows a timeline of the IEEE PoE standards, beginning with the ≤10W standard in 1999.
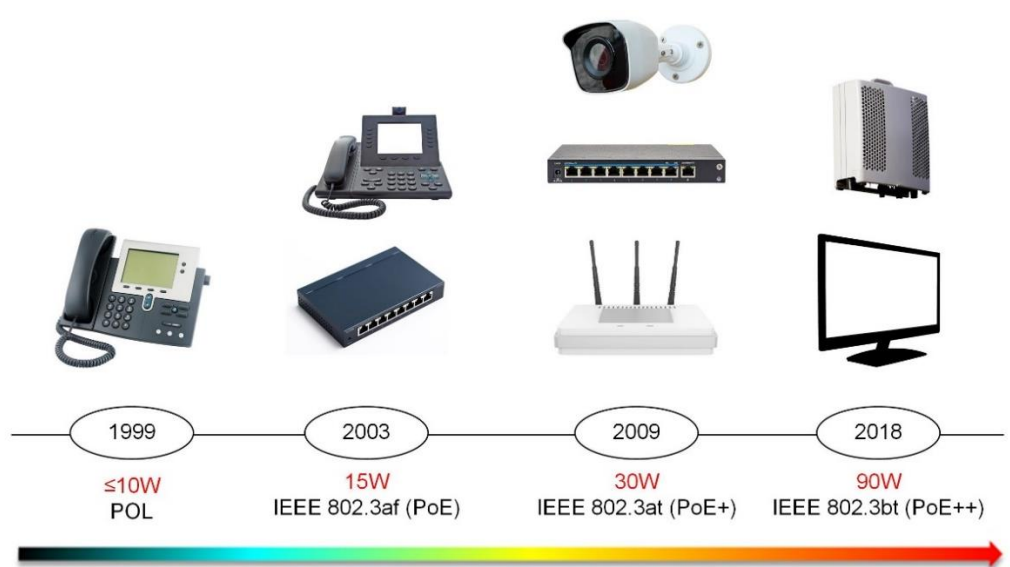

1999	2003	2009	2018
≤10W POL	15W IEEE 802.3af (PoE)	30W IEEE 802.3at (PoE+)	90W IEEE 802.3bt (PoE++)

Figure 1: PoE Standard Evolution History

PoE Power Classification

PoE devices are assigned a class (Class 0 through 8, for a total of nine classes) based on the power they require. The 802.3af standard covered Class 0 to Class 3, with voltages ranging between 37V and 57V, and output power up to 15.4. These devices are recommended for sensors and simple cameras.

The 802.3at standard (also known as PoE+) introduced Class 4, which raises the output power to 30W across the same voltage range, though these devices are only compatible with PoE+ PSE. These devices can be used in complex cameras, LCD displays, and tablets.

Lastly, the 802.3bt standard (also called PoE++) introduced Class 5 through Class 8, with output power between 45W and 90W. These devices can support laptops, TVs, and electrical systems in buildings. Figure 2 summarizes these power classes and their related input voltages, input powers, and output voltages.

Standard	802.3 af				802.3 at	802.3 bt			
Class	Class 0	Class 1	Class 2	Class 3	Class 4	Class 5	Class 6	Class 7	Class8
Type	1	1	1	1	2	3	3	4	4
PSE Output power	15.4W	4W	7W	15.4W	30W	45W	60W	75W	90W
PSE Output Voltage	44V – 57V				50V – 57V	50V/52V – 57V			
PD Input Power	13W	3.84W	6.49W	13W	25.5W	40W	51W	62W	71.3W
PD Input Voltage	37V – 57V				42.5V – 57V	41V – 57V			

Figure 2: PoE Power Classification

PoE Working Principles

Network cables consist of wires twisted in pairs, with data pairs that are able to send information, and unused pairs that are called spare pairs. When a PD and PSE successfully communicate, it is called a handshake. When the PSE shakes hands with a PD, it follows the main steps listed below:

1. PD check: The PSE sends a test voltage (<10.1V) to the PD resistor (24.9kΩ). If the impedance values match, this indicates the presence of a standard PoE device.

2. Power classification): The PSE sends one voltage and obtains current feedback to confirm the PD's power level (from Class 1 to Class 8).

3. Supply power: The PSE's input power rises to about 54V.

4. Stabilize power and monitor): The power stabilizes at about 54V, and the maximum power is limited based on the classification results.

5. Disconnect: If the PD is disconnected, the PSE stops supplying power.

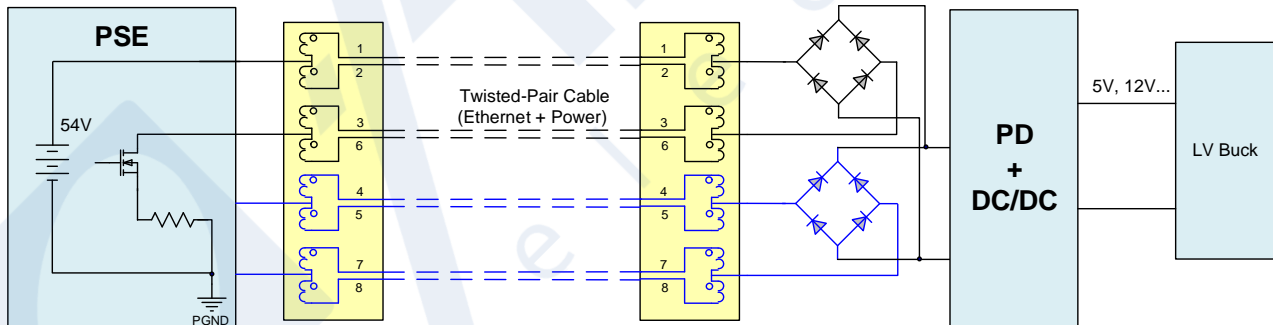Figure 3 shows the overall communication structure.

Figure 3: PSE and PD Communication Hardware Structure

Figure 4 shows how voltage levels change while hand shaking occurs between the PSE and PD.
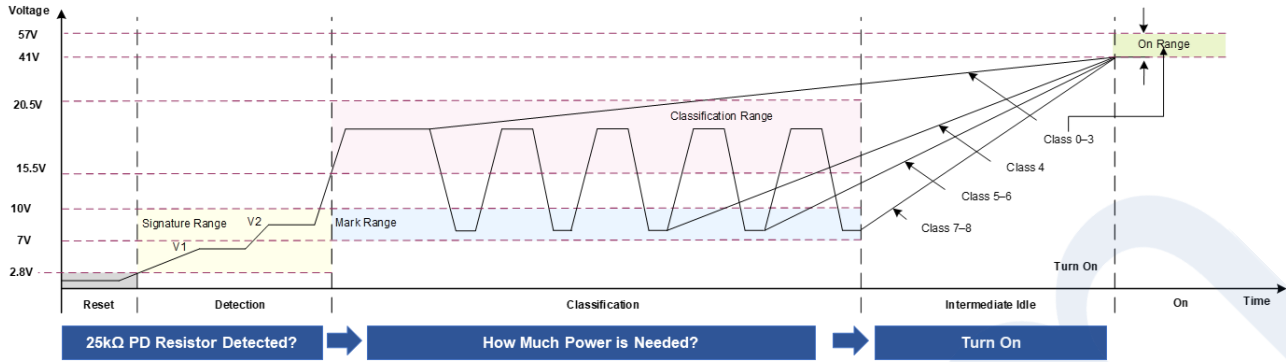
Figure 4: Input Voltage Changes during Handshaking

Challenges when Designing PoE Solutions

PoE devices face a few challenges, the first being efficiency. Although PoE devices incorporate both power and data transfer, they can have lower efficiency if they are not designed correctly. In particular, designers must optimize the power circuit to reduce components' impedances and select an optimal transformer to improve efficiency.

In addition, the high amount of power transfer creates audible noise, which can affect a device's ability to meet modern EMI standards. When unregulated, EMI can degrade devices in the surrounding area and reduce a system's lifetime. PoE devices that supply more power are physically larger, which can take vital room in space-constrained applications.

Figure 5 shows a typical 15W PoE PD power circuit. Due to the number of required components, this circuit is complex and bulky. The optocoupler and TL431 voltage regulator alone comprise their own circuit system with numerous components.
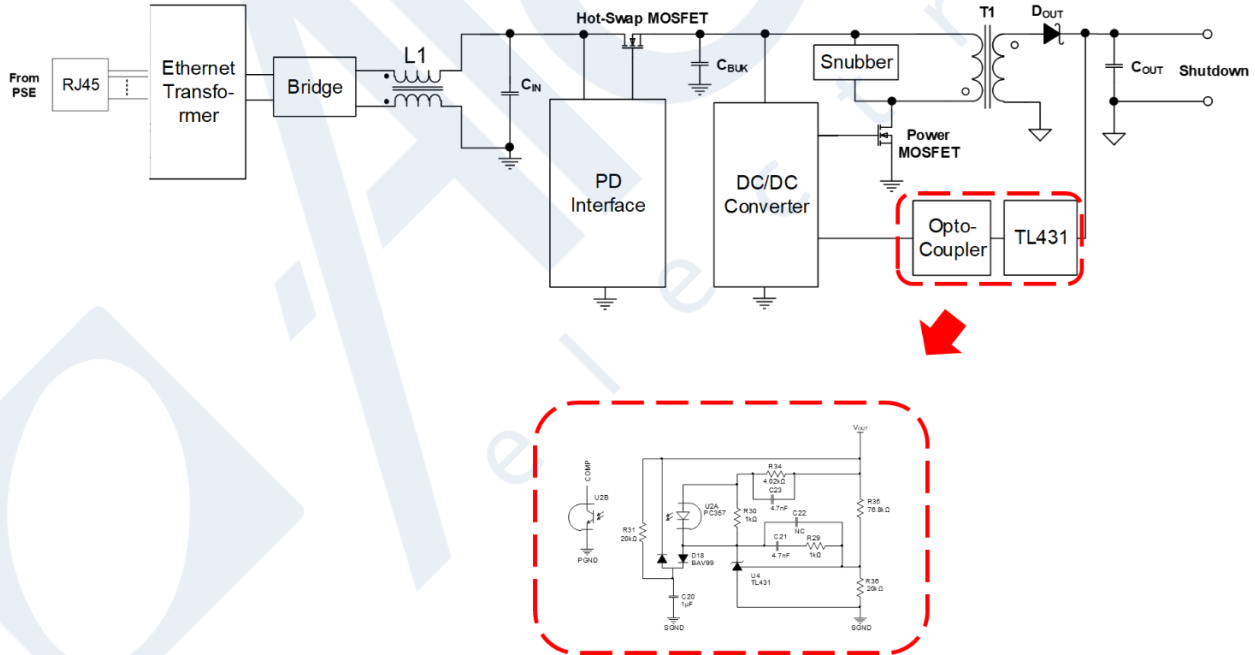

Figure 5: Traditional 15W PD Power Circuit with Optocoupler Feedback

Optimizing a PoE Solution

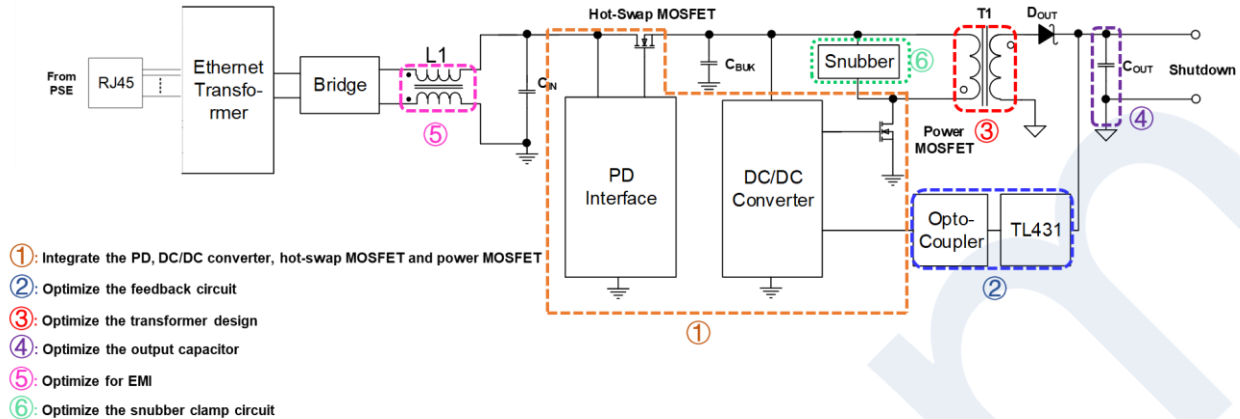There are six simple methods to optimize this circuit (see Figure 6).

Figure 6: Optimizing a PoE PD Design

These methods are described in greater detail below.

1. <u>Full integration</u>: For PoE devices, a completely integrated solution is an excellent way to keep a solution compact. Common questions for PoE solutions include "Can this system include a PD and a DC/DC converter?" and "Can the solution include a hot-swap MOSFET and power MOSFET?"

    The answer to both questions is yes. By integrating the PD, converter, and MOSFETs, designers can significantly reduce the PCB size and design cycle. Integrated solutions also reduce the BOM cost, since a simplified solution requires fewer external components.

2. <u>Feedback circuit</u>: A traditional flyback circuit requires a voltage regulator, optocoupler feedback network, loop compensation, and soft-start circuit. Figure 8 shows the complexity of different circuits, such as a traditional SSR feedback circuit. With the evolution of flyback technology, a primary feedback method was introduced (Gen 1 PSR feedback). This type of circuit typically includes auxiliary winding.

    The MP8017 PoE PD solution uses a new feedback method, called Gen 2 PSR feedback. This system does not require auxiliary winding or an optocoupler (see Figure 7). Instead, the device samples the output voltage (V_{OUT}) from the SW pin. Benefits of this method include:

    a. Simplified design circuit since the transformer does not require auxiliary winding

    b. Reduced transformer cost

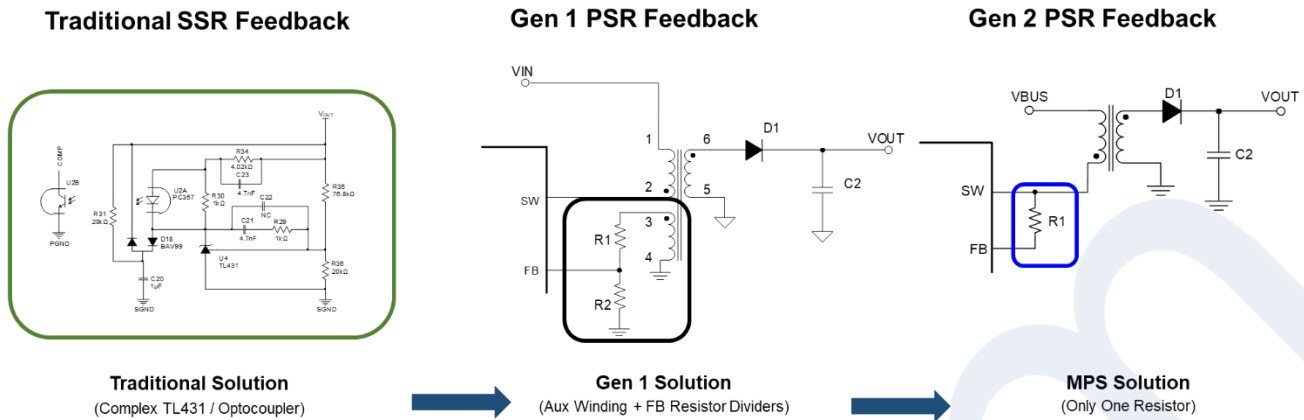   c. Additional power windings that can be wound on the same core to reduce impedance and improve efficiency.

Traditional SSR Feedback   **Gen 1 PSR Feedback**   **Gen 2 PSR Feedback**

Traditional Solution
(Complex TL431 / Optocoupler)

Gen 1 Solution
(Aux Winding + FB Resistor Dividers)

MPS Solution
(Only One Resistor)

Figure 7: Feedback Solutions Comparison

Using this advanced feedback method simplified the circuit and reduces the BOM.

3. <u>Transformer design</u>: For most designs, the transformer is the physically largest and most expensive component in the circuit. Traditionally, an EP13 transformer is used for 12W applications. However, by optimizing the feedback circuit and removing the need for auxiliary winding, designers can implement a high switching frequency (f_{SW}) to reduce the transformer turns. This means an EP7 transformer can replace the EP13, with the EP7 taking up less than a third of the space (see Figure 8).
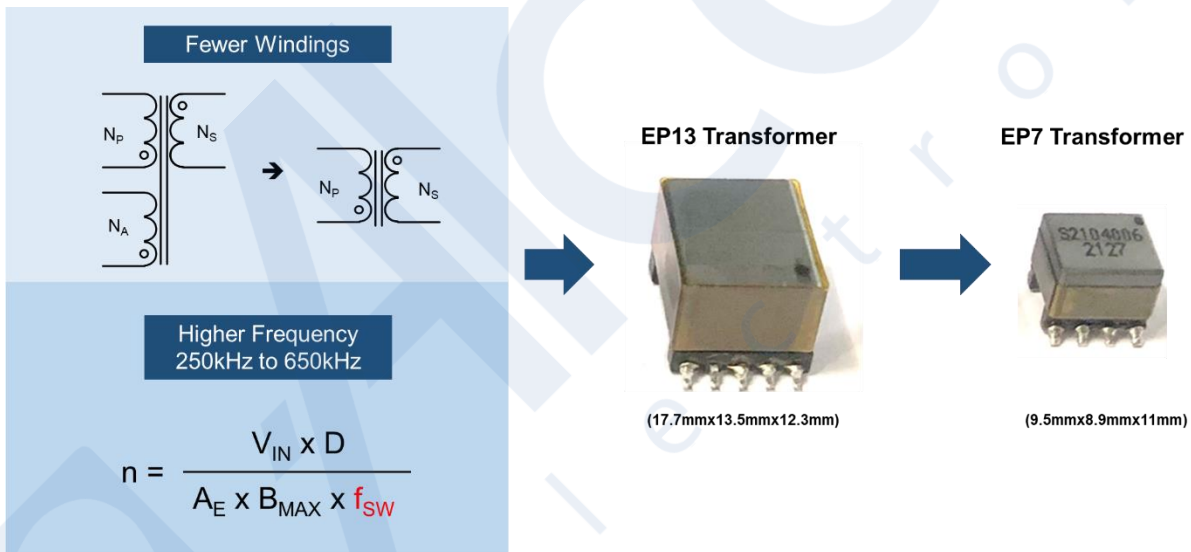

Fewer Windings

**Higher Frequency
250kHz to 650kHz**

$$n = \frac{V_{IN} \times D}{A_E \times B_{MAX} \times f_{SW}}$$

EP13 Transformer

(17.7mmx13.5mmx12.3mm)

EP7 Transformer

(9.5mmx8.9mmx11mm)

Figure 8: EP13 Transformer vs. EP7 Transformer

4. <u>Output capacitance</u>: A conventional PoE device has a typical frequency of about 250kHz, and requires electrolytic capacitors to reduce the output ripple. If f_{SW} increases, the number of output capacitors can be reduced. For example, when f_{SW} is 650kHz, a 12W application only needs two ceramic capacitors with a 0805 size. In addition, by utilizing continuous conduction mode (CCM) control, the transformer's secondary side peak current is smaller. A smaller peak current further reduces the output ripple caused by the output capacitor's ESR and the layout board's resistance. Figure 9 compares the secondary current in both CCM and discontinuous conduction mode (DCM).
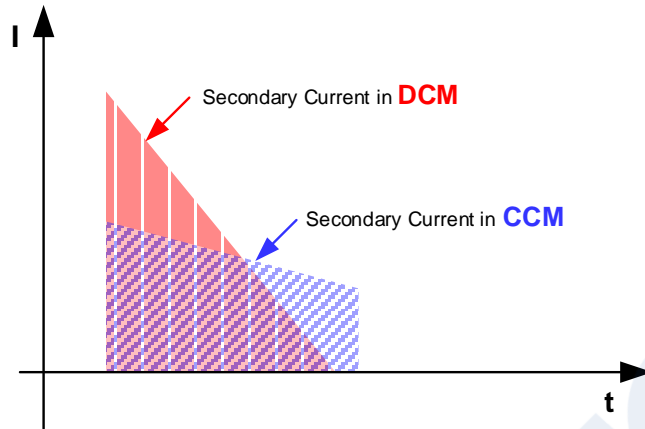
Figure 9: Transformer Secondary Side's Current in DCM and CCM

5. <u>EMI design</u>: All relevant devices must pass EMC standards, but it can be challenging to optimize devices for EMI performance. Flyback solutions typically require a common-mode (CM) inductor to improve EMI performance, though this inductor can be expensive and take up vital PCB space. There are two methods to address EMI challenges without using a CM inductor: supporting spread spectrum frequency dithering, and creating smoother SW waveforms.

In spread spectrum frequency dithering, f_{SW} fluctuates within its nominal range. The MP8017 supports a dither function using its M/D pin. Its frequency dithering is fixed at ±6%, with a modulation frequency of about 9kHz. Figure 10 shows how using frequency dithering can reduce noise spikes.

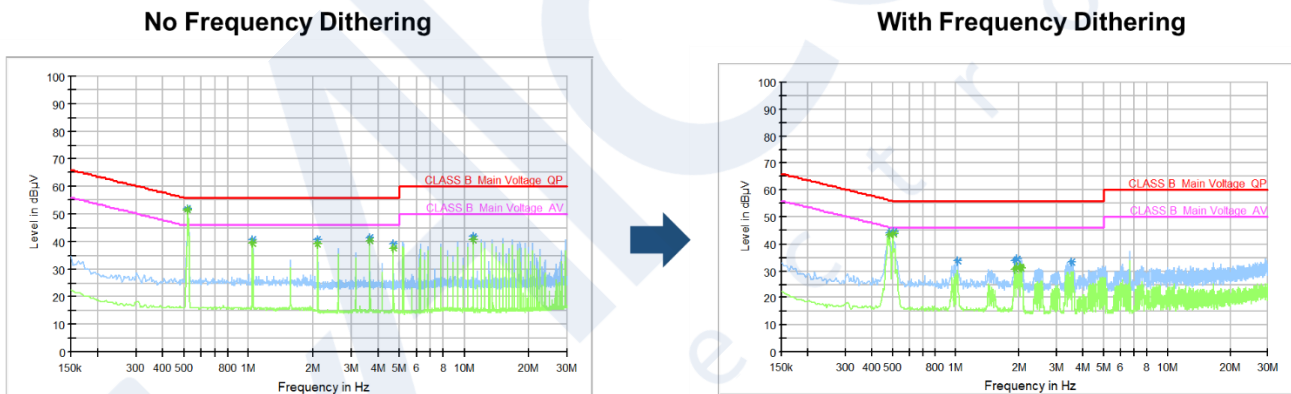**Figure 10: No Frequency Dithering vs. Frequency Dithering**

Optimizing the SW waveform is another way to improve EMI (see Figure 11).
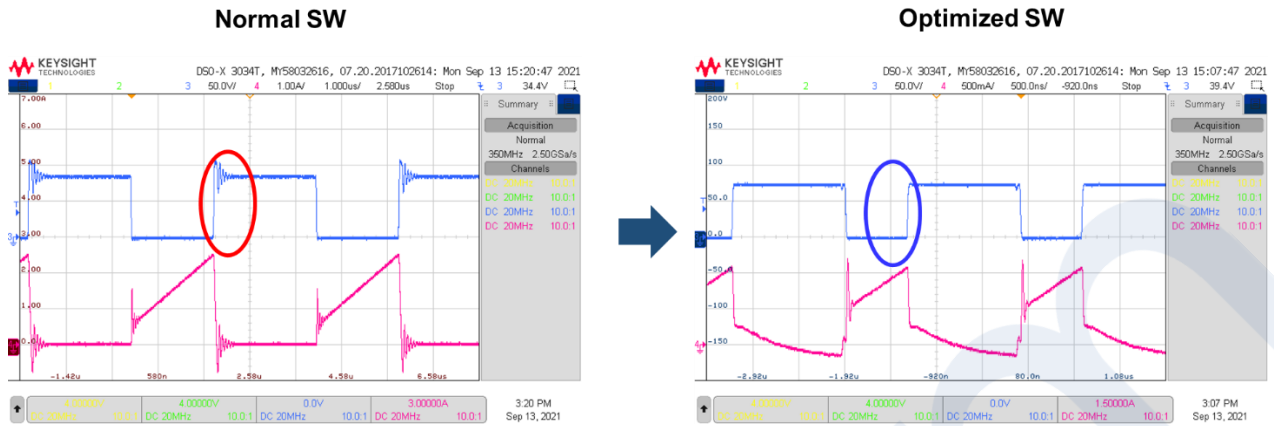
Normal SW **Optimized SW**

Figure 11: Normal SW vs. Optimized SW

EMI performance was greatly improved after implementing these methods with the MP8017, and the CM inductor was removed without reducing EMI performance.

6. <u>Active snubber</u>: In flyback applications, a resistor capacitor diode (RCD) snubber is widely used as the clamping circuit to reduce SW's peak voltage and absorb leakage inductance energy. However, this circuit has two issues:

    a. SW produces resonance, which negatively impacts EMI performance.

    b. System efficiency is reduced after the leakage inductance energy is consumed.

An active clamp control method can mitigate these issues (see Figure 12). This method uses a power MOSFET to replace the resistor and diode found in a traditional RCD snubber. This allows devices such as the MP8017 to implement secondary-side regulation (SSR), which improves efficiency.
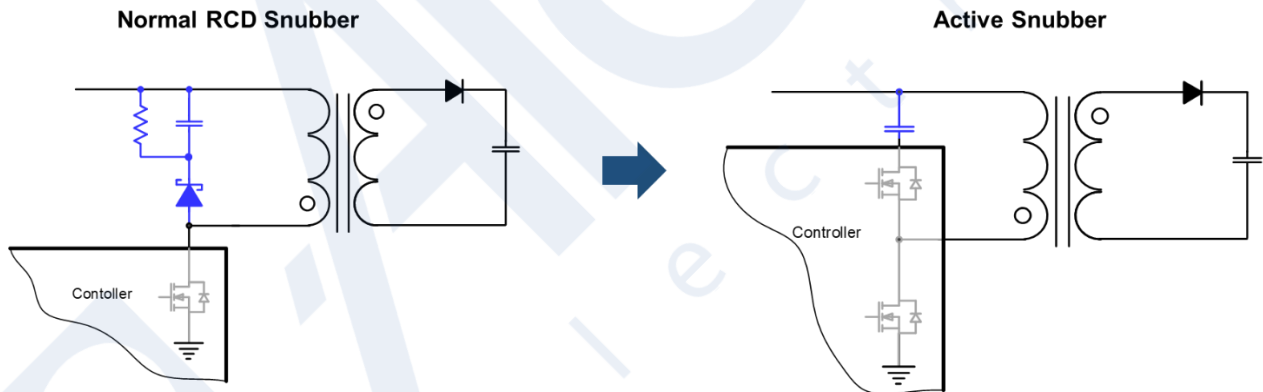
Normal RCD Snubber **Active Snubber**

Figure 12: RCD Snubber vs. Active Snubber

By implementing the six main methods listed above, the final circuit can be greatly simplified compared to a traditional circuit (see Figure 13).
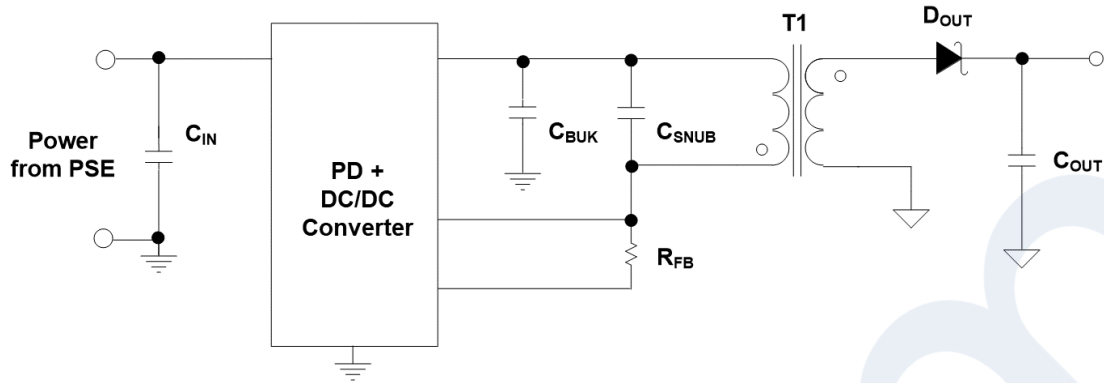
Figure 13: Final Circuit

Conclusion

PoE is an innovative concept that continuously rises to meet the growing power demands of modern technology. Despite its general reliability, it can be difficult for designers to maintain a high efficiency with these solutions, though implementing a few optimization methods can help mitigate these issues. The MP8017 confirmed that selecting optimal transformers, snubbers, and output capacitors — as well as implementing frequency dithering and integrating components onto a single die — are effective methods to guarantee efficient without hindering performance.