S1C31W73 (rev.1.0)

EPSON
EXCEED YOUR VISION

32-bit Single Chip Microcontroller

- Arm® 32-bit RISC CPU core Cortex®-M0+
- Embedded 80SEG x 32COM LCD driver
- Embedded 384K bytes Flash memory, 32K bytes RAM
- Various interfaces such as UART, QSPI, I2C, and USB that support DMA transfer

arm®

■ DESCRIPTIONS

The S1C31W73 is a 32-bit MCU with an Arm® Cortex®-M0+ processor included that features low-power operation. It incorporates an LCD driver capable of driving up to a 2,560-dot LCD panel, a large-capacity Flash memory, and a lot of serial interface circuits. The S1C31W73 is suitable for various kinds of battery-driven controller applications.

■ FEATURES

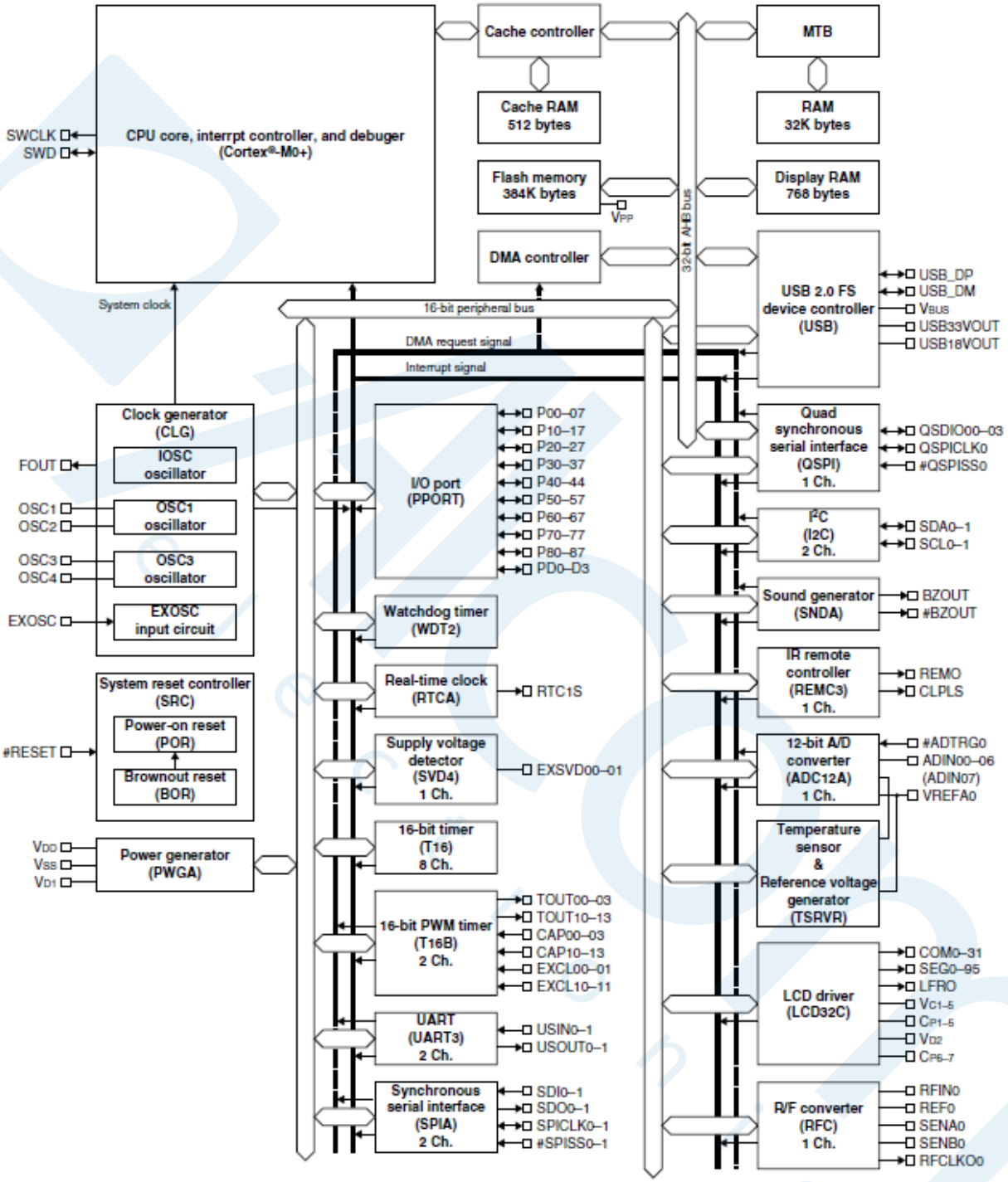
Model	S1C31W73
CPU	
CPU core	Arm® 32-bit RISC CPU core Cortex®-M0+
Other	Serial-wire debug ports (SW-DP) and a micro trace buffer (MTB) included
Embedded Flash memory	
Capacity	384K bytes (for both instructions and data)
Erase/program count	1,000 times (min.) * When being programmed by the dedicated flash loader
Other	On-board programming function
	Flash programming voltage can be generated internally.
Embedded RAMs	
General-purpose RAM	32K bytes (shared with MTB)
Display RAM	768 bytes
Instruction cache	512 bytes
Serial interfaces	
UART (UART3)	2 channels
	Baud-rate generator included, IrDA1.0 supported
	Open drain output, signal polarity, and baud rate division ratio are configurable.
	Infrared communication carrier modulation output function
Synchronous serial interface (SPIA)	2 channels
	2 to 16-bit variable data length
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
Quad synchronous serial interface (QSPI)	1 channel
	Supports single, dual, and quad transfer modes.
	Low CPU overhead memory mapped access mode that can directly read data from the external flash memory with XIP (eXecute-In-Place) mode.
I²C (I2C)	2 channels
	Baud-rate generator included
DMA Controller (DMAC)	
Number of channels	4 channels
Data transfer path	Memory to memory, memory to peripheral, and peripheral to memory
Transfer mode	Basic, ping-pong, scatter-gather
DMA trigger source	UART3, SPIA, QSPI, I2C, T16B, ADC12A, and software
Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency (operating frequency)	V_{D1} voltage mode = mode0: 33 MHz (max.) V_{D1} voltage mode = mode1: 2.1 MHz (max.)
IOSC oscillator circuit (boot clock source)	V_{D1} voltage mode = mode0: 32/24/16/12/8/2/1 MHz (typ.) software selectable (TBD) V_{D1} voltage mode = mode1: 2/1 MHz (typ.) software selectable
	2 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU when the system clock = 32 MHz)
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator
	32 kHz (typ.) embedded oscillator
	Oscillation stop detection circuit included
OSC3 oscillator circuit	16 MHz (max.) crystal/ceramic oscillator
EXOSC clock input	33 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.

I/O port (PPORT)	
Number of general-purpose I/O ports	73bit(max.)
	Pins are shared with the peripheral I/O.
Number of input interrupt ports	69bit(max.)
Number of ports that support universal port multiplexer (UPMUX)	32bit(max.)
	A peripheral circuit I/O function selected via software can be assigned to each port.
Timers	
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.
	Programmable NMI/reset generation cycle
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters
	Theoretical regulation function for 1-second correction
	Alarm and stopwatch functions
16-bit timer (T16)	8 channels
	Generates the SPIA and QSPI master clocks, and the ADC12A operating clock/ trigger signal.
16-bit PWM timer (T16B)	2 channels
	Event counter/capture function
	PWM waveform generation function
	Number of PWM output or capture input ports: 4 ports/channel
Supply voltage detector (SVD4)	
Number of channels	1 channel
Detection voltage	V_{DD} or an external voltage (2 external detection ports are available.)
Detection level	V_{DD}: 32 levels (1.7 to 5.0 V)/external voltage: 32 levels (1.7 to 5.0 V)
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation.
12-bit A/D converter (ADC12A)	
Conversion method	Successive approximation type
Resolution	12 bits
Number of conversion channels	1 channel
Number of analog signal inputs	8 ports/channel (The temperature sensor output is connected to a port.)
Temperature sensor/reference voltage generator (TSRVR)	
Temperature sensor circuit	Sensor output can be measured using ADC12A.
Reference voltage generator	Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, VDD, and external input.
R/F converter (RFC)	
Conversion method	CR oscillation type 24-bit counters
Number of conversion channels	1 channel
Supported sensors	DC bias resistive sensors
IR remote controller (REMC3)	
Number of transmitter channels	1 channel
Other	EL lamp drive waveform can be generated (by the hardware) for an application ex- ample.
	Output inversion function
LCD driver (LCD32C)	
LCD output	96SEG × 1–16COM (max.), 88SEG × 17–24COM (max.), 80SEG × 25–32COM (max.)
LCD contrast	16 levels
Other	1/5 or 1/4 bias power supply included (built-in power supply voltage booster circuit), external voltage can be applied,
USB 2.0 FS device controller (USB)	
Number of transceiver/receiver channels	1 channel
Transfer rate	FS (12 Mbps)
Clock source	PLL (12 MHz OSC3 · 4)
Number of endpoints	4 endpoints (3 general-purpose endpoints and endpoint 0)
Power supply	Voltage regulators for USB included
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Brown-out reset	Reset when the power supply voltage drops
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).
Interrupt	
Non-maskable interrupt	6 systems (Reset, NMI, HardFault, SVCall, PendSV, SysTic)
Programmable interrupt	External interrupt: 1 systems
	Internal interrupt: 27 systems

Power supply voltage	
V_{DD} operating voltage	1.8 to 5.5 V
V_{DD} operating voltage for Flash programming	2.2 to 5.5 V
V_{DD} operating voltage when LCD driver is used	1.8 to 5.5 V
Operating temperature	
Operating temperature range	-40 to 105 °C
Flash programming temperature range	-40 to 85°C
Current consumption (Typ. value)	
SLEEP mode *1	0.7 µA IOSC = OFF, OSC1 = OFF, OSC3 = OFF
	1.2 µA IOSC = OFF, OSC1 = 32kHz, OSC3 = OFF, RTC = ON
HALT mode *2	1.7 µA IOSC = OFF, OSC1 = 32kHz, OSC3 = OFF
	9.7 µA IOSC = OFF, OSC1 = 32kHz, OSC3 = OFF, LCD ON (no panel load)
RUN mode	220 µA/MHz V_{D1} voltage mode = mode0, CPU = IOSC
	150 µA/MHz V_{D1} voltage mode = mode1, CPU = IOSC
Shipping form	
1 *3	QFP21-216PIN (P-LQFP216-2424-0.40, t = 1.7 mm, 0.4 mm pitch)
2	Die form (pad pitch: 80 µm (min.))

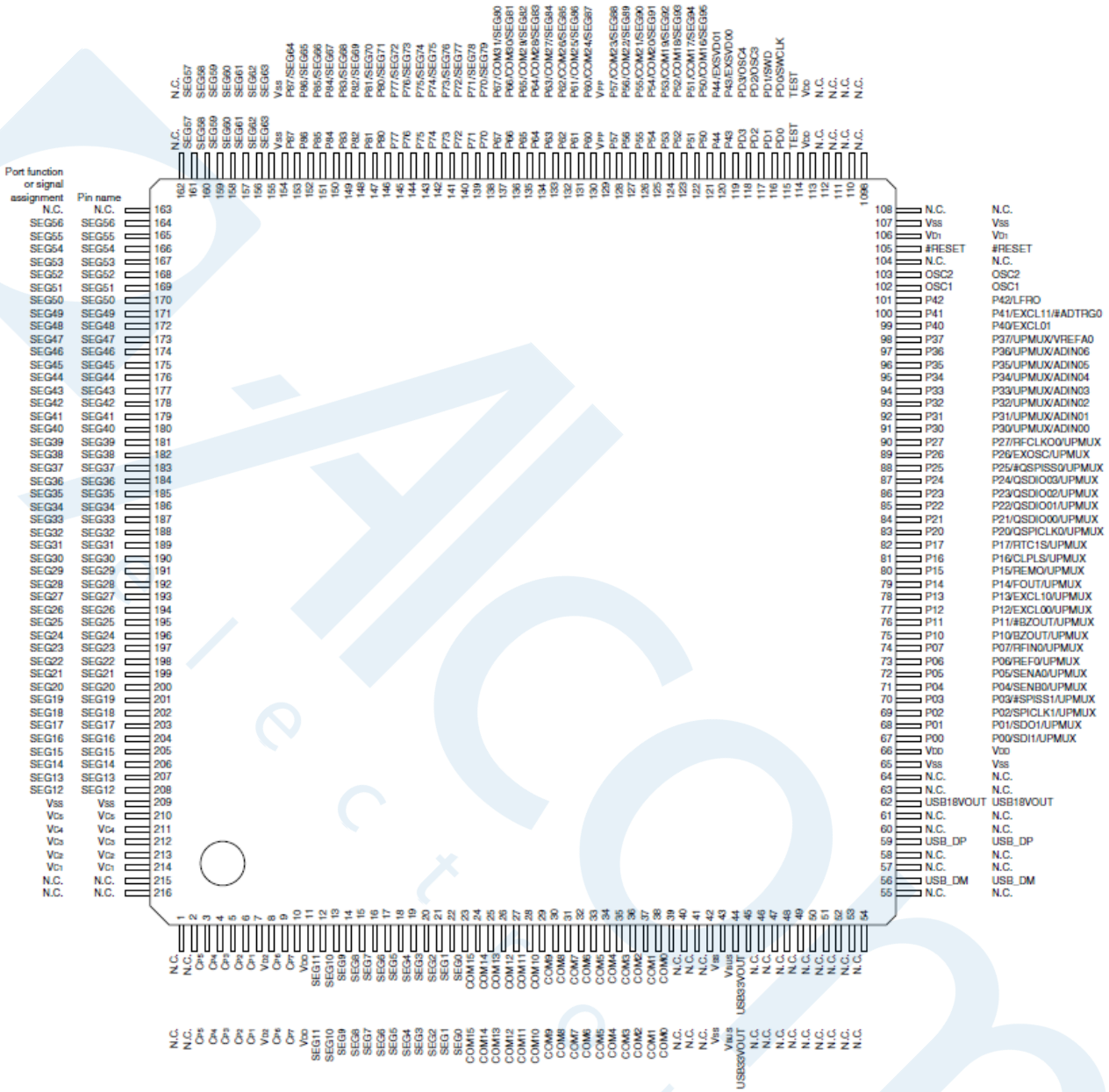
*1 SLEEP mode refers to deep sleep mode in the Cortex®-M0+ processor.
*2 HALT mode refers to sleep mode in the Cortex®-M0+ processor.
*3 Shown in parentheses are JEITA package names.

■ Block Diagram

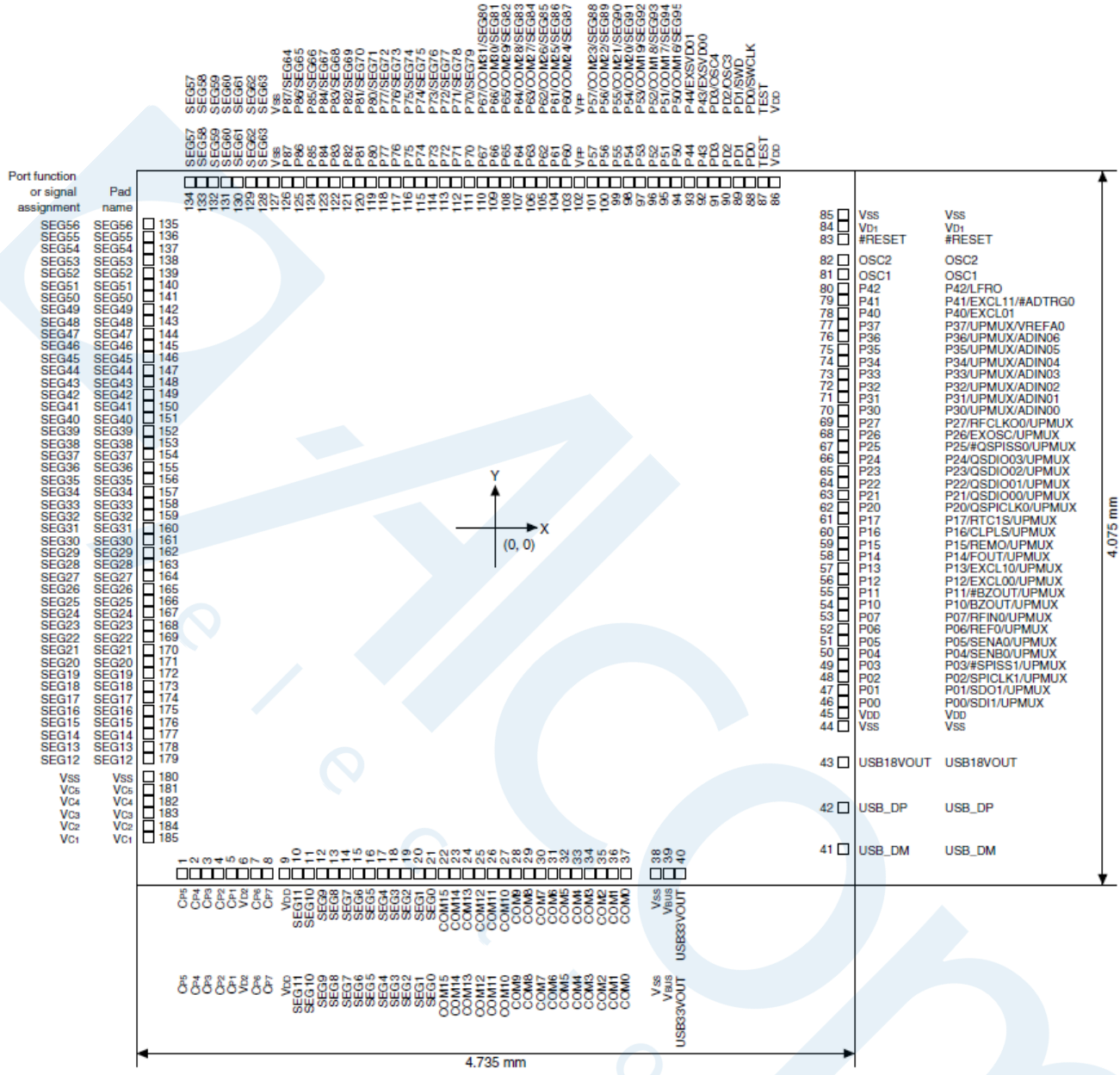


■ Pin Configuration Diagram

QFP21-216PIN



■ Pad Configuration Diagram



Pad opening: X = 68 µm, Y = 68 µm
Chip thickness: 400 µm

■ Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Tolerant fail-safe structure: = Over voltage tolerant fail-safe type I/O cell included

✓ The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD}.

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
VDD	VDD	P	–	–	Power supply (+)
VSS	VSS	P	–	–	GND
VPP	VPP	P	–	–	Power supply for Flash programming
VD1	VD1	A	–	–	VD1 regulator output
VD2	VD2	A	–	–	LCD circuit power supply booster output
VC1–5	VC1–5	P	–	–	LCD panel driver power supply
CP1–5	CP1–5	A	–	–	LCD power supply boost capacitor connect pins
CP6–7	CP6–7	A	–	–	LCD circuit power supply boost capacitor connect pin
OSC1	OSC1	A	-	–	OSC1 oscillator circuit input
OSC2	OSC2	A	-	–	OSC1 oscillator circuit output
TEST	TEST	I	I (Pull-down)	–	Test mode enable input
#RESET	#RESET	I	I (Pull-up)	–	Reset input
P00	P00	I/O	Hi-Z	✓	I/O port
	SDI1	I			Synchronous serial interface Ch.1 data input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P01	P01	I/O	Hi-Z	✓	I/O port
	SDO1	O			Synchronous serial interface Ch.1 data output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P02	P02	I/O	Hi-Z	✓	I/O port
	SPICLK1	I/O			Synchronous serial interface Ch.1 clock input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P03	P03	I/O	Hi-Z	✓	I/O port
	#SPISS1	I			Synchronous serial interface Ch.1 slave-select input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P04	P04	I/O	Hi-Z	✓	I/O port
	SENB0	A			R/F converter Ch.0 sensor B oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P05	P05	I/O	Hi-Z	✓	I/O port
	SENA0	A			R/F converter Ch.0 sensor A oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P06	P06	I/O	Hi-Z	✓	I/O port
	REF0	A			R/F converter Ch.0 reference oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P07	P07	I/O	Hi-Z	✓	I/O port
	RFIN0	A			R/F converter Ch.0 oscillation input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P10	P10	I/O	Hi-Z	✓	I/O port
	BZOUT	O			Sound generator output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P11	P11	I/O	Hi-Z	✓	I/O port
	#BZOUT	O			Sound generator inverted output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P12	P12	I/O	Hi-Z	✓	I/O port
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P13	P13	I/O	Hi-Z	✓	I/O port
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P14	P14	I/O	Hi-Z	✓	I/O port
	FOUT	O			Clock external output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P15	P15	I/O	Hi-Z	✓	I/O port
	REMO	O			IR remote controller transmit data output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P16	P16	I/O	Hi-Z	✓	I/O port
	CLPLS	O			IR remote controller clear pulse output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P17	P17	I/O	Hi-Z	✓	I/O port
	RTC1S	O			Real-time clock 1-second cycle pulse output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P20	P20	I/O	Hi-Z	✓	I/O port
	QSPICLK0	I/O			Quad synchronous serial interface Ch.0 clock input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P21	P21	I/O	Hi-Z	✓	I/O port
	QSDIO00	I/O			Quad synchronous serial interface Ch.0 data input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P22	P22	I/O	Hi-Z	✓	I/O port
	QSDIO01	I/O			Quad synchronous serial interface Ch.0 data input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P23	P23	I/O	Hi-Z	✓	I/O port
	QSDIO02	I/O			Quad synchronous serial interface Ch.0 data input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P24	P24	I/O	Hi-Z	✓	I/O port
	QSDIO03	I/O			Quad synchronous serial interface Ch.0 data input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P25	P25	I/O	Hi-Z	✓	I/O port
	#QSPISS0	I/O			Quad synchronous serial interface Ch.0 slave-select input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P26	P26	I/O	Hi-Z	✓	I/O port
	EXOSC	I			Clock generator external clock input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P27	P27	I/O	Hi-Z	✓	I/O port
	RFCLKO0	O			R/F converter Ch.0 clock monitor output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P30	P30	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN00	A			12-bit A/D converter Ch.0 analog signal input 0
P31	P31	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN01	A			12-bit A/D converter Ch.0 analog signal input 1
P32	P32	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN02	A			12-bit A/D converter Ch.0 analog signal input 2
P33	P33	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN03	A			12-bit A/D converter Ch.0 analog signal input 3
P34	P34	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN04	A			12-bit A/D converter Ch.0 analog signal input 4
P35	P35	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN05	A			12-bit A/D converter Ch.0 analog signal input 5

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P36	P36	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN06	A			12-bit A/D converter Ch.0 analog signal input 6
P37	P37	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	VREFA0	A			12-bit A/D converter Ch.0 reference voltage input
P40	P40	I/O	Hi-Z	–	I/O port
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1
P41	P41	I/O	Hi-Z	✓	I/O port
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	#ADTRG0	I			12-bit A/D converter Ch.0 trigger input
P42	P42	I/O	Hi-Z	✓	I/O port
	LFRO	O			LCD frame signal monitor output
P43	P43	I/O	Hi-Z	✓	I/O port
	EXSVD00	A			Supply voltage detector Ch.0 external voltage detection input 0
P44	P44	I/O	Hi-Z	✓	I/O port
	EXSVD01	A			Supply voltage detector Ch.0 external voltage detection input 1
P50	P50	I/O	Hi-Z	✓	I/O port
	COM16	A			LCD common output
	SEG95	A			LCD segment output
P51	P51	I/O	Hi-Z	✓	I/O port
	COM17	A			LCD common output
	SEG94	A			LCD segment output
P52	P52	I/O	Hi-Z	✓	I/O port
	COM18	A			LCD common output
	SEG93	A			LCD segment output
P53	P53	I/O	Hi-Z	✓	I/O port
	COM19	A			LCD common output
	SEG92	A			LCD segment output
P54	P54	I/O	Hi-Z	✓	I/O port
	COM20	A			LCD common output
	SEG91	A			LCD segment output
P55	P55	I/O	Hi-Z	✓	I/O port
	COM21	A			LCD common output
	SEG90	A			LCD segment output
P56	P56	I/O	Hi-Z	✓	I/O port
	COM22	A			LCD common output
	SEG89	A			LCD segment output
P57	P57	I/O	Hi-Z	✓	I/O port
	COM23	A			LCD common output
	SEG88	A			LCD segment output
P60	P60	I/O	Hi-Z	✓	I/O port
	COM24	A			LCD common output
	SEG87	A			LCD segment output
P61	P61	I/O	Hi-Z	✓	I/O port
	COM25	A			LCD common output
	SEG86	A			LCD segment output
P62	P62	I/O	Hi-Z	✓	I/O port
	COM26	A			LCD common output
	SEG85	A			LCD segment output
P63	P63	I/O	Hi-Z	✓	I/O port
	COM27	A			LCD common output
	SEG84	A			LCD segment output
P64	P64	I/O	Hi-Z	✓	I/O port
	COM28	A			LCD common output
	SEG83	A			LCD segment output
P65	P65	I/O	Hi-Z	✓	I/O port
	COM29	A			LCD common output
	SEG82	A			LCD segment output
P66	P66	I/O	Hi-Z	✓	I/O port
	COM30	A			LCD common output
	SEG81	A			LCD segment output
P67	P67	I/O	Hi-Z	✓	I/O port
	COM31	A			LCD common output
	SEG80	A			LCD segment output
P70	P70	I/O	Hi-Z	✓	I/O port
	SEG79	A			LCD segment output

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P71	P71	I/O	Hi-Z	✓	I/O port
	SEG78	A			LCD segment output
P72	P72	I/O	Hi-Z	✓	I/O port
	SEG77	A			LCD segment output
P73	P73	I/O	Hi-Z	✓	I/O port
	SEG76	A			LCD segment output
P74	P74	I/O	Hi-Z	✓	I/O port
	SEG75	A			LCD segment output
P75	P75	I/O	Hi-Z	✓	I/O port
	SEG74	A			LCD segment output
P76	P76	I/O	Hi-Z	✓	I/O port
	SEG73	A			LCD segment output
P77	P77	I/O	Hi-Z	✓	I/O port
	SEG72	A			LCD segment output
P80	P80	I/O	Hi-Z	✓	I/O port
	SEG71	A			LCD segment output
P81	P81	I/O	Hi-Z	✓	I/O port
	SEG70	A			LCD segment output
P82	P82	I/O	Hi-Z	✓	I/O port
	SEG69	A			LCD segment output
P83	P83	I/O	Hi-Z	✓	I/O port
	SEG68	A			LCD segment output
P84	P84	I/O	Hi-Z	✓	I/O port
	SEG67	A			LCD segment output
P85	P85	I/O	Hi-Z	✓	I/O port
	SEG66	A			LCD segment output
P86	P86	I/O	Hi-Z	✓	I/O port
	SEG65	A			LCD segment output
P87	P87	I/O	Hi-Z	✓	I/O port
	SEG64	A			LCD segment output
PD0	SWCLK	I	I (Pull-up)	✓	Serial-wire debugger clock input
	PD0	I/O			I/O port
PD1	SWD	I/O	I (Pull-up)	✓	Serial-wire debugger data input/output
	PD1	I/O			I/O port
PD2	PD2	I/O	Hi-Z	–	I/O port
	OSC3	A			OSC3 oscillator circuit input
PD3	PD3	I/O	Hi-Z	–	I/O port
	OSC4	A			OSC3 oscillator circuit output
COM0–15	COM0–15	A	Hi-Z	–	LCD common outputs
SEG0–63	SEG0–63	A	Hi-Z	–	LCD segment outputs
USB_DP	USB_DP	I/O	I	–	USB D+ signal input/output
USB_DM	USB_DM	I/O	I	–	USB D- signal input/output
VBUS	VBUS	P	–	–	USB VBUS input (5 V input allowed)
USB18VOUT	USB18VOUT	P	–	–	USB 1.8 V regulator output
USB33VOUT	USB33VOUT	P	–	–	USB 3.3 V regulator output

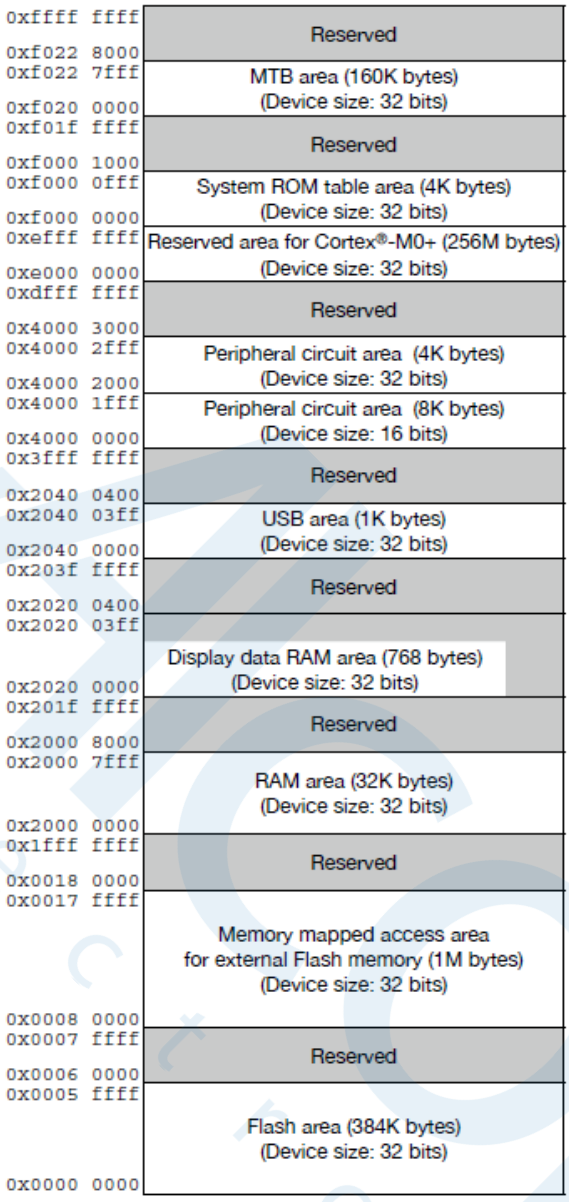
Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
Synchronous serial interface (SPIA)	SDI*n*	I	*n* = 0	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
I^2C (I2C)	SCL*n*	I/O	*n* = 0, 1	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART3)	USIN*n*	I	*n* = 0, 1	UART3 Ch.*n* data input
	USOUT*n*	O		UART3 Ch.*n* data output
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n* = 0, 1	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1
	TOUT*n*2/CAP*n*2	I/O		T16B Ch.*n* PWM output/capture input 2
	TOUT*n*3/CAP*n*3	I/O		T16B Ch.*n* PWM output/capture input 3

Note: Do not assign a function to two or more pins simultaneously.

■ Memory Map


0xffff ffff
0xf022 8000
Reserved
0xf022 7fff
0xf020 0000
MTB area (160K bytes)
(Device size: 32 bits)
0xf01f ffff
0xf000 1000
Reserved
0xf000 0fff
0xf000 0000
System ROM table area (4K bytes)
(Device size: 32 bits)
0xefff ffff
0xe000 0000
Reserved area for Cortex®-M0+ (256M bytes)
(Device size: 32 bits)
0xdfff ffff
0x4000 3000
Reserved
0x4000 2fff
0x4000 2000
Peripheral circuit area (4K bytes)
(Device size: 32 bits)
0x4000 1fff
0x4000 0000
Peripheral circuit area (8K bytes)
(Device size: 16 bits)
0x3fff ffff
0x2040 0400
Reserved
0x2040 03ff
0x2040 0000
USB area (1K bytes)
(Device size: 32 bits)
0x203f ffff
0x2020 0400
Reserved
0x2020 03ff
0x2020 0000
Display data RAM area (768 bytes)
(Device size: 32 bits)
0x201f ffff
0x2000 8000
Reserved
0x2000 7fff
0x2000 0000
RAM area (32K bytes)
(Device size: 32 bits)
0x1fff ffff
0x0018 0000
Reserved
0x0017 ffff
0x0008 0000
Memory mapped access area
for external Flash memory (1M bytes)
(Device size: 32 bits)
0x0007 ffff
0x0006 0000
Reserved
0x0005 ffff
0x0000 0000
Flash area (384K bytes)
(Device size: 32 bits)

Seiko Epson Corporation

Sales & Marketing Division

Device Sales & Marketing Department
29th Floor, JR Shinjuku Miraina Tower, 4-1-6 Shinjuku,
Shinjuku-ku, Tokyo 160-8801, Japan

EPSON semiconductor website

global.epson.com/products_and_drivers/semicon/

Document code: 414011700
First issue May 2020