EFR32BG21B Gecko Wireless SoC Family Data Sheet

The EFR32BG21B SoC is part of the Wireless Gecko portfolio. EFR32BG21B SoCs are ideal for enabling energy-friendly Bluetooth 5 networking for IoT devices.

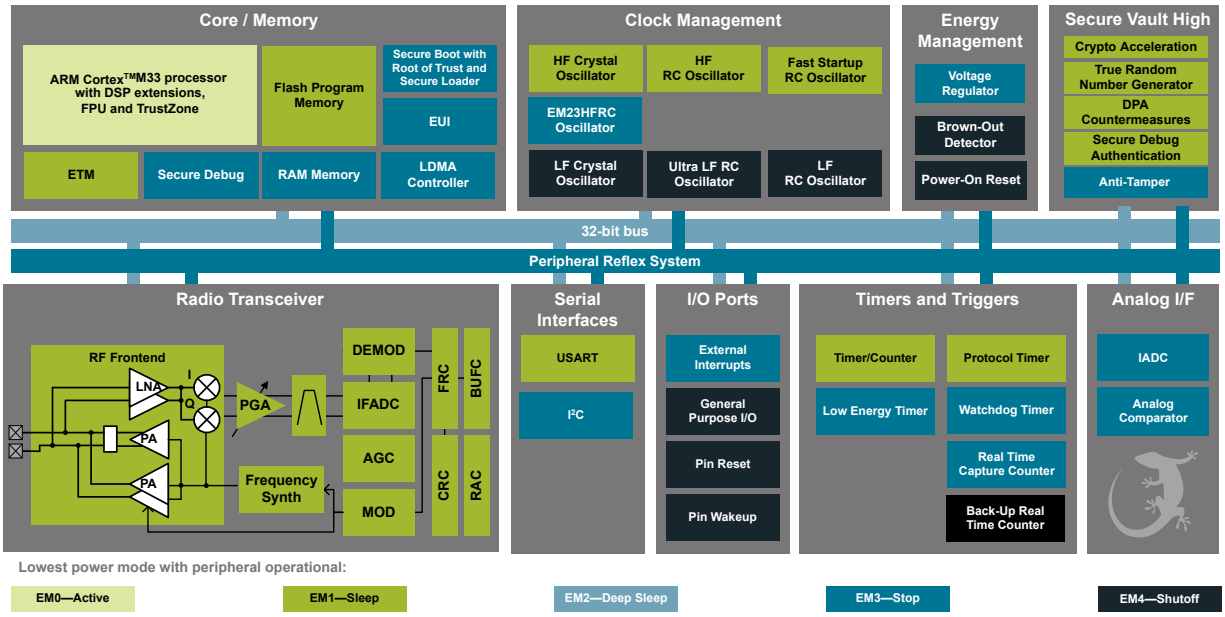
The single-die solution combines an 80 MHz ARM Cortex-M33 a high performance 2.4 GHz radio, and an integrated Hardware Secure Engine to provide a highly secure, energy efficient wireless SoC for IoT connected applications.

EFR32BG21B applications include:

- Lighting
- Connected Home
- Gateways and Digital Assistants
- Building Automation and Security

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 80 MHz maximum operating frequency
- Up to 1024 kB of flash and 96 kB of RAM
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Integrated PA with up to 20 dBm (2.4 GHz) TX power
- Robust peripheral set and up to 20 GPIO in a 4x4 QFN package



1. Feature List

The EFR32BG21B highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 80 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 1024 kB flash program memory
  - Up to 96 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to 20 dBm
- **Low Energy Consumption**
  - 8.8 mA RX current at 2.4 GHz (1 Mbps GFSK)
  - 9.3 mA TX current @ 0 dBm output power at 2.4 GHz
  - 33.8 mA TX current @ 10 dBm output power at 2.4 GHz
  - 50.9 µA/MHz in Active Mode (EM0)
  - 5.0 µA EM2 DeepSleep current

    (96 kB RAM retention and RTC running from LFXO)
  - 4.5 µA EM2 DeepSleep current

    (16 kB RAM retention and RTC running from LFRCO)
- **High Receiver Performance**
  - -97.5 dBm sensitivity @ 1 Mbit/s GFSK
  - -94.4 dBm sensitivity @ 2 Mbit/s GFSK
  - -104.9 dBm sensitivity @ 125 kbps GFSK
- **Supported Modulation Format**
  - GFSK
- **Protocol Support**
  - Bluetooth Low Energy (Bluetooth 5)
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - Up to 20 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 3 × 16-bit Timer/Counter
    - 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter
    - 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 2 × Watchdog Timer
  - 3 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard(ISO 7816)/IrDA/I^2S)
  - 2 × I^2C interface with SMBus support
- **Wide Operating Range**
  - 1.71 V to 3.8 V single power supply
  - -40°C to 125°C ambient
- **Secure Vault**
  - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
  - True Random Number Generator (TRNG)
  - ARM® TrustZone®
  - Secure Boot (Root of Trust Secure Loader)
  - Secure Debug Unlock
  - DPA Countermeasures
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
- **QFN32 4x4 mm Package**
  - 0.4 mm pitch

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power @ Frequency Band	Flash (kB)	RAM (kB)	Secure Vault	GPIO	Package
EFR32BG21B010F1024IM32-B	Bluetooth 5.1	10 dBm @ 2.4 GHz	1024	96	High	20	QFN32
EFR32BG21B010F512IM32-B	Bluetooth 5.1	10 dBm @ 2.4 GHz	512	64	High	20	QFN32
EFR32BG21B010F768IM32-B	Bluetooth 5.1	10 dBm @ 2.4 GHz	768	64	High	20	QFN32
EFR32BG21B020F1024IM32-B	Bluetooth 5.1	20 dBm @ 2.4 GHz	1024	96	High	20	QFN32
EFR32BG21B020F512IM32-B	Bluetooth 5.1	20 dBm @ 2.4 GHz	512	64	High	20	QFN32
EFR32BG21B020F768IM32-B	Bluetooth 5.1	20 dBm @ 2.4 GHz	768	64	High	20	QFN32

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high performance radio transceiver. The devices are well suited for secure connected IoT multiprotocol devices requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG21 Reference Manual.

A block diagram of the EFR32BG21B family is shown in Figure 3.1 Detailed EFR32BG21B Block Diagram on page 7. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

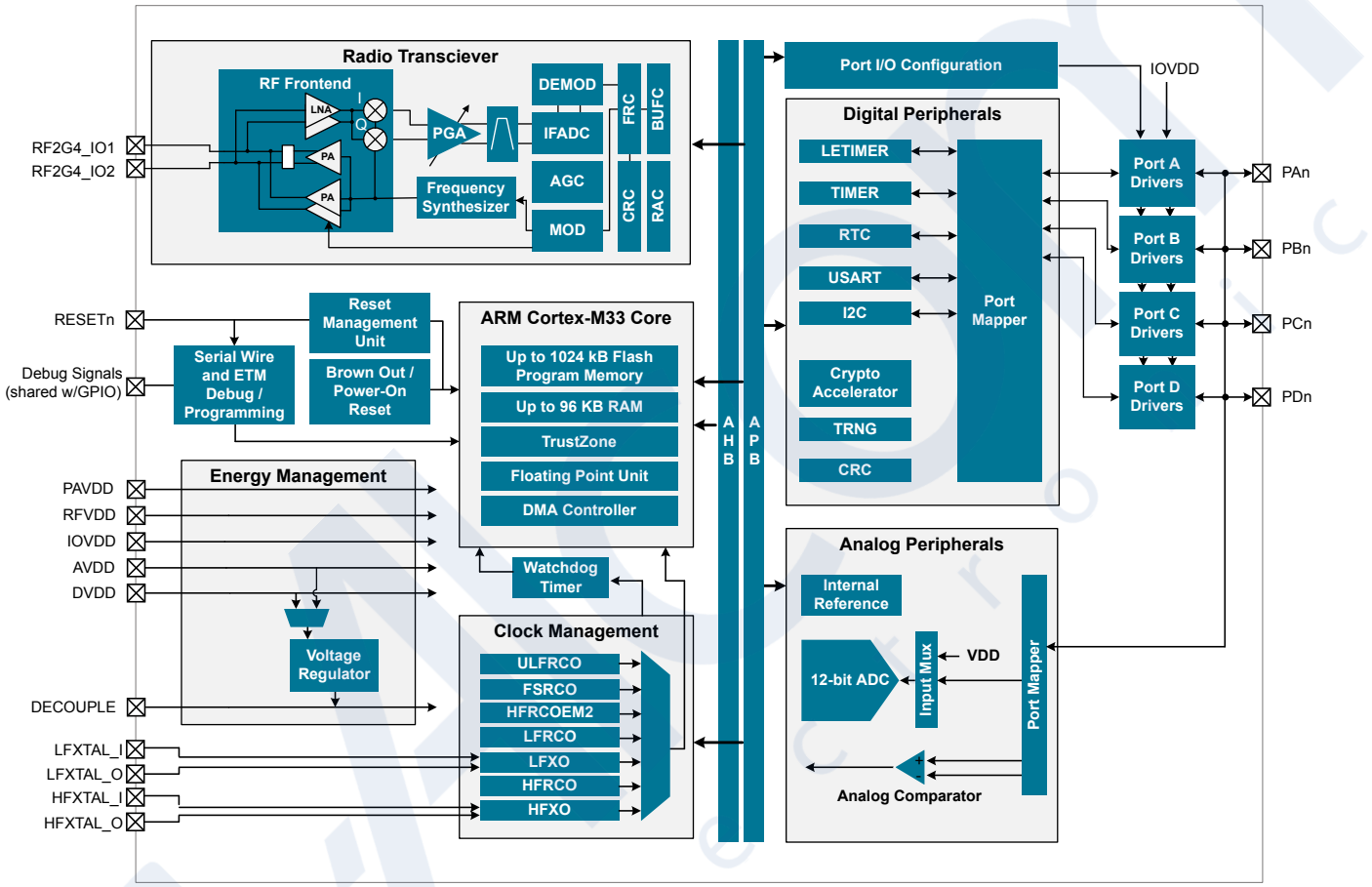

Figure 3.1. Detailed EFR32BG21B Block Diagram

3.2 Radio

The EFR32BG21B features a highly configurable radio transceiver supporting the Bluetooth Low Energy wireless protocol.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of two single-ended pins (RF2G4_IO1 and RF2G4_IO2) that interface directly to two LNAs and two 10 dBm PAs. For devices that support 20 dBm, these pins also interface to the 20 dBm on-chip balun. Integrated switches select either RF2G4_IO1 or RF2G4_IO2 to be the active path.

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32BG21B contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.2.3 Receiver Architecture

The EFR32BG21B uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

3.2.4 Transmitter Architecture

The EFR32BG21B uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32BG21B. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Packet and State Trace

The EFR32BG21B Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.6 Data Buffering

The EFR32BG21B features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.7 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32BG21B. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.3 General Purpose Input/Output (GPIO)

EFR32BG21B has up to 20 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in .

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32BG21B. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFR32BG21B supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU and RF synthesizer. The HFXO provides excellent RF clocking performance using a 38.4 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 80 MHz.
- An integrated high frequency RC oscillator (HFRCOEM2) runs down to EM2 and is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition some timers offer dead-time insertion.

See 3.12 Configuration Summary for information on the feature set of each timer.

3.5.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.5.3 Real Time Clock with Capture (RTCC)

The Real Time Clock with Capture (RTCC) is a 32-bit counter providing timekeeping down to EM3. The RTCC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.5.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined invervals.

3.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes. Note that not all instances of I^2C are avaliable in all energy modes.

3.6.3 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.7 Secure Vault High Features

A dedicated Hardware Secure Engine containing its own CPU enables the Secure Vault High functions. It isolates cryptographic functions and data from the host Cortex-M33 core and provides the following security features:

- Secure Boot with Root of Trust and Secure Loader (RTSL)
- Cryptographic Accelerator
- True Random Number Generator (TRNG)
- Secure Debug with Lock/Unlock
- DPA Countermeasures
- Secure Key Management with PUF
- Anti-Tamper
- Secure Attestation

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed and protects Over The Air updates.

More information on this feature can be found in the Application Note *AN1218: Series 2 Secure Boot with RTSL*.

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.7.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, Secure Vault High also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

More information on this feature can be found in the Application Note *AN1190: Series 2 Secure Debug*.

3.7.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.7.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by what is called "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of being able to protect a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33 (which includes off-chip storage as well). The symmetric key used for this wrapping and unwrapping must be highly secure as it can expose all other key material in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.7.7 Anti-Tamper

Secure Vault High devices provide internal tampers monitoring the system such as voltage, temperature, and electro-mechanical pulses as well as detecting tamper of the security sub-system itself. There are also 8 external configurable tamper pins for supporting external tamper sources like case tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all the protected key material un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

More information on this feature can be found in the Application Note *AN1247: Anti-Tamper Protection Configuration and Use*.

3.7.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory, and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

This secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

More information on this feature can be found in the Application Note *AN1268: Authenticating Silicon Labs Devices Using Device Certificates*.

3.8 Analog

3.8.1 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.2 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of up to 12 bits at up to 1 Msps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage references. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32BG21B. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 1024 kB flash program memory
- Up to 96 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. In addition to the main flash array where Program code is normally written the MSC also provides an Information block where additional information such as special user information or flash-lock bits are stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.11 Memory Map

The EFR32BG21B memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

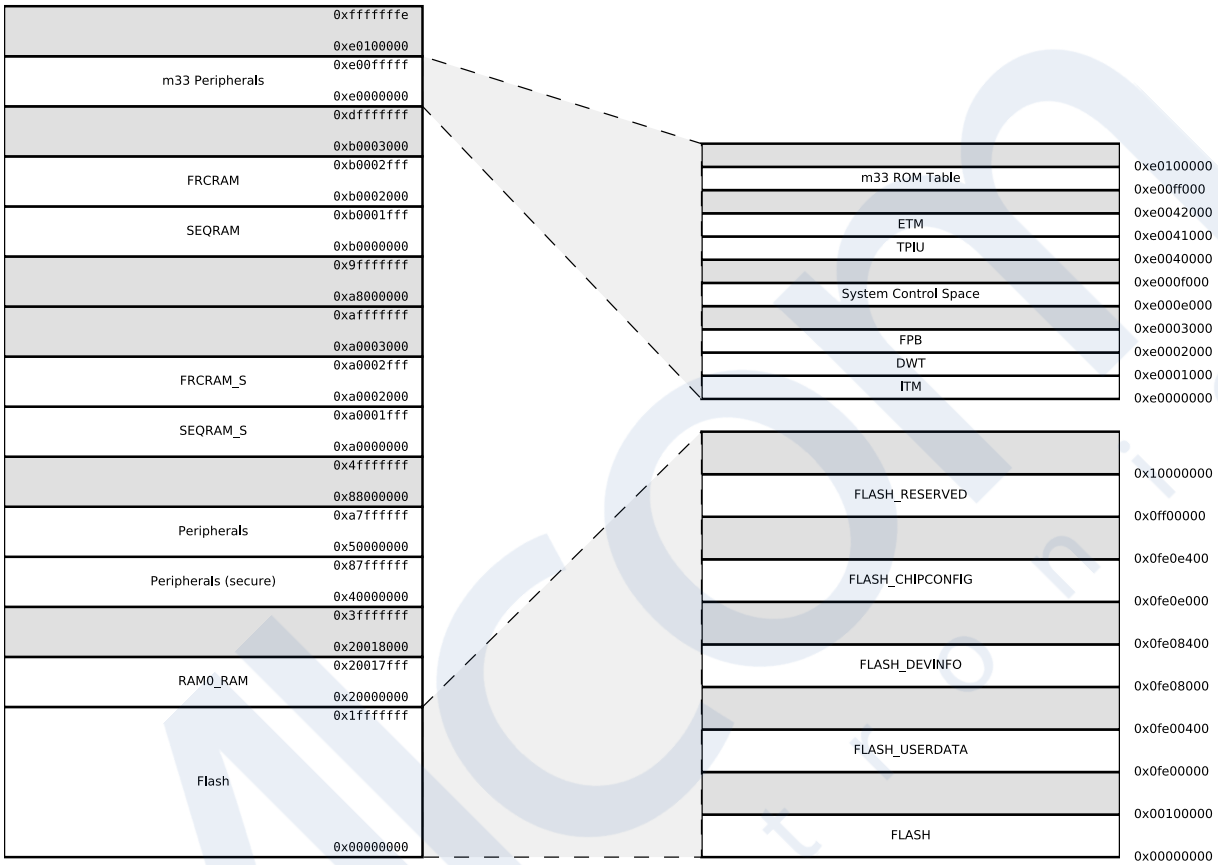

Figure 3.2. EFR32BG21B Memory Map — Core Peripherals and Code Space

3.12 Configuration Summary

The features of the EFR32BG21B are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Lowest Energy Mode	Configuration
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	16-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
USART0	EM1	+IrDA, +I2S, +SmartCard
USART1	EM1	+IrDA, +I2S, +SmartCard
USART2	EM1	+IrDA, +I2S, +SmartCard
I2C0	EM2 / EM3	
I2C1	EM1	

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry (e.g., diodes), some EFR32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pin

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/about-us/corporate-responsibility/commitment-to-quality.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	+150	°C
Junction temperature	T_{JMAX}	-I grade	—	—	+135	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.2	V
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
Input RF level on pins RF2G4_IO1 and RF2G4_IO2	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pins RF2G4_IOx	V_{MAX2G4}		-0.3	—	V_{PAVDD}	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

4.1.2 General Operating Conditions

This table specifies the general operating temperature range and supply voltage range for all supplies. The minimum and maximum values of all other tables are specifed over this operating range, unless otherwise noted.

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-I temperature grade [1]	-40	—	+125	° C
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4[2]	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.0	3.8	V
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.71	3.0	3.8	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.0	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.0	V_{PAVDD}	V
DECOUPLE output capacitor[3]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
HCLK and Core frequency	f_{HCLK}	MODE = WS1, RAMWSEN = 1[4]	—	—	80	MHz
		MODE = WS1, RAMWSEN = 0[4]	—	—	50	MHz
		MODE = WS0, RAMWSEN = 0[4]	—	—	39	MHz
PCLK frequency	f_{PCLK}		—	—	50	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$		—	—	80	MHz
HCLK Radio frequency[5]	$f_{HCLKRADIO}$		38	38.4	40	MHz

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. Flash wait states are set by the MODE field in the MSC_READCTRL register. RAM wait states are enabled by setting the RAMWSEN bit in the SYSYCFG_DMEM0RAMCTRL register.
5. The recommended radio crystal frequency is 38.4 MHz. Any crystal frequency other than 38.4 MHz is expressly not supported. The minimum and maximum HCLKRADIO frequency in this table represent the design limits, which are much wider than the typical crystal tolerance.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient QFN32 (4x4mm) Package	$THE\text{-}TA_{JA\_QFN32\_4X4}$	2-Layer PCB, Natural Convection[1]	—	94.3	—	°C/W
		4-Layer PCB, Natural Convection[1]	—	35.4	—	°C/W
Thermal Resistance Junction to Case QFN32 (4x4mm) Package	$THE\text{-}TA_{JC\_QFN32\_4X4}$	2-Layer PCB, Natural Convection[1]	—	36.3	—	°C/W
		4-Layer PCB, Natural Convection[1]	—	23.5	—	°C/W

Note:

1. Measured according to JEDEC standard JESD51-2A. Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).

4.1.4 Current Consumption

4.1.4.1 MCU current consumption at 1.8V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = 1.8V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.4. MCU current consumption at 1.8V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled[1]	I_{ACTIVE}	80 MHz HFRCO, CPU running Prime from flash	—	50.9	—	µA/MHz
		80 MHz HFRCO, CPU running while loop from flash	—	45.5	—	µA/MHz
		80 MHz HFRCO, CPU running CoreMark loop from flash	—	59.7	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	63.6	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	55.5	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	59.1	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	67.0	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	360	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled[1]	I_{EM1}	80 MHz HFRCO	—	28.7	—	µA/MHz
		38.4 MHz crystal	—	46.7	—	µA/MHz
		38 MHz HFRCO	—	38.7	—	µA/MHz
		26 MHz HFRCO	—	42.2	—	µA/MHz
		16 MHz HFRCO	—	50.0	—	µA/MHz
		1 MHz HFRCO	—	343	—	µA/MHz
Current consumption in EM2 mode	I_{EM2}	Full RAM retention and RTC running from LFXO	—	5.0	—	µA
		Full RAM retention and RTC running from LFRCO	—	5.0	—	µA
		1 bank (16kB) RAM retention and RTC running from LFRCO	—	4.5	—	µA
Current consumption in EM3 mode	I_{EM3}	Full RAM retention and RTC running from ULFRCO	—	4.7	—	µA
		1 bank (16kB) RAM retention and RTC running from ULFRCO	—	4.2	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.14	—	µA
		BURTC with LFXO	—	0.51	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	107	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current Consumption per retained 16kB RAM bank in EM2	I_{RAM}		—	0.10	—	µA

Note:

1. The typical EM0/EM1 current measurement includes some current consumed by the security core for periodical housekeeping purposes. This does not include current consumed by user-triggered security operations, such as cryptographic calculations.

4.1.4.2 MCU current consumption at 3.0V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU current consumption at 3.0V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled[1]	I_{ACTIVE}	80 MHz HFRCO, CPU running Prime from flash	—	50.9	—	µA/MHz
		80 MHz HFRCO, CPU running while loop from flash	—	45.6	55.5	µA/MHz
		80 MHz HFRCO, CPU running CoreMark loop from flash	—	59.8	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	63.8	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	55.6	75.1	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	59.1	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	67.1	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	362	1018	µA/MHz
Current consumption in EM1 mode with all peripherals disabled[1]	I_{EM1}	80 MHz HFRCO	—	28.7	37.6	µA/MHz
		38.4 MHz crystal	—	46.9	—	µA/MHz
		38 MHz HFRCO	—	38.7	57.5	µA/MHz
		26 MHz HFRCO	—	42.2	—	µA/MHz
		16 MHz HFRCO	—	50.2	—	µA/MHz
		1 MHz HFRCO	—	345	994	µA/MHz
Current consumption in EM2 mode	I_{EM2}	Full RAM retention and RTC running from LFXO	—	5.1	—	µA
		Full RAM retention and RTC running from LFRCO	—	5.0	—	µA
		1 bank (16 kB) RAM retention and RTC running from LFRCO	—	4.5	10.5	µA
Current consumption in EM3 mode	I_{EM3}	Full RAM retention and RTC running from ULFRCO	—	4.8	11.4	µA
		1 bank (16 kB) RAM retention and RTC running from ULFRCO	—	4.3	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.21	0.5	µA
		BURTC with LFXO	—	0.61	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	146	—	µA
Current consumption per retained 16kB RAM bank in EM2	I_{RAM}		—	0.10	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The typical EM0/EM1 current measurement includes some current consumed by the security core for periodical housekeeping purposes. This does not include current consumed by user-triggered security operations, such as cryptographic calculations.

4.1.4.3 Radio current consumption at 1.8V

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8V. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. Radio current consumption at 1.8V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.1	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	8.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.4	—	mA
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.8	—	mA
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power	—	9.3	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 0 dBm output power	—	16.6	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power	—	33.8	—	mA

4.1.4.4 Radio current consumption at 3.0V

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0V. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. Radio current consumption at 3.0V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.1	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	8.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.4	—	mA
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.8	—	mA
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power	—	10.5	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 0 dBm output power	—	16.7	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power	—	34.0	—	mA
		f = 2.4 GHz, CW, 20 dBm PA, 10 dBm output power, PAVDD = 3.0 V	—	60.8	—	mA
		f = 2.4 GHz, CW, 20 dBm PA, 20 dBm output power, PAVDD = 3.3 V	—	185	—	mA

4.1.5 2.4 GHz RF Transceiver Characteristics

4.1.5.1 RF Transmitter Characteristics

4.1.5.1.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.8. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power [1]	$POUT_{MAX}$	20 dBm PA, PAVDD = 3.3V	—	+20.2	—	dBm
Maximum TX power	$POUT_{MAX10}$	10 dBm PA	—	+10.5	—	dBm
Maximum TX power	$POUT_{MAX0}$	0 dBm PA	—	+0.4	—	dBm
Minimum active TX power	$POUT_{MIN}$	20 dBm PA, PAVDD = 3.3 V	—	-20.5	—	dBm
		10 dBm PA	—	-19.3	—	dBm
		0 dBm PA	—	-23.5	—	dBm
Output power step size	$POUT_{STEP}$	0 dBm PA,-15 dBm < Output Power < -5 dBm	—	1.5	—	dB
		0 dBm PA,-5 dBm < Output Power < 0 dBm	—	0.3	—	dB
		10 dBm PA, -5 dBm < Output power < 0 dBm	—	1.5	—	dB
		10 dBm PA, 0 dBm < Output power < 10 dBm	—	1.0	—	dB
		20 dBm PA, 0 dBm < Output Power < 5 dBm	—	0.7	—	dB
		20 dBm PA, 5 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs PAVDD supply voltage variation, frequency = 2450MHz	$POUT_{VAR\_V}$	20 dBm PA P_{out} = $POUT_{MAX}$ output power with PAVDD voltage swept from 3.0V to 3.8V.	—	0.8	—	dB
		10 dbm PA output power with PAVDD voltage swept from 1.8 V to 3.0 V	—	0.1	—	dB
		0 dBm PA output power with PAVDD voltage swept from 1.8 V to 3.0 V	—	0.1	—	dB
Output power variation vs temperature, Frequency = 2450MHz	$POUT_{VAR\_T}$	AVDD = 3.3V supply, 20 dBm PA at P_{out} = $POUT_{MAX}$, (-40 to +125 °C)	—	1.5	—	dB
		10 dBm PA at 10 dBm, (-40 to +125 °C)	—	0.3	—	dB
		0 dBm PA at 0 dBm, (-40 to +125 °C)	—	2.1	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output power variation vs RF frequency	$POUT_{VAR\_F}$	20 dBm PA, $POUT_{MAX}$, PAVDD = 3.3 V.	—	0.2	—	dB
		10 dBm PA, 10 dBm	—	0.2	—	dB
		0 dBm PA, 0 dBm	—	0.1	—	dB
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of CW carrier. P_{out} = $POUT_{MAX}$. PAVDD = 3.3V. Test Frequency = 2450MHz.	—	-47	—	dBm
		Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NRR}$	Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V, Test Frequency = 2450MHz.	—	-26	—	dBc
		Continuous transmission of CW carrier. P_{out} = 10 dBm. Test Frequency = 2450 MHz.	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V. Test Frequency = 2450MHz.	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V. Test Frequency = 2450MHz.	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, 20 dBm PA P_{out} = $POUT_{MAX}$, PAVDD = 3.3V. Test Frequency = 2450MHz.	—	-47	—	dBm
		Restricted bands >960 MHz, Continuous transmission of CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V, Test Frequency = 2450MHz.	—	-47	—	dBm
		Restricted bands 30-88 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	1G-14G, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-36	—	dBm
		47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-56	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = 10 dBm, Test Frequency = 2450MHz.	—	-50	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3 V,Test Frequency = 2450 MHz	—	-26	—	dBc
		Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI 300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-26	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = 10 dBm, Test Frequency = 2450MHz.	—	-16	—	dB

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.5.1.2 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.9. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$	—	635.1	—	kHz
		P_{out} = 10 dBm	—	672.9	—	kHz
		P_{out} = 0 dBm	—	646.5	—	kHz
Power spectral density limit	PSD_{LIMIT}	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$, Per FCC part 15.247	—	+6.4	—	dBm/ 3kHz
		P_{out} = 10 dBm, Per FCC part 15.247 at 10 dBm	—	-3.7	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-13.6	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	+10.2	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 10 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$, Inband spurs at ± 2 MHz	—	-26.3	—	dBm
		P_{out} = 10 dbm, Inband spurs at ± 2 MHz	—	-36.4	—	dBm
		P_{out} = 0 dbm, Inband spurs at ± 2 MHz	—	-46.3	—	dBm
		PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$ Inband spurs at ± 3 MHz	—	-20	—	dBm
		P_{out} = 10 dBm Inband spurs at ± 3 MHz	—	-41.9	—	dBm
		P_{out} = 0dbm Inband spurs at ± 3 MHz	—	-51.5	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.1.5.1.3 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.10. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$	—	1238.6	—	kHz
		P_{out} = 10 dBm	—	1182.5	—	kHz
		P_{out} = 0 dBm	—	1249.7	—	kHz
Power spectral density limit	PSD_{LIMIT}	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$, Per FCC part 15.247	—	+3.7	—	dBm/ 3kHz
		P_{out} = 10 dBm, Per FCC part 15.247 at 10 dBm	—	-6.4	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-16.2	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	+9.0	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 10 dBm 99% BW at highest and lowest channels in band	—	2.1	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	2.1	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	PAVDD = 3.3 V P_{out} = $POUT_{MAX}$, Inband spurs at ± 2 MHz	—	-31.7	—	dBm
		P_{out} = 10 dBm, Inband spurs at ± 4 MHz	—	-41.9	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 4 MHz	—	-51.7	—	dBm
		PAVDD = 3.3 V P_{out} = $POUT_{MAX}$ Inband spurs at ± 6 MHz	—	-35.7	—	dBm
		P_{out} = 10 dBm Inband spurs at ± 6 MHz	—	-46.0	—	dBm
		P_{out} = 0 dbm Inband spurs at ± 6 MHz	—	-55.7	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.1.5.1.4 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.11. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$	—	770.9	—	kHz
		P_{out} = 10 dBm	—	760.1	—	kHz
		P_{out} = 0 dBm	—	775.1	—	kHz
Power spectral density limit	PSD_{LIMIT}	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$, Per FCC part 15.247	—	+5.4	—	dBm/ 3kHz
		P_{out} = 10 dBm, Per FCC part 15.247 at 10 dBm	—	-4.6	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-14.4	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	+10.2	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 10 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 10 dbm, Inband spurs at ± 2 MHz	—	-38.3	—	dBm
		P_{out} = 0 dbm, Inband spurs at ± 2 MHz	—	-47.6	—	dBm
		PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$ Inband spurs at ± 3 MHz	—	-20	—	dBm
		P_{out} = 10 dBm Inband spurs at ± 3 MHz	—	-42.3	—	dBm
		P_{out} = 0dbm Inband spurs at ± 3 MHz	—	-51.8	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.1.5.1.5 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.12. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$	—	609.7	—	kHz
		P_{out} = 10 dBm	—	619.3	—	kHz
		P_{out} = 0 dBm	—	617.4	—	kHz
Power spectral density limit	PSD_{LIMIT}	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$, Per FCC part 15.247	—	+14.6	—	dBm/ 3kHz
		P_{out} = 10 dBm, Per FCC part 15.247 at 10 dBm	—	+4.5	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-5.3	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	+10.1	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 10 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$, Inband spurs at ± 2 MHz	—	-27.7	—	dBm
		P_{out} = 10 dbm, Inband spurs at ± 2 MHz	—	-38.5	—	dBm
		P_{out} = 0 dbm, Inband spurs at ± 2 MHz	—	-47.8	—	dBm
		PAVDD = 3.3 V, P_{out} = $POUT_{MAX}$ Inband spurs at ± 3 MHz	—	-20	—	dBm
		P_{out} = 10 dBm Inband spurs at ± 3 MHz	—	-42.4	—	dBm
		P_{out} = 0dbm Inband spurs at ± 3 MHz	—	-51.8	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.1.5.2 RF Receiver Characteristics

4.1.5.2.1 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.13. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-54.8	—	dBm
		1 GHz to 12 GHz	—	-57.1	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, conducted measurement	—	-54.8	—	dBm
		Above 960 MHz, conducted measurement.	—	-77.3	—	dBm

4.1.5.2.2 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.14. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-97.5	—	dBm
		With non-ideal signals[2] [1]	—	-97.1	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [3]	—	+6.6	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [4] [3] [5]	—	-8.3	—	dB
		Interferer is reference signal at -1 MHz offset[1] [4] [3] [5]	—	-8.7	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [4] [3] [5]	—	-42.1	—	dB
		Interferer is reference signal at -2 MHz offset[1] [4] [3] [5]	—	-48.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [4] [3] [5]	—	-42.4	—	dB
		Interferer is reference signal at -3 MHz offset[1] [4] [3] [5]	—	-54.8	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [5]	—	-42.1	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [5]	—	-42.4	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [5]	—	-8.3	—	dB
Intermodulation performance	IM	n = 3 [6]	—	-23	—	dBm

Note:

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.1.5.2.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.15. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-94.4	—	dBm
		With non-ideal signals[2 1]	—	-94.3	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	+6.0	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-8.0	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-8.8	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 4 3 5]	—	-42.2	—	dB
		Interferer is reference signal at -4 MHz offset[1 4 3 5]	—	-50.3	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 4 3 5]	—	-54.4	—	dB
		Interferer is reference signal at -6 MHz offset[1 4 3 5]	—	-55.4	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-8.0	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 5]	—	-42.2	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 5]	—	+6.0	—	dB
Intermodulation performance	IM	n = 3[6]	—	-22.3	—	dBm

Note:

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.1.5.2.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.16. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal[1]	—	-100.6	—	dBm
		With non-ideal signals[2 1]	—	-100.0	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	+2.1	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 4 3 5]	—	-9.0	—	dB
		Interferer is reference signal at -1 MHz offset[1 4 3 5]	—	-9.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-44.4	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-51.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 4 3 5]	—	-44.3	—	dB
		Interferer is reference signal at -3 MHz offset[1 4 3 5]	—	-58.3	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-44.4	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-44.3	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-9.0	—	dB

Note:

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -72 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.1.5.2.5 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.17. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal[1]	—	-104.9	—	dBm
		With non-ideal signals[2 1]	—	-104.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	+0.8	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 4 3 5]	—	-13.1	—	dB
		Interferer is reference signal at -1 MHz offset[1 4 3 5]	—	-13.6	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-49.5	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-56.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 4 3 5]	—	-47.0	—	dB
		Interferer is reference signal at -3 MHz offset[1 4 3 5]	—	-63.1	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-49.5	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-47.0	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-13.1	—	dB

Note:

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -79 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.1.6 Flash Characteristics

Table 4.18. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure[1]	EC_{FLASH}	$T_A \leq 125$ °C	10,000	—	—	cycles
Flash data retention[1]	RET_{FLASH}	$T_A \leq 125$ °C	10	—	—	years
Program Time	t_{PROG}	one word (32-bits)	40.2	44.0	47.9	uSec
		average per word over 128 words	9.97	10.9	11.9	uSec
Page Erase Time[2]	t_{PERASE}		11.6	12.7	13.9	ms
Mass Erase Time[3] [4]	t_{MERASE}		11.7	12.8	14.1	ms
Page Erase Current	I_{ERASE}	T_A = 25 °C	—	—	2.13	mA
Program Current	I_{WRITE}	T_A = 25 °C	—	—	2.73	mA
Mass Erase Current	I_{MERASE}	T_A = 25 °C	—	—	2.30	mA
Flash Supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Page Erase time is measured from setting the ERASEPAGE bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.
3. Mass Erase is issued by the CPU and erases all of User space.
4. Mass Erase time is measured from setting the ERASEMAIN0 bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.

4.1.7 Wake Up, Entry, and Exit times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.19. Wake Up, Entry, and Exit times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
WakeupTime from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	AHB Clocks
		Code execution from RAM	—	1.43	—	µs
WakeupTime from EM2	t_{EM2_WU}	Code execution from flash	—	12.2	—	µs
		Code execution from RAM	—	3.92	—	µs
		Code execution from flash @ 80 MHz	—	9.00	—	µs
		Code execution from RAM @ 80 MHz	—	2.87	—	µs
WakupTime from EM3	t_{EM3_WU}	Code execution from flash	—	12.2	—	µs
		Code execution from RAM	—	3.92	—	µs
		Code execution from flash @ 80 MHz	—	9.00	—	µs
		Code execution from RAM @ 80 MHz	—	2.87	—	µs
WakeupTime from EM4	t_{EM4_WU}	Code execution from Flash	—	17.8	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.52	—	µs
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	74.0	—	µs
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	74.0	—	µs
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	84.1	—	µs

4.1.8 Oscillators

4.1.8.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.20. High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{HFXO}	see note[1]	—	38.4	—	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	38.4 MHz, CL = 10 pF[2]	—	—	40	Ω
Supported range of crystal load capacitance	C_{HFXO_LC}	38.4 MHz, ESR = 40[3]	—	10	—	pF
Supply Current	I_{HFXO}		—	500	—	µA
Startup Time	$T_{STARTUP}$	38.4 MHz, ESR = 40 Ohm, CL = 10 pF	—	160	—	µs
On-chip tuning cap step size[4]	SS_{HFXO}		—	0.04	—	pF

Note:

1. The BLE radio requires a 38.4 MHz crystal with a tolerance of ± 50 ppm over temperature and aging. Please use the recommended crystal.
2. The crystal should have a maximum ESR less than or equal to this maximum rating.
3. It is recommended to use a crystal with a 10 pF load capacitance rating. Only crystals with a 10 pF load cap rating have been characterized for RF use.
4. The tuning step size is the effective step size when incrementing one of the tuning capacitors by one count. The step size for the each of the indivdual tuning capacitors is twice this value.

4.1.8.2 Low Frequency Crystal Oscillator

Table 4.21. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kOhm, CL = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	357	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kOhm, CL = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	63	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.1.8.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.22. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F_{HFRCO_ACC}	For all production calibrated frequencies	-3	—	+3	%
Current consumption on all supplies [1]	I_{HFRCO}	F_{HFRCO} = 1 MHz	—	27	—	µA
		F_{HFRCO} = 2 MHz	—	27	—	µA
		F_{HFRCO} = 4 MHz	—	27	—	µA
		F_{HFRCO} = 7 MHz	—	59	—	µA
		F_{HFRCO} = 13 MHz	—	77	—	µA
		F_{HFRCO} = 16 MHz	—	87	—	µA
		F_{HFRCO} = 19 MHz	—	90	—	µA
		F_{HFRCO} = 26 MHz	—	116	—	µA
		F_{HFRCO} = 32 MHz	—	139	—	µA
		F_{HFRCO} = 38 MHz[2]	—	170	—	µA
		F_{HFRCO} = 40 MHz[3]	—	172	—	µA
		F_{HFRCO} = 48 MHz[2]	—	207	—	µA
		F_{HFRCO} = 56 MHz[2]	—	228	—	µA
		F_{HFRCO} = 64 MHz[2]	—	269	—	µA
		F_{HFRCO} = 80 MHz[2]	—	285	—	µA
Clock out current for HFRCODPLL[4]	$I_{CLKOUT\_HFRCODPLL}$	FORECEEN bit of HFRCO0_CTRL = 1	—	3.0	—	µA/MHz
Clock Out current for HFRCOEM23[4]	$I_{CLKOUT\_HFRCOEM23}$	FORECEEN bit of HFRCOEM23_CTRL = 1	—	1.6	—	µA/MHz
Coarse trim step Size (% of period)	SS_{HFRCO_COARSE}	Step size measured at coarse trim mid-scale. (Fine trim also set to mid scale.)	—	0.64	—	%
Fine trim step Size (% of period)	SS_{HFRCO_FINE}	Step size measured at fine trim mid-scale. (Coarse trim also set to mid scale.)	—	0.1	—	%
Period jitter	PJ_{HFRCO}	19 MHz	—	0.04	—	% RMS
Startup Time[5]	$T_{STARTUP}$	FREQRANGE = 0 to 7	—	3.2	—	µs
		FREQRANGE = 8 to 15	—	1.2	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band Frequency Limits[6]	f_{HFRCO_BAND}	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17.0	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33.0	—	51.0	MHz
		FREQRANGE = 13	42.2	—	64.6	MHz
		FREQRANGE = 14	48.8	—	74.8	MHz
		FREQRANGE = 15	57.6	—	87.4	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. This frequency is calibrated for the HFRCODPLL only.
3. This frequency is calibrated for the HFRCOEM23 only.
4. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
5. Hardware delay ensures setting to within +-0.5%. Hardware also enforces this delay on a band change.
6. The frequency band limits represent the lowest and highest freqeuncy which each band can achieve over the operating range.

4.1.8.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.23. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		17.2	20	21.2	MHz

4.1.8.5 Low Frequency RC Oscillator

Table 4.24. Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		31.785	32.768	33.751	kHz
Frequency calibration step	F_{TRIM_STEP}	Typical trim step at mid-scale	—	0.33	—	%
Startup time	$T_{STARTUP}$		—	220	—	µs
Current consumption	I_{LFRCO}		—	186	—	nA

4.1.8.6 Ultra Low Frequency RC Oscillator

Table 4.25. Ultra Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	F_{ULFRCO}		0.944	1.0	1.095	kHz

4.1.9 GPIO Pins (3V GPIO pins)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = 3.0 V.

Table 4.26. GPIO Pins (3V GPIO pins)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	200	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3*IOVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7*IOVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*IOVDD	—	—	V
		RESETn	0.05*DVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.62 V	—	—	0.4 * IOVDD	V
Output high voltage	V_{OH}	Sourcing 20mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.62 V	0.6 * IOVDD	—	—	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.7V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.7V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	R_{PULL}	pull-up: MODEn = DISABLE DOUT=1, pull-down: MODEn = WIREDORPULLDOWN DOUT = 0	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	26	—	ns

Note:
1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.1.10 Analog to Digital Converter (ADC)

Unless otherwise indicated, typical conditions are: ADCCLK=10 MHz, OSR=2

Table 4.27. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	V_{AVDD}	Normal mode	1.71	—	3.8	V
Maximum Input Range[1]	V_{IN_MAX}	Maximum allowable input voltage	0	—	AVDD	V
Full-Scale Voltage	V_{FS}	Voltage required for Full-Scale measurement	—	V_{REF} / Gain	—	
Input Measurement Range	V_{IN}	Differential Mode - Plus and Minus inputs	$-V_{FS}$	—	$+V_{FS}$	V
		Single Ended Mode - One input tied to ground	0	—	V_{FS}	V
Input Sampling Capacitance	Cs	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	f_{CLK}	(1 Mbps)	—	—	10	MHz
Throughput rate	f_{SAMPLE}	f_{CLK} = 10 MHz	—	—	1	Msps
Current from all supplies, Continuous operation	$I_{ADC\_CONTINUOUS}$	1 Msps, OSR=2, f_{CLK} = 10 MHz	—	290	385	µA
Current in Standby mode. ADC is not functional but can wake up in 1us.	I_{STBY}	Normal Mode	—	16.3	—	µA
ADC Startup Time	$t_{startup}$	From power down state	—	5	—	µs
		From Standby state	—	1	—	µs
ADC Resolution	Resolution	Max value is at OSR=64	—	12	—	bits
Differential Nonlinearity	DNL	Differential Input. (No missing codes)	-1	+/- 0.25	+1.5	LSB12
Integral Nonlinearity	INL	Differential Input.	-2.5	+/- 0.65	-+2.5	LSB12
Effective number of bits	ENOB	Differential Input. Gain=1x, f_{IN} = 10 kHz, Internal VREF=1.21V.	10.5	11.18	—	bits
Signal to Noise + Distortion Ratio Normal Mode	SNDR	Differential Input. Gain=1x,f_{IN} = 10 kHz, Internal VREF=1.21V	65	69.1	—	dB
		Differential Input. Gain=2x, f_{IN} = 10 kHz, Internal VREF=1.21V	—	68.8	—	dB
		Differential Input. Gain=4x, f_{IN} = 10 kHz, Internal VREF=1.21V	—	66.9	—	dB
		Differential Input. Gain=0.5x, f_{IN} = 10 kHz, Internal VREF=1.21V	—	69.2	—	dB
Total Harmonic Distortion	THD	Differential Input. Gain=1x, f_{IN} =10 kHz, Internal VREF=1.21V	—	-80.3	-70	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range	SFDR	Differential Input. Gain=1x, f_{IN} = 10 kHz, Internal VREF=1.21V	72	86.5	—	dB
Common Mode Rejection Ratio	CMRR	Normal mode. DC to 100 Hz	—	87.0	—	dB
		Normal mode. AC (measured at 500 kHz)	—	68.6	—	dB
Power Supply Rejection Ratio	PSRR	DC to 100 Hz	—	80.4	—	dB
		AC high frequency, using VREF_pad (measured at 500 kHz)	—	33.4	—	dB
		AC high frequency, using internal VBGR (measured at 500 kHz)	—	65.2	—	dB
Gain Error	GE	GAIN = 1 and 0.5, using external VREF, direct mode.	-0.3	0.069	0.3	%
		GAIN = 2, using external VREF, direct mode.	-0.4	0.151	0.4	%
		GAIN = 3, using external VREF, direct mode.	-0.7	0.186	0.7	%
		GAIN = 4, using external VREF, direct mode.	-1.1	0.227	1.1	%
		Internal VREF, Gain=1	—	0.023	—	%
Offset	OFFSET	GAIN = 1 and 0.5, Differential Input	-3	0.27	3	LSB
		GAIN = 2, Differential Input	-4	0.27	4	LSB
		GAIN = 3, Differential Input	-4	0.25	4	LSB
		GAIN = 4, Differential Input	-4	0.29	4	LSB
External reference voltage range[1]	V_{EVREF}		1.0	—	AVDD	V
Internal Reference voltage	V_{IVREF}		—	1.21	—	V

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.

4.1.11 Analog Comparator (ACMP)

Table 4.28. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ACMP Supply current from AVDD pin	I_{ACMP}	BIAS = 4, HYST = DISABLED	—	4.17	—	µA
		BIAS = 5, HYST = DISABLED	—	8.96	—	µA
		BIAS = 6, HYST = DISABLED	—	23.1	—	µA
		BIAS = 7, HYST = DISABLED	—	43.9	70	µA
ACMP Supply current from AVDD pin with Hysteresis	I_{ACMP_WHYS}	BIAS = 4, HYST = SYM30MV	—	5.98	—	µA
		BIAS = 5, HYST = SYM30MV	—	13.0	—	µA
		BIAS = 6, HYST = SYM30MV	—	33.6	—	µA
		BIAS = 7, HYST = SYM30MV	—	64.2	—	µA
Comparator delay with 100mV overdrive	T_{DELAY}	BIAS = 4	—	155	—	ns
		BIAS = 5	—	86.6	—	ns
		BIAS = 6	—	50.6	—	ns
		BIAS = 7	—	39.9	—	ns
Input offset voltage	V_{OFFSET}	BIAS = 4, VCM = 0.15 to AVDD - 0.15	-25	—	+25	mV
		BIAS = 7, VCM = 0.15 to AVDD - 0.15	-30	—	+30	mV
Input Range	V_{IN}	Input Voltage Range	0	—	AVDD	V
Hysteresis (BIAS = 4)	V_{HYST}	HYST = SYM10MV[1]	—	21.2	—	mV
		HYST = SYM20MV[1]	—	39.9	—	mV
		HYST = SYM30MV[1]	—	57.6	—	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V Reference	1.19	1.25	1.31	V
		Internal 2.5 V Reference	2.34	2.5	2.75	V
Capacitive Sense Oscillator Resistance	$R_{CSRESSEL}$	CSRESSEL = 0	—	14	—	kΩ
		CSRESSEL = 1	—	24	—	kΩ
		CSRESSEL = 2	—	43	—	kΩ
		CSRESSEL = 3	—	60	—	kΩ
		CSRESSEL = 4	—	80	—	kΩ
		CSRESSEL = 5	—	99	—	kΩ
		CSRESSEL = 6	—	120	—	kΩ

Note:
1. V_{CM} = 1.25 V

4.1.12 Temperature Sense

Table 4.29. Temperature Sense

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range	T_{sense_range}		-40	—	125	°C
Temperature sensor resolution	$T_{senseRes}$		—	0.25	—	°C

4.1.13 Brown Out Detectors

4.1.13.1 DVDD BOD

BOD Thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.30. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply Rising	—	1.67	1.71	V
		Supply Falling	1.62	1.65	—	V
BOD response time	$t_{DVDD\_BOD\_DELAY}$	Supply dropping at 100mV/µs slew rate[1]	—	0.95	—	µs
BOD hysteresis	$V_{DVDD\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.1.13.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.31. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD\_LE\_BOD}$	Supply Falling	1.5	—	1.71	V
BOD response time	$t_{DVDD\_LE\_BOD\_DELAY}$	Supply dropping at 2mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	$V_{DVDD\_LE\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.1.13.3 AVDD and VIO BODs

BOD Thresholds for AVDD BOD and BOD for VIO supply or supplies. All energy modes.

Table 4.32. AVDD and VIO BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	—	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	V_{BOD_HYST}		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.1.14 USART SPI Master Timing

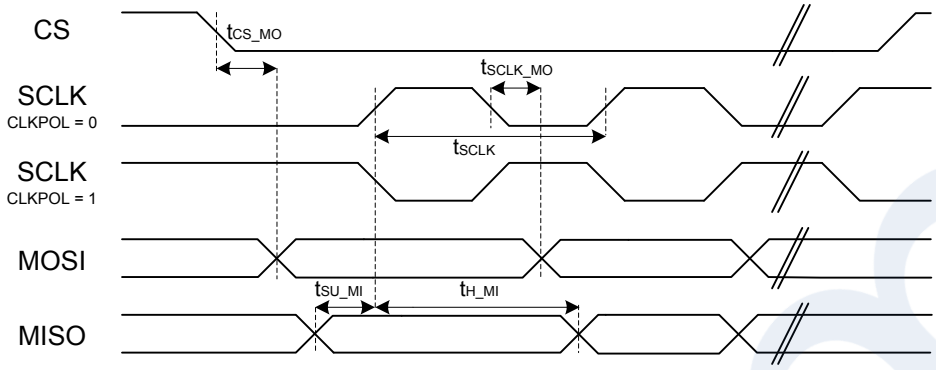

Figure 4.1. SPI Master Timing (SMSDELAY = 0)

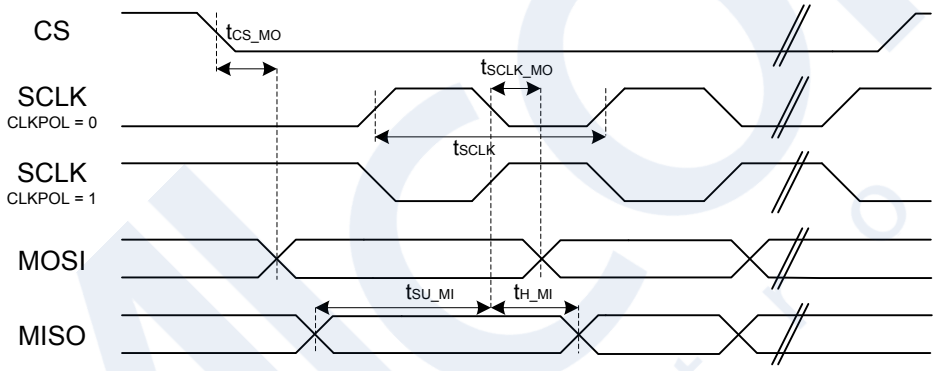

Figure 4.2. SPI Master Timing (SMSDELAY = 1)

4.1.14.1 SPI Master Timing

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.33. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		2*$t_{HFPERCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		-18.5	—	22.5	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		-13	—	11	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.62 V	44	—	—	ns
		IOVDD = 3.0 V	34	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		-8.5	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

4.1.15 USART SPI Slave Timing

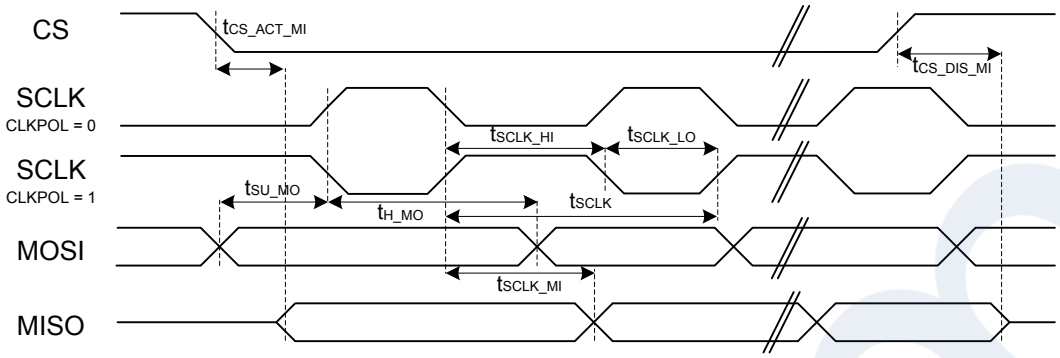

Figure 4.3. SPI Slave Timing

4.1.15.1 SPI Slave Timing

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.34. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		$6*t_{HFPERCLK}$	—	—	ns
SCLK high time[1] [2] [3]	t_{SCLK_HI}		$2.5*t_{HFPERCLK}$	—	—	ns
SCLK low time[1] [2] [3]	t_{SCLK_LO}		$2.5*t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		16	—	52.5	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		15	—	46	ns
MOSI setup time [1] [2]	t_{SU_MO}		3.5	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		4.5	—	—	ns
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		$13.5 + 1.5*t_{HFPERCLK}$	—	$31 + 2.5*t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

4.1.16 I2C Electrical Specifications

4.1.16.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.35. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	µs
STOP condition set-up time	t_{SU_STO}		4.0	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.1.16.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.36. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.1.16.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.37. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.1.17 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The table below provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- SE firmware version 1.2.4
- Gecko Bootloader size 16 KB

Table 4.38. Boot Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Boot time[1]	t_{BOOT}	Secure boot application check disabled, 50 kB application size	—	29.2	—	ms
		Secure boot application check enabled, 50 kB application size	—	38.6	—	ms
		Secure boot application check enabled, 150 kB application size	—	42.6	—	ms
		Secure boot application check enabled, 350 kB application size	—	50.4	—	ms

Note:
1. Secure boot check of second stage bootloader enabled for all measurements.

4.1.18 Crypto Operation Timing for SE Manager API

Values in this table represent timing from SE Manager API call to return. The Cortex-M33 HCLK frequency is 38.4 MHz. The timing specifications below are measured at the SE Manager function call API. Each duration in the table contains some portion that is influenced by SE Manager build compilation and Cortex-M33 operating frequency and some portion that is influenced by the Hardware Secure Engine's firmware version and its operating speed (typically 80 MHz). The contributions of the Cortex-M33 properties to the overall specification timing are most pronounced for the shorter operations such as AES and hash when operating on small payloads. The overhead of command processing at the mailbox interface can also dominate the timing for shorter operations.

Conditions:

- SE firmware version 1.2.4
- GSDK version 3.0.1

Table 4.39. Crypto Operation Timing for SE Manager API

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 timing	t_{AES128}	AES-128 CCM encryption, PT 1 kB	—	265	—	µs
		AES-128 CCM encryption, PT 32 kB	—	1450	—	µs
		AES-128 CTR encryption, PT 1 kB	—	231	—	µs
		AES-128 CTR encryption, PT 32 kB	—	798	—	µs
		AES-128 GCM encryption, PT 1 kB	—	246	—	µs
		AES-128 GCM encryption, PT 32 kB	—	810	—	µs
AES-256 timing	t_{AES256}	AES-256 CCM encryption, PT 1 kB	—	279	—	µs
		AES-256 CCM encryption, PT 32 kB	—	1880	—	µs
		AES-256 CTR encryption, PT 1 kB	—	239	—	µs
		AES-256 CTR encryption, PT 32 kB	—	1010	—	µs
		AES-256 GCM encryption, PT 1 kB	—	255	—	µs
		AES-256 GCM encryption, PT 32 kB	—	1030	—	µs
ECC P-256 timing	t_{ECC_P256}	ECC key generation, P-256	—	5.5	—	ms
		ECC signing, P-256	—	5.7	—	ms
		ECC verification, P-256	—	6.1	—	ms
ECC P-521 timing[1]	t_{ECC_P521}	ECC key generation, P-521	—	29.7	—	ms
		ECC signing, P-521	—	30.8	—	ms
		ECC verification, P-521	—	37.2	—	ms
ECC P-25519 timing[1]	t_{ECC_P25519}	ECC key generation, P-25519	—	4.3	—	ms
		ECC signing, P-25519	—	4.4	—	ms
		ECC verification, P-25519	—	6.0	—	ms
ECDH compute secret timing	t_{ECDH}	ECDH compute secret, P-521[1]	—	29.5	—	ms
		ECDH compute secret, P-25519[1]	—	41.8	—	ms
		ECDH compute secret, P-256	—	5.4	—	ms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE client timing	$t_{ECJPAKE\_C}$	ECJPAKE client write round one	—	21.4	—	ms
		ECJPAKE client read round one	—	14.3	—	ms
		ECJPAKE client write round two	—	16.2	—	ms
		ECJPAKE client read round two	—	7.6	—	ms
		ECJPAKE client derive secret	—	10.5	—	ms
ECJPAKE server timing	$t_{ECJPAKE\_S}$	ECJPAKE server write round one	—	21.4	—	ms
		ECJPAKE server read round one	—	14.3	—	ms
		ECJPAKE server write round two	—	16.3	—	ms
		ECJPAKE server read round two	—	7.6	—	ms
		ECJPAKE server derive secret	—	10.5	—	ms
POLY-1305 timing[1]	$t_{POLY1305}$	POLY-1305, PT 1 kB	—	212	—	µs
		POLY-1305, PT 32 kB	—	1070	—	µs
SHA-256 timing	t_{SHA256}	SHA-256, PT 1 kB	—	251	—	µs
		SHA-256, PT 32 kB	—	677	—	µs
SHA-512 timing[1]	t_{SHA512}	SHA-512, PT 1 kB	—	251	—	µs
		SHA-512, PT 32 kB	—	566	—	µs

Note:
1. Option is only available on OPNs with Secure Vault High feature set.

4.1.19 Crypto Operation Average Current for SE Manager API

Values in this table represent current consumed by security core during the operation, and represent additions to the current consumed by the Cortex-M33 application CPU due to the Hardware Secure Engine CPU and its associated crypto accelerators. The current measurements below represent the average value of the current for the duration of the crypto operation. Instantaneous peak currents may be higher.

Conditions:

- SE firmware version 1.2.4
- GSDK version 3.0.1

Table 4.40. Crypto Operation Average Current for SE Manager API

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 current	I_{AES128}	AES-128 CCM encryption, PT 1 kB	—	5.0	—	mA
		AES-128 CCM encryption, PT 32 kB	—	8.8	—	mA
		AES-128 CTR encryption, PT 1 kB	—	4.5	—	mA
		AES-128 CTR encryption, PT 32 kB	—	8.8	—	mA
		AES-128 GCM encryption, PT 1 kB	—	4.7	—	mA
		AES-128 GCM encryption, PT 32 kB	—	9.0	—	mA
AES-256 current	I_{AES256}	AES-256 CCM encryption, PT 1 kB	—	5.2	—	mA
		AES-256 CCM encryption, PT 32 kB	—	8.8	—	mA
		AES-256 CTR encryption, PT 1 kB	—	4.7	—	mA
		AES-256 CTR encryption, PT 32 kB	—	8.8	—	mA
		AES-256 GCM encryption, PT 1 kB	—	4.8	—	mA
		AES-256 GCM encryption, PT 32 kB	—	9.0	—	mA
ECC P-256 current	$I_{ECCP256}$	ECC key generation, P-256	—	6.6	—	mA
		ECC signing, P-256	—	6.6	—	mA
		ECC verification, P-256	—	6.5	—	mA
ECC P-521 current[1]	$I_{ECCP521}$	ECC key generation, P-521	—	6.7	—	mA
		ECC signing, P-521	—	6.7	—	mA
		ECC verification, P-521	—	6.7	—	mA
ECC P-25519 current[1]	$I_{ECCP25519}$	ECC key generation, P-25519	—	6.5	—	mA
		ECC signing, P-25519	—	6.5	—	mA
		ECC verification, P-25519	—	6.5	—	mA
ECDH compute secret current	I_{ECDH}	ECDH compute secret, P-521[1]	—	6.7	—	mA
		ECDH compute secret, P-25519[1]	—	6.4	—	mA
		ECDH compute secret, P-256	—	6.5	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE client current	$I_{ECJPAKE\_C}$	ECJPAKE client write round one	—	6.7	—	mA
		ECJPAKE client read round one	—	6.6	—	mA
		ECJPAKE client write round two	—	6.6	—	mA
		ECJPAKE client read round two	—	6.5	—	mA
		ECJPAKE client derive secret	—	6.6	—	mA
ECJPAKE server current	$I_{ECJPAKE\_S}$	ECJPAKE server write round one	—	6.6	—	mA
		ECJPAKE server read round one	—	6.6	—	mA
		ECJPAKE server write round two	—	6.6	—	mA
		ECJPAKE server read round two	—	6.5	—	mA
		ECJPAKE server derive secret	—	6.5	—	mA
POLY-1305 current[1]	$I_{POLY1305}$	POLY-1305, PT 1 kB	—	4.4	—	mA
		POLY-1305, PT 32 kB	—	6.4	—	mA
SHA-256 current	I_{SHA256}	SHA-256, PT 1 kB	—	3.4	—	mA
		SHA-256, PT 32 kB	—	6.6	—	mA
SHA-512 current[1]	I_{SHA512}	SHA-512, PT 1 kB	—	3.4	—	mA
		SHA-512, PT 32 kB	—	6.1	—	mA

Note:
1. Option is only available on OPNs with Secure Vault High feature set.

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

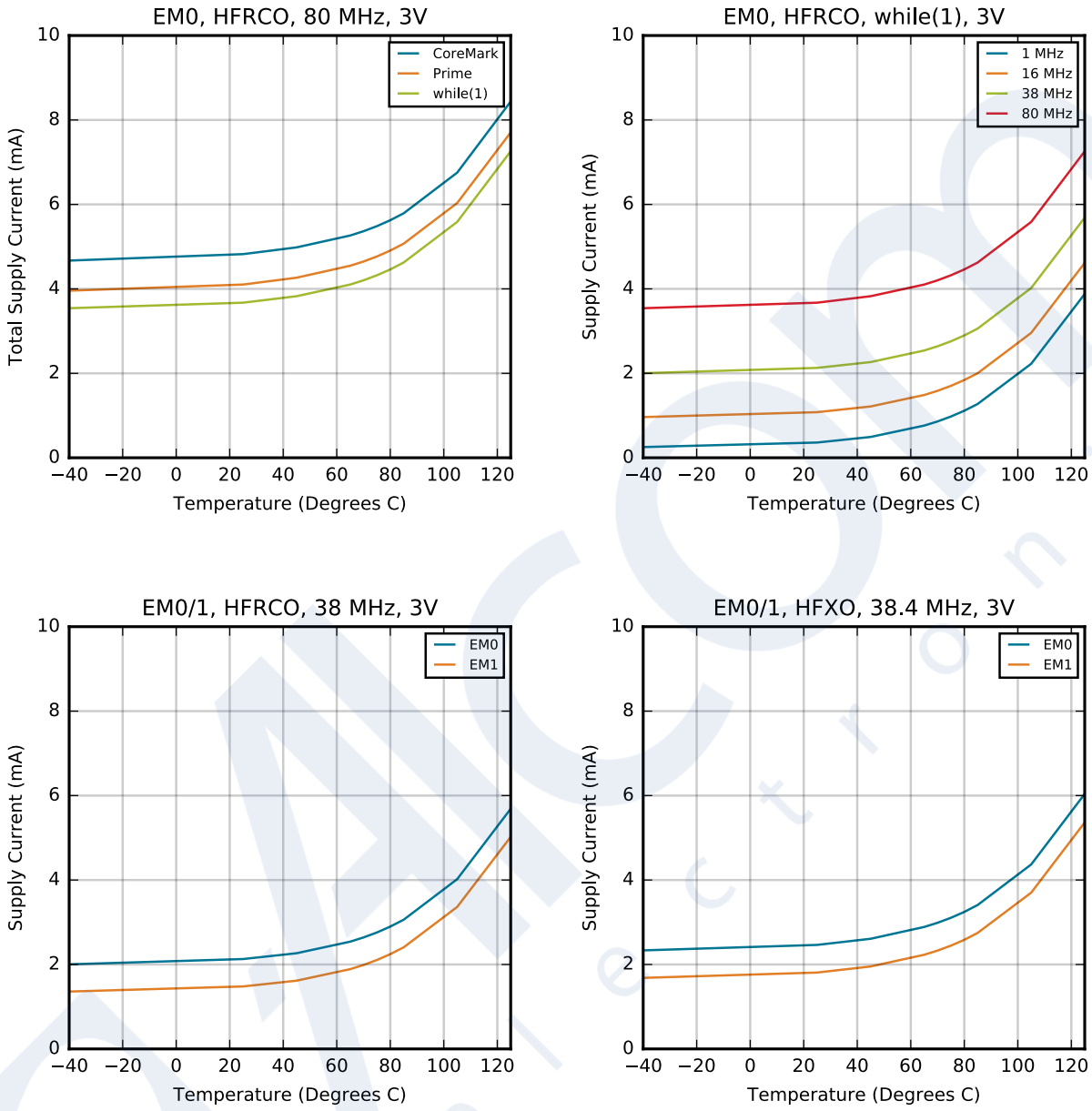

Figure 4.4. EM0 Active Mode Typical Supply Current vs. Temperature

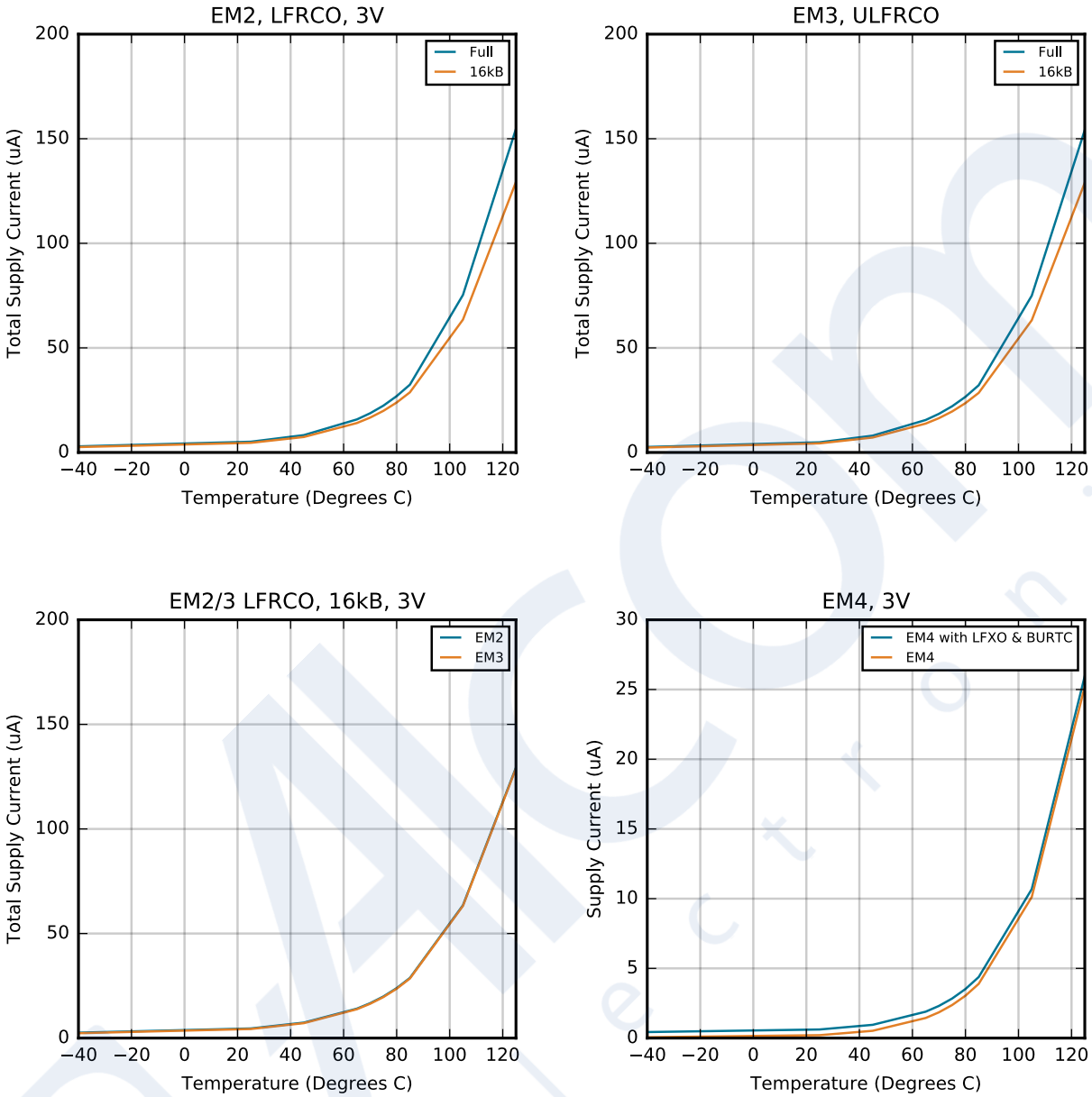

Figure 4.5. EM2, EM3, and EM4 Sleep Mode Typical Supply Current vs. Temperature

4.2.2 2.4 GHz Radio

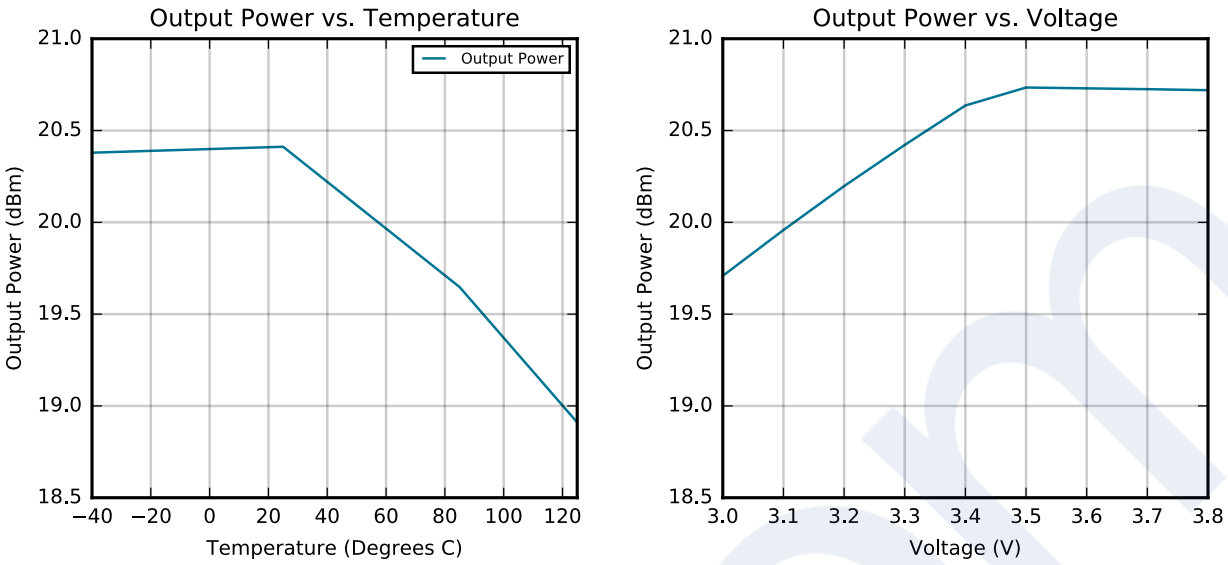

Figure 4.6. 2.4 GHz 20 dBm PA RF Transmitter Output Power

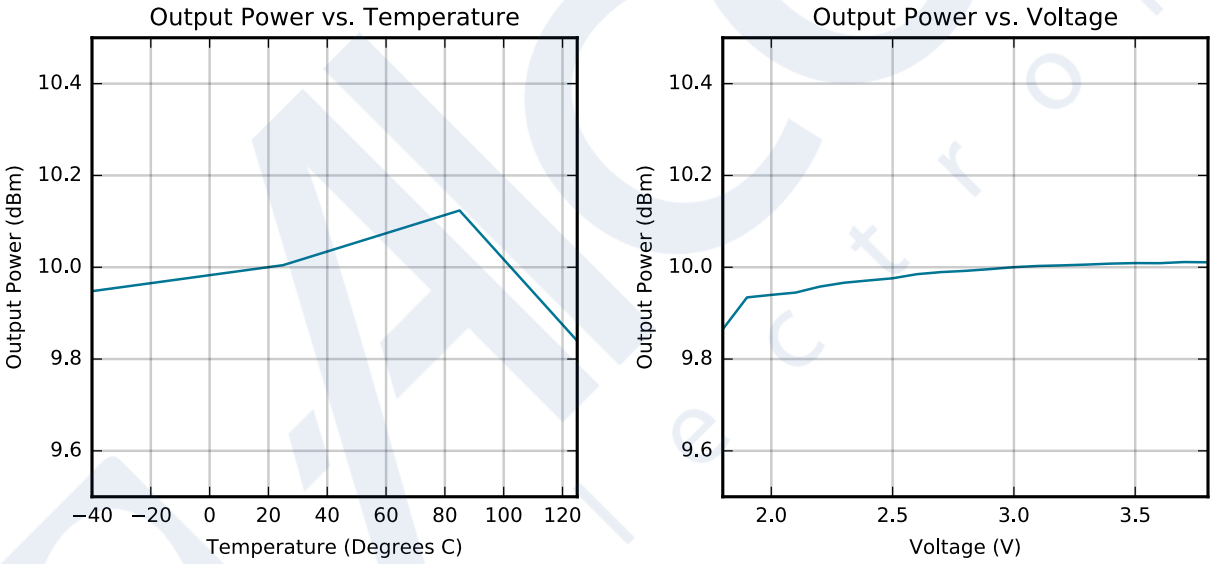

Figure 4.7. 2.4 GHz 10 dBm PA RF Transmitter Output Power

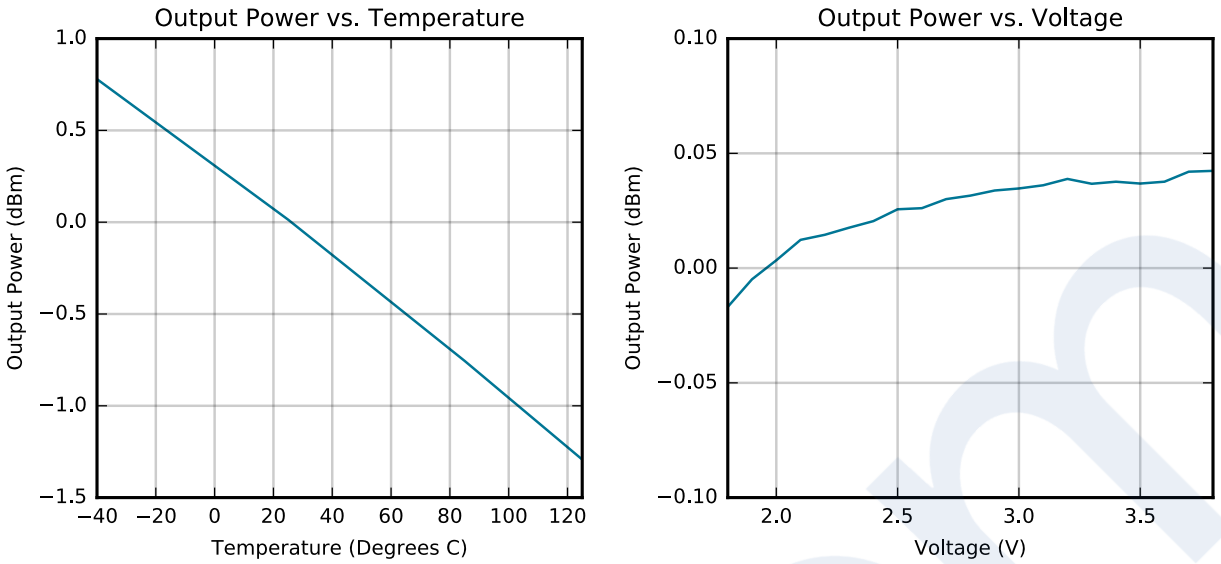

Figure 4.8. 2.4 GHz 0 dBm PA RF Transmitter Output Power

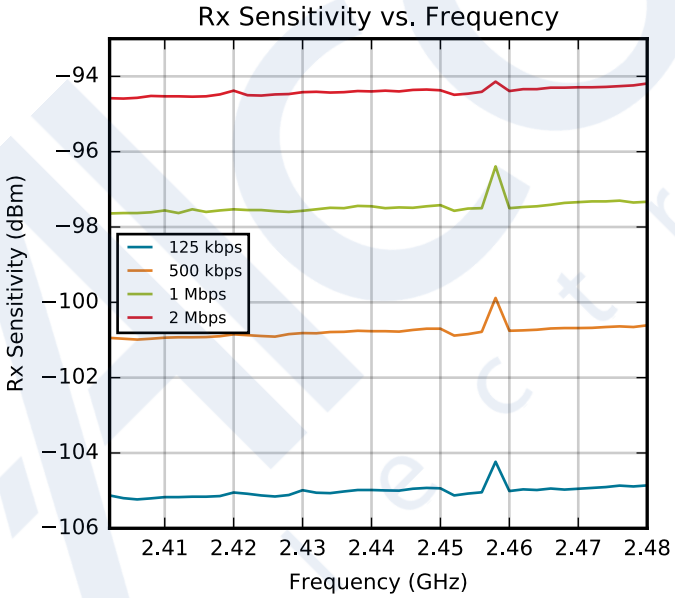

Figure 4.9. 2.4 GHz BLE RF Receiver Sensitivity

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections are shown in the following figure.

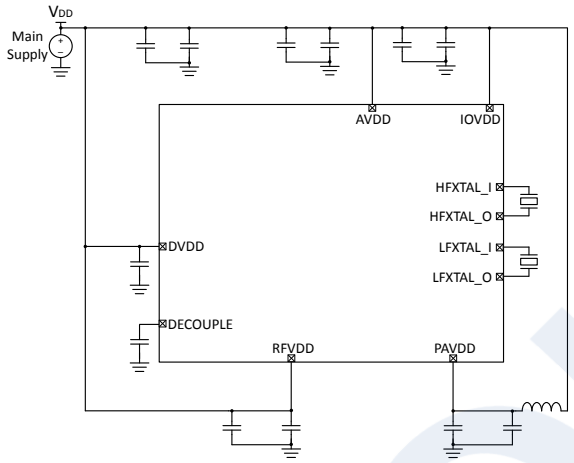

Figure 5.1. EFR32BG21B Typical Application Circuit: Direct Supply Configuration

5.2 RF Matching Networks

RF Matching Network connections are described in the following sub-sections. For more information on matching networks and recommendations, see AN930.2: EFR32 Series 2 2.4 GHz Matching Guide and AN928.2: EFR32 Series 2 Layout Design Guide. Application Notes can be accessed on the Silicon Labs website (www.silabs.com).

5.2.1 2.4 GHz 0 dBm Matching Network

The recommended RF matching network circuit diagram for 2.4GHz applications with a transmit power of 0 dBm or less is shown in Figure 5.2 Typical 0 dBm 2.4 GHz RF impedance-matching network circuit on page 68. Typical component values are shown in Table 5.1 2.4GHz 0 dBm Component Values on page 68. Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

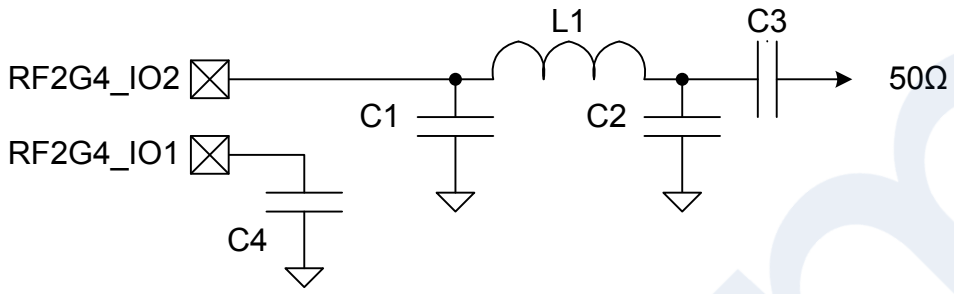

Figure 5.2. Typical 0 dBm 2.4 GHz RF impedance-matching network circuit

Table 5.1. 2.4GHz 0 dBm Component Values

Designator	Value
C1	1.7 pF
C2	0.9 pF
L1	2.0 nH
C3	2.7 pF
C4	0.5 pF

5.2.2 2.4 GHz 10 dBm Matching Network

The recommended RF matching network circuit diagram for 2.4GHz applications with a transmit power of greater than 0 dBm and up to 10 dBm is shown in Figure 5.3 Typical 10 dBm 2.4 GHz RF impedance-matching network circuit on page 69. Typical component values are shown in Table 5.2 2.4GHz 10 dBm Component Values on page 69. Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

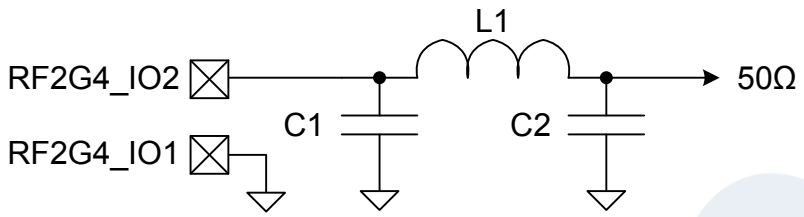

Figure 5.3. Typical 10 dBm 2.4 GHz RF impedance-matching network circuit

Table 5.2. 2.4GHz 10 dBm Component Values

Designator	Value
C1	1.9 pF
L1	2.1 nH
C2	0.9 pF

5.2.3 2.4 GHz 20 dBm Matching Network

For part numbers which support the high-power 20 dBm PA, the recommended RF matching network circuit diagram for 2.4GHz applications with a transmit power of greater than 10 and up to 20 dBm is shown in Figure 5.4 Typical 20 dBm 2.4 GHz RF impedance-matching network circuit on page 69. Typical component values are shown in Table 5.3 2.4GHz 20 dBm Component Values on page 69. Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

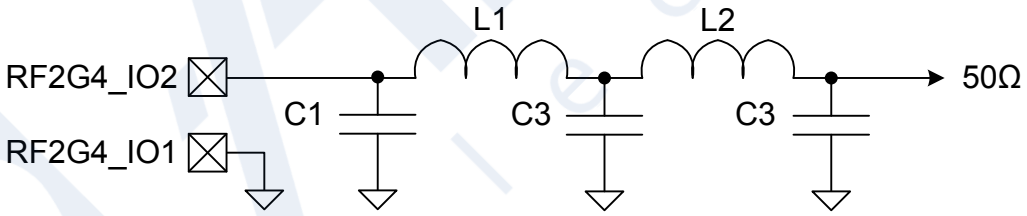

Figure 5.4. Typical 20 dBm 2.4 GHz RF impedance-matching network circuit

Table 5.3. 2.4GHz 20 dBm Component Values

Designator	Value
C1	2.3 pF
L1	2.3 nH
C2	0.8 pF
L2	1.1 nH
C3	0.3 pF

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN32 2.4GHz Device Pinout

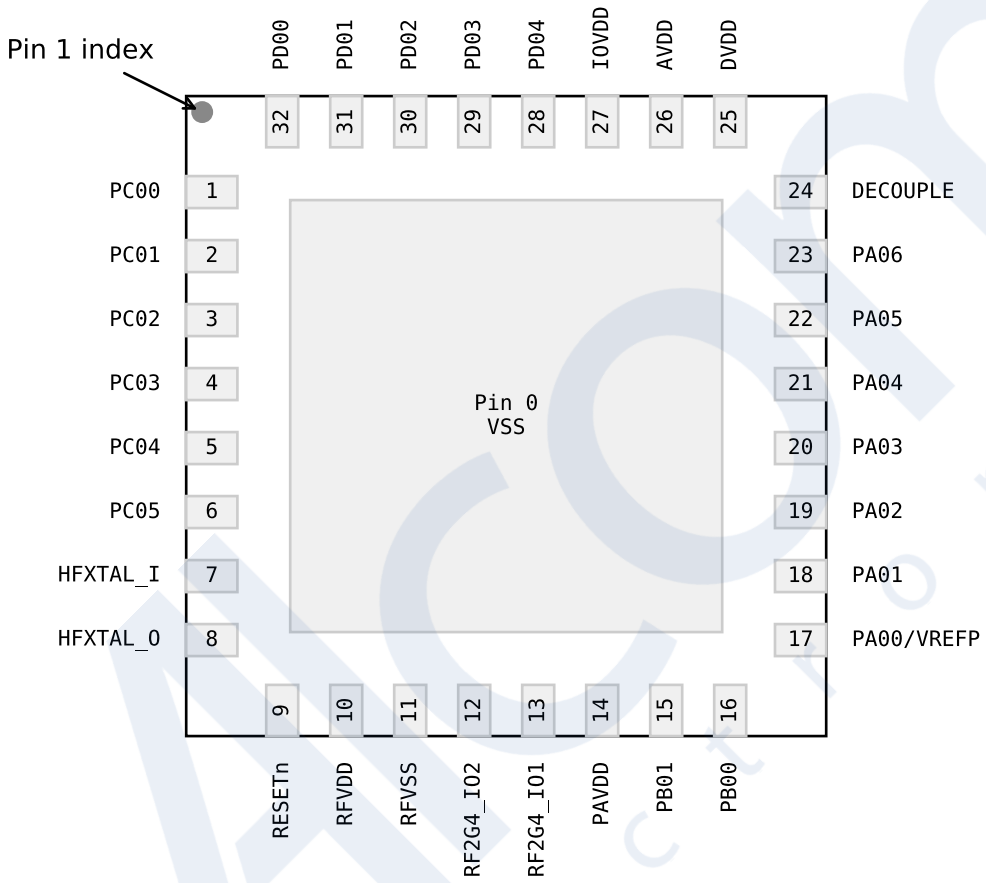

Figure 6.1. QFN32 2.4GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.2 Alternate Function Table, 6.3 Analog Peripheral Connectivity, and 6.4 Digital Peripheral Connectivity.

Table 6.1. QFN32 2.4GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output
RESETn	9	Reset Pin	RFVDD	10	Radio power supply

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RFVSS	11	Radio Ground	RF2G4_IO2	12	2.4 GHz RF input/output
RF2G4_IO1	13	2.4 GHz RF input/output	PAVDD	14	Power Amplifier (PA) power supply
PB01	15	GPIO	PB00	16	GPIO
PA00	17	GPIO	PA01	18	GPIO
PA02	19	GPIO	PA03	20	GPIO
PA04	21	GPIO	PA05	22	GPIO
PA06	23	GPIO	DECOUPLE	24	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
DVDD	25	Digital power supply	AVDD	26	Analog power supply
IOVDD	27	Digital IO power supply.	PD04	28	GPIO
PD03	29	GPIO	PD02	30	GPIO
PD01	31	GPIO	PD00	32	GPIO

6.2 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows what functions are available on each device pin.

Table 6.2. GPIO Alternate Function Table

GPIO	Alternate Functions			
PC00	GPIO.EM4WU6			
PC05	GPIO.EM4WU7			
PB01	GPIO.EM4WU3			
PA00		IADC0.VREFP		
PA01	GPIO.SWCLK			
PA02	GPIO.SWDIO			
PA03	GPIO.SWV GPIO.TDO GPIO.TRACEDATA0			
PA04	GPIO.TDI GPIO.TRACECLK			
PA05	GPIO.EM4WU0			
PD02	GPIO.EM4WU9			
PD01		LFXO.LFXTAL_I LFXO.LF_EXTCLK		
PD00		LFXO.LFXTAL_O		

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is avaliable on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals.

Table 6.3. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are avaliable on each GPIO port.

Table 6.4. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.ASYNCH11			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		

Peripheral.Resource	PORT			
	PA	PB	PC	PD
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		
USART2.CLK			Available	Available
USART2.CS			Available	Available
USART2.CTS			Available	Available
USART2.RTS			Available	Available
USART2.RX			Available	Available
USART2.TX			Available	Available

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

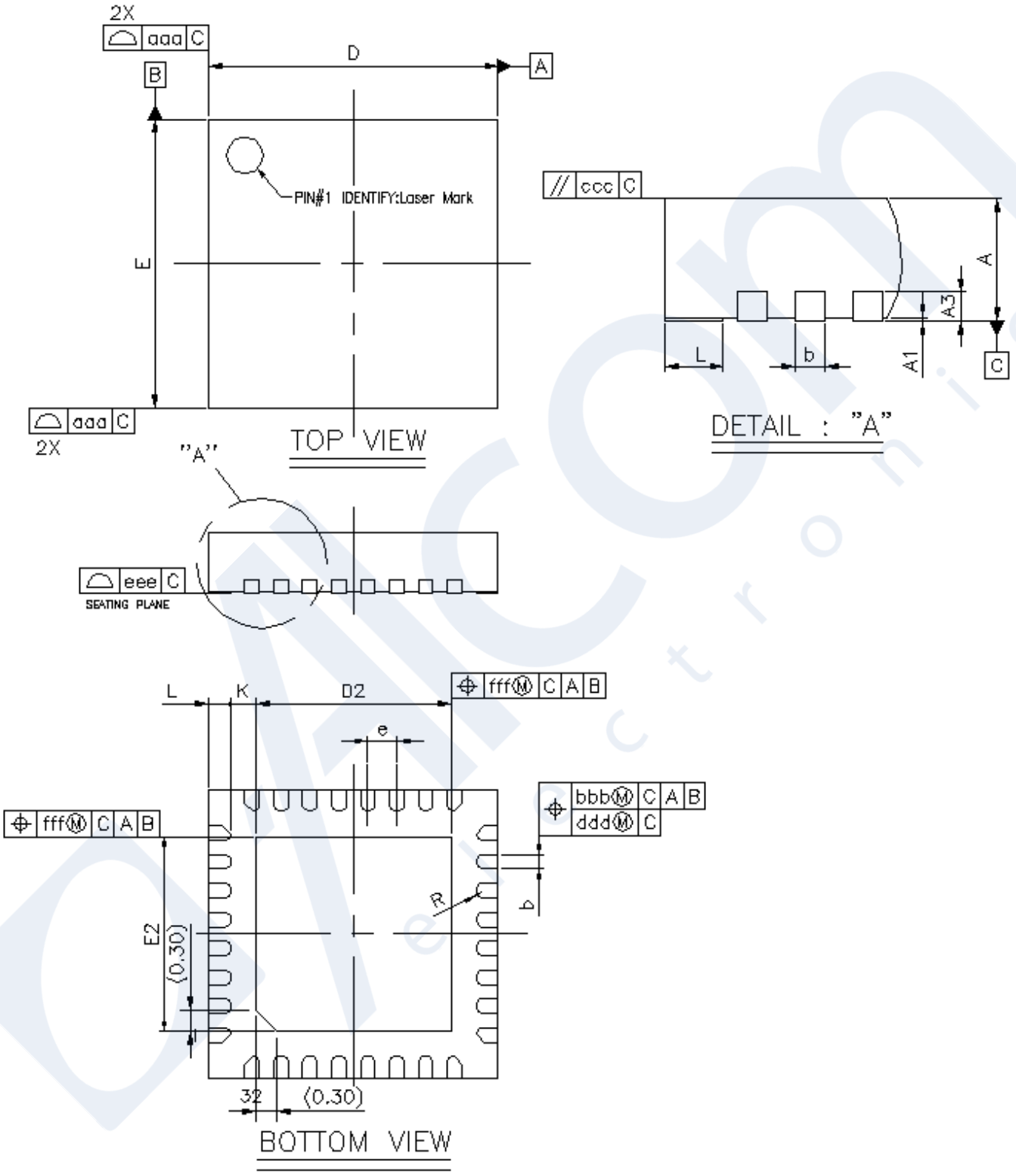

Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.20	0.30	0.40
K	0.20	—	—
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

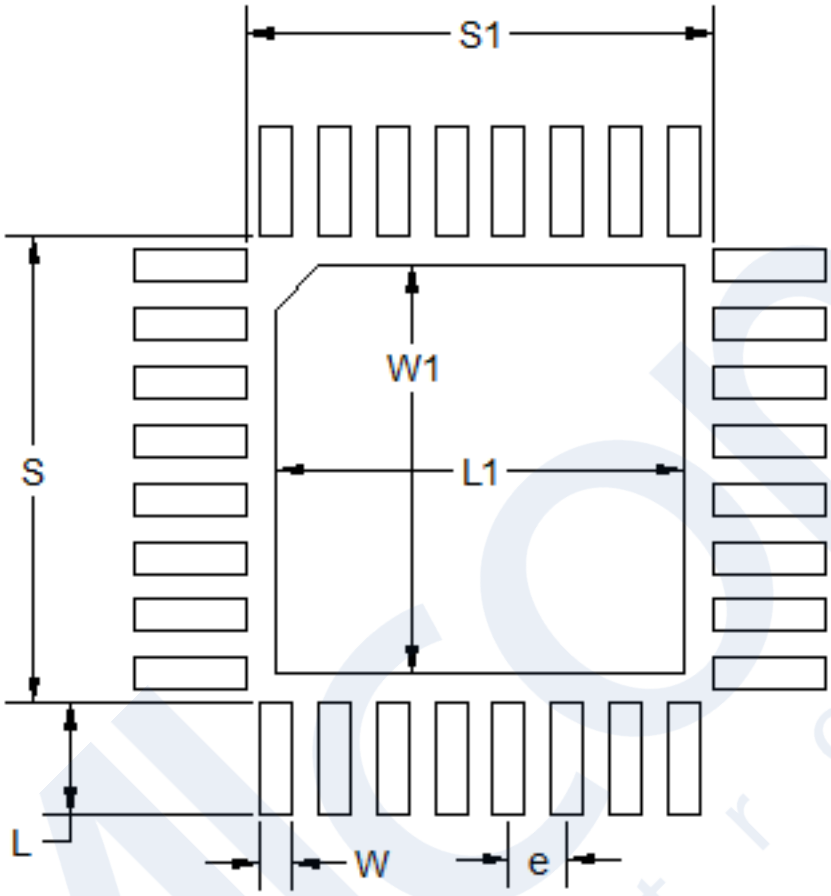

Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
L	0.76
W	0.22
e	0.40
S	3.21
S1	3.21
L1	2.80
W1	2.80

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.101 mm (4 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

7.3 QFN32 Package Marking

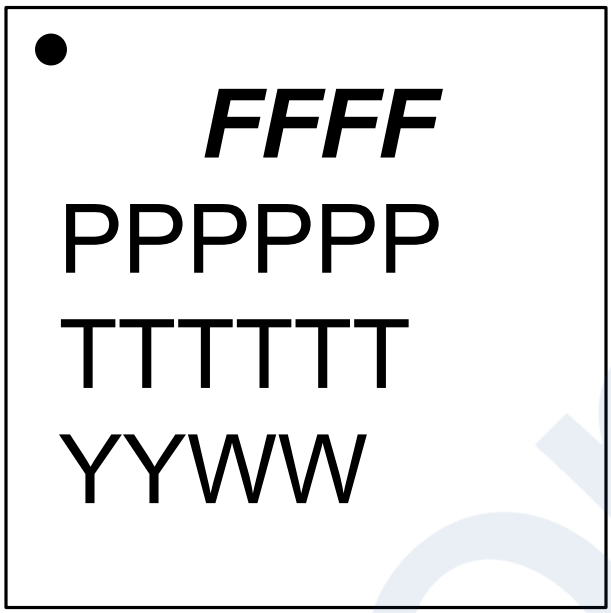

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- FFFF – The product family codes.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Series (2)
  4. Device Configuration (1, 2, 3, ...)
- PPPPPP – The product option codes.
  - 1-2. MCU Feature Codes
  - 3-4. Radio Feature Codes
  - 5. Flash (J = 1024k | I = 768k | H = 512k | W= 352k | G = 256k | F = 128k)
  - 6. Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. Revision History

Revision 1.0

April, 2021

- Changed number of 16-bit Timer/Counter modules to 3 in 1. Feature List.
- Added TIMER3 to Table 3.1 Configuration Summary on page 15.
- Added sections 4.1.17 Boot Timing, 4.1.18 Crypto Operation Timing for SE Manager API, and 4.1.19 Crypto Operation Average Current for SE Manager API.
- Updated Secure Vault terminology throughout the document.

Revision 0.5

June, 2020

- Initial Release.
- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated 3.5.2 Low Energy Timer (LETIMER) lowest energy mode.
- Fixed minor typos throughout the document.
- Added Secure Vault supporting information:
  - Updated feature list in 3.7.2 Cryptographic Accelerator and in the Secure Vault section of 1. Feature List.
  - Added 3.7.5 DPA Countermeasures.
  - Added 3.7.6 Secure Key Management with PUF.
  - Added 3.7.7 Anti-Tamper.
  - Added 3.7.8 Secure Attestation.
- Added reference to J-PAKE and PBKDF2 support to 3.7.2 Cryptographic Accelerator.
- Added references to matching guide and layout design guide appnotes in 5.2 RF Matching Networks.