GWU2X

Datasheet

UG1000-1.0E, 6/29/2021

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Revision History

Date	Version	Description
6/29/2021	1.0E	Initial version published.

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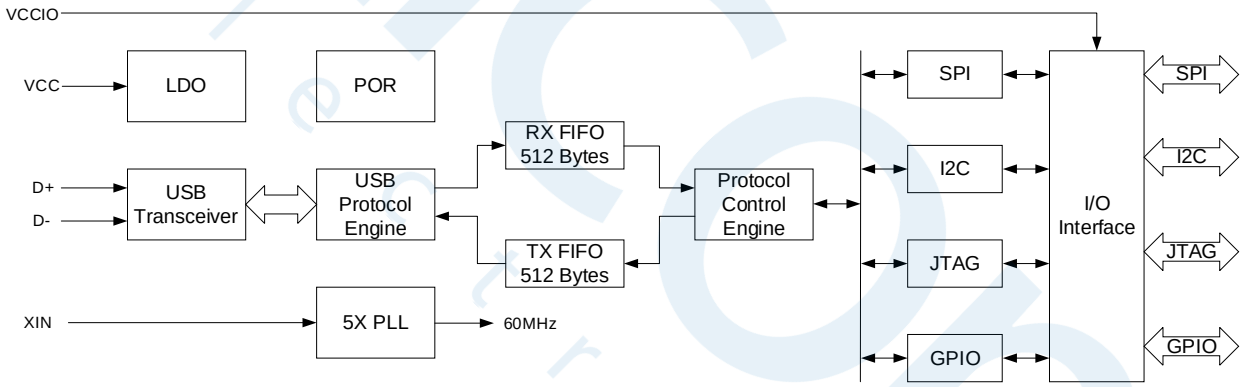
1 Function

1.1 Overview

GWU2X is the first interface bridge ASSP chip in the Gowin Gobridge family. It is a highly integrated, low-power, and single-chip solution for communicating with peripheral interfaces over USB. It is designed to bridge SPI, I2C, JTAG, and GPIO. The structure view is as shown in Figure 1-1.

Figure 1-1 GWU2X Structure View



1.2 Features

- Supports full-speed USB device interface, compatible with the USB v1.1 specification.
- Built-in USB protocol processing, without device firmware programming.
- Supports USB to JTAG/ SPI/ I^2C.
- Independent I/O power supply, supports multiple level standards.
- 16 general-purpose input and output pins.
- Supports I2C, SPI and JTAG host interfaces with adjustable clock and independent data receive buffer.

- API provided for host device usage.

1.3 Typical Applications

- USB products field upgrading
- USB Industry control
- USB Flash Card Reader
- USB-based instruments
- USB-SPI Bus Interface
- USB JTAG Programmer

1.4 Driver Supported

GWU2X supports the WinUSB drivers as below:

- Windows XP 64 bits
- Windows 7/ Windows 10 32 bits,64 bits

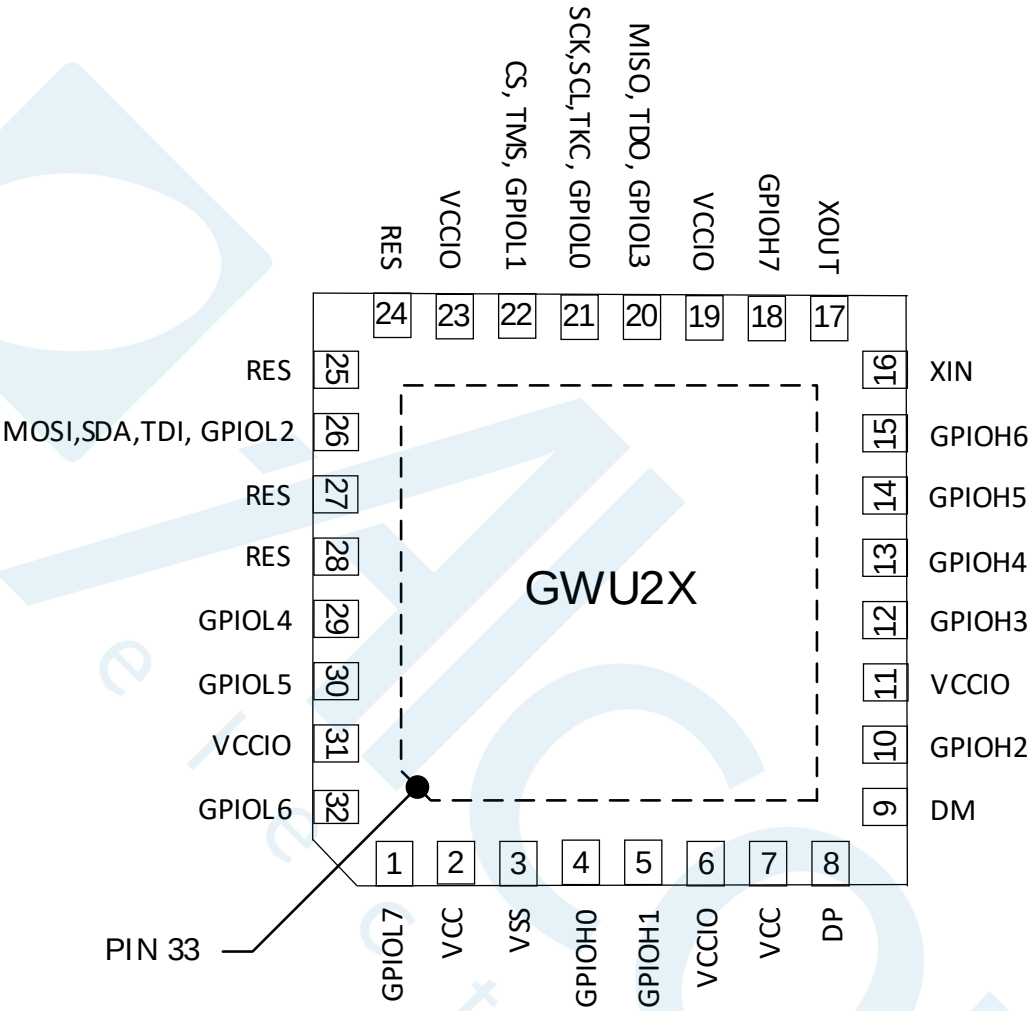
2 Package

GWU2X package information is described in Table 2-1 as below.

Table 2-1 Product Package Resources

Package	Pitch (mm)	Size (mm)
QN32	0.5	5 x 5

2.1 QN32 Pin Description

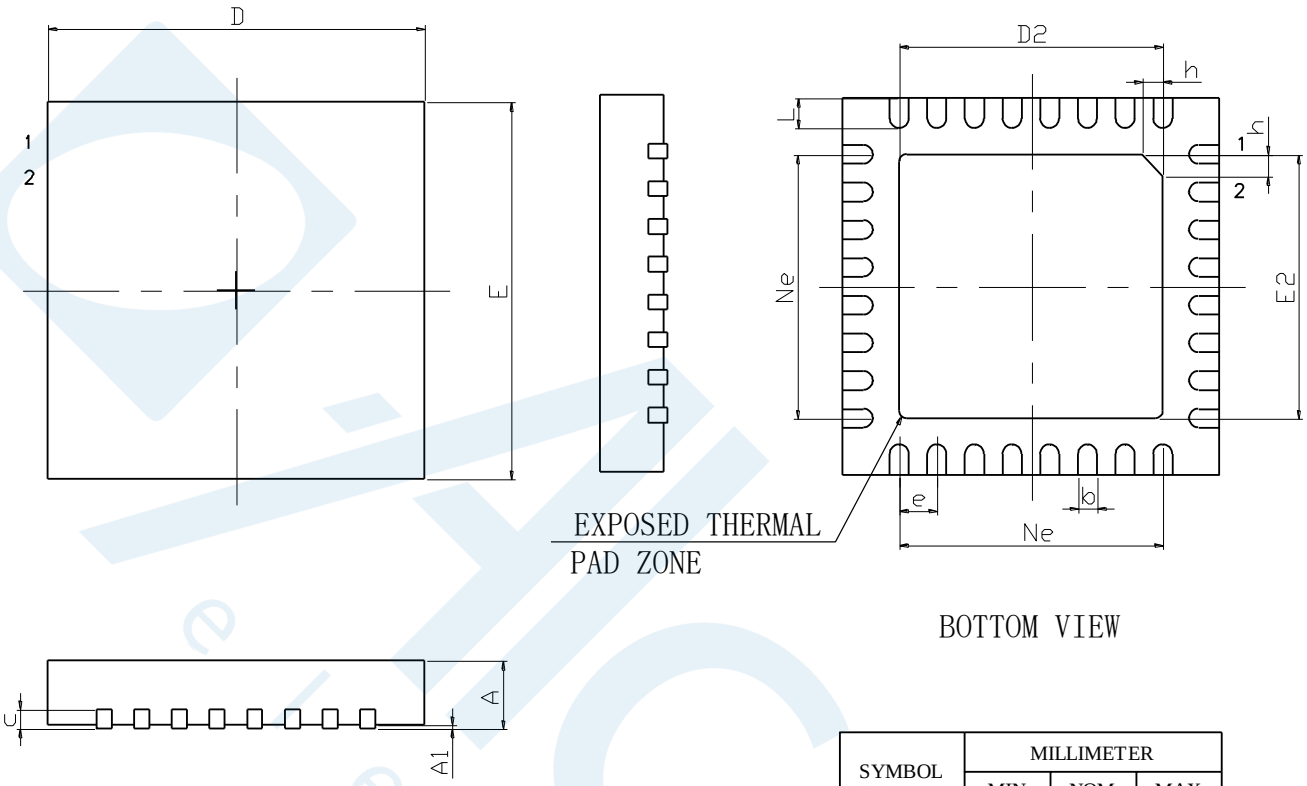


Pin Number	Pin Name	Type	Description
2，7，	VCC	Power Supply	Power Input
6，11，19，23，31	VCCIO	Power Supply	Input/Output pin voltage
3，33	VSS	Power Ground	Common Ground
16	XIN	Clock	Input of crystal oscillation, external crystal and oscillator capacitor
17	XOUT	Clock	Reverse output of crystal oscillation, external crystal and oscillator capacitor
8	DP	Two-Way	USB Data signal D+; 1.5K pull-up resistor needs to be

Pin Number	Pin Name	Type	Description
			connected
9	DM	Bidirectional	USB data signal D-
21	SCK	Output	SPI serial clock output
	SCL	Output	I^2C serial clock output
	TCK	Output	JTAG serial clock output
	GPIOL0	Two-Way	Bidirectional port L0
22	CS	Output	SPI slave selection
	TMS	Output	JTAG test mode selection
	GPIOL1	Two-Way	Bidirectional port L1
26	MOSI	Output	SPI main device data transmission.
	SDA	Two-Way	I2C serial data
	TDI	Output	JTAG main device test data output
	GPIOL2	Two-Way	Bidirectional port L2
20	MISO	Input	SPI main device data reception
	TDO	Input	JTAG main device test data reception
	GPIOL3	Two-Way	Bidirectional port L3
29	GPIOL4	Two-Way	Bidirectional port L4
30	GPIOL5	Two-Way	Bidirectional port L5
32	GPIOL6	Two-Way	Bidirectional port L6
1	GPIOL7	Two-Way	Bidirectional port L7
4	GPIOH0	Two-Way	Bidirectional port H0
5	GPIOH1	Two-Way	Bidirectional port H1
10	GPIOH2	Two-Way	Bidirectional port H2
12	GPIOH3	Two-Way	Bidirectional port H3
13	GPIOH4	Two-Way	Bidirectional port H4
14	GPIOH5	Two-Way	Bidirectional port H5
15	GPIOH6	Two-Way	Bidirectional port H6
18	GPIOH7	Two-Way	Bidirectional port H7
24，25，27，28	RES		Reserved port. Need to be left floating

2.2 QN32 Package Outline

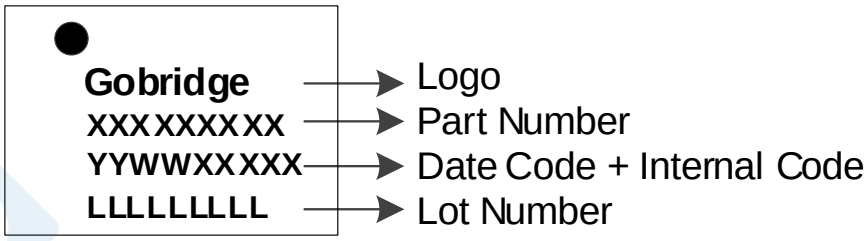
Figure 2-1 QN32 Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

2.3 Package Marking

Figure 2-2 Package Mark Meaning



3 Function Description

3.1 Hardware Description

- Both VCC and VCCIO need to be provided for the GWU2X chip to work normally. It is suggested to connect a power decoupling capacitor with a capacity of 0.01uF ~ 0.1uF to the power pin of each chip. The synchronous serial interface voltage can be adjusted dynamically through VCCIO, with the range of 2.5V~3.4V.
- 12MHz clock signal to the XIN pin provided by an external active crystal oscillator is required for the GWU2X chip to work normally. In general, the clock signal is generated by the built-in inverter in GWU2X through the crystal oscillator with stable frequency.The peripheral circuit only needs to connect a 12MHz crystal between the XIN and XOUT pins and connect oscillating capacitors to the ground for the XIN and XOUT pins respectively.
- GWU2X chip has built-in power on reset circuit, and no external reset is required.
- The USB port of GWU2X chip has no built-in pull-up resistor, and additional 1.5K pull-up resistor needs to be provided at the DP end. It is recommended to connect the insurance resistor or inductor or ESD protection device in series for safety, and the AC-DC equivalent series resistance should be within 5Ω.
- Some pins of GWU2X chip have multiple functions, so they have different characteristics during the chip reset and in the normal working state after reset. All pins with a tri-state output have a built-in pull-up resistor. This knid of pin acts as an output pin after the chip is reset and runs the firmware. During the chip reset, tri-state output is prohibited and the built-in pull-up resistor provides the pull-up current. If necessary, the external circuit can provide an external pull-up resistor or pull-down

resistor to set the relevant pin's default level during the reset of the GWU2X chip. The resistance value of the external pull-up resistor or pull-down resistor is usually between 2KΩ and 5KΩ.

3.2 GPIO Interface

GWU2X provides 16 GPIO pins, all of which can be independently configured as output or input.

3.3 Synchronous Serial Interface

GWU2X synchronous serial port is an active serial port, which can only be used as Host/Master. Its internal Protocol Engine Control module and the external computer driver can be applied to implement I2C serial port, SPI serial port and JTAG serial port.

3.3.1 I²C

The main pins of I^2C serial port include SCL pin and SDA pin. SCL is used for one-way output synchronous clock, open leak output and built-in pull up resistance. SDA is used for quasi-two-way data input and output, open leak output and input, and built-in pull up resistance.

The basic elements of I^2C serial timing include: start bit, stop bit, bit output, bit input, byte output, and byte input.

3.3.2 SPI

The main pins of SPI serial port include SCK pin, MISO pin, MOSI pin, and the chip selection pin of CS. SCK is used for one-way output synchronous clock, MISO is used for one-way input data, MOSI is used for one-way output data, and the chip selector pin of CS is used for device selection.

3.3.3 JTAG

The main pins of JTAG serial port include TMS pin, TDI pin, and TDO pin. TMS is used for mode selection, TCK is used for output synchronous clock, TDI is used for output test data, and TDO is used for input test data.

The timing sequence of JTAG serial port follows IEEE1149.1 protocol, allowing data changes on TMS, TDI and TDO signals when TCK signal falls from high to low. At the time of TCK rising edge, the data on TMS, TDI and TDO signals will remain unchanged, so as to facilitate sampling of TMS, TDI

and TDO signals with the rising edge of TCK signals

4 Driver

For the detailed information, please refer to:

- UG1002-1.0_GWU2X Programming Guide_U2X_IIC,
- UG1003-1.0_GWU2X Programming Guide_U2X_JTAG
- UG1004-1.0_GWU2X Programming Guide_ U2X_SPI.

5 Devices Characteristics and Ratings

5.1 Absolute Max. Ratings

Table 5-1 Absolute Max. Ratings

Parameter	Description	Min.	Max.	Unit
TA	Ambient temperature during work	-40	85	℃
TS	Ambient temperature during storage	-65	150	℃
VCC	Power voltage	-0.5	3.75	V
VCCIO	Input/Output pin voltage	-0.5	3.75	V

5.2 Electrical Characteristics

Table 5-2 Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power voltage	3	3.3	3.6	V
VCCIO	Input/Output pin voltage	2.5	-	3.4	V
Icc1	Total power supply current during operation	-	35	-	mA
VIL	Low-level input voltage	-0.3	-	0.35*VCCO	V
VIH	High-level input voltage	0.65*VCCO	-	3.6	V
VOL	Low-level output	-	-	0.4	V

Parameter	Description	Min.	Typ.	Max.	Unit
	voltage (Drive current = 8mA)				
VOH	High-level output voltage (Drive current = 6mA)	VCCO-0.4	–	–	V
UVOL	Low-level output voltage of USB		–	0.4	V
UVOH	High-level output voltage of USB	2.8	–	–	V
UVse	Single-ended receiving threshold	0.8	–	2.0	V

5.3 Timing Parameters

Table 5-3 Timing Parameters

Parameter	Description	Min.	Typ.	Max.	Unit
FCLK	The Input clock signal frequency of the XIN pin	-	12	-	MHz
TPR	Reset time of power on	-	5	-	ms

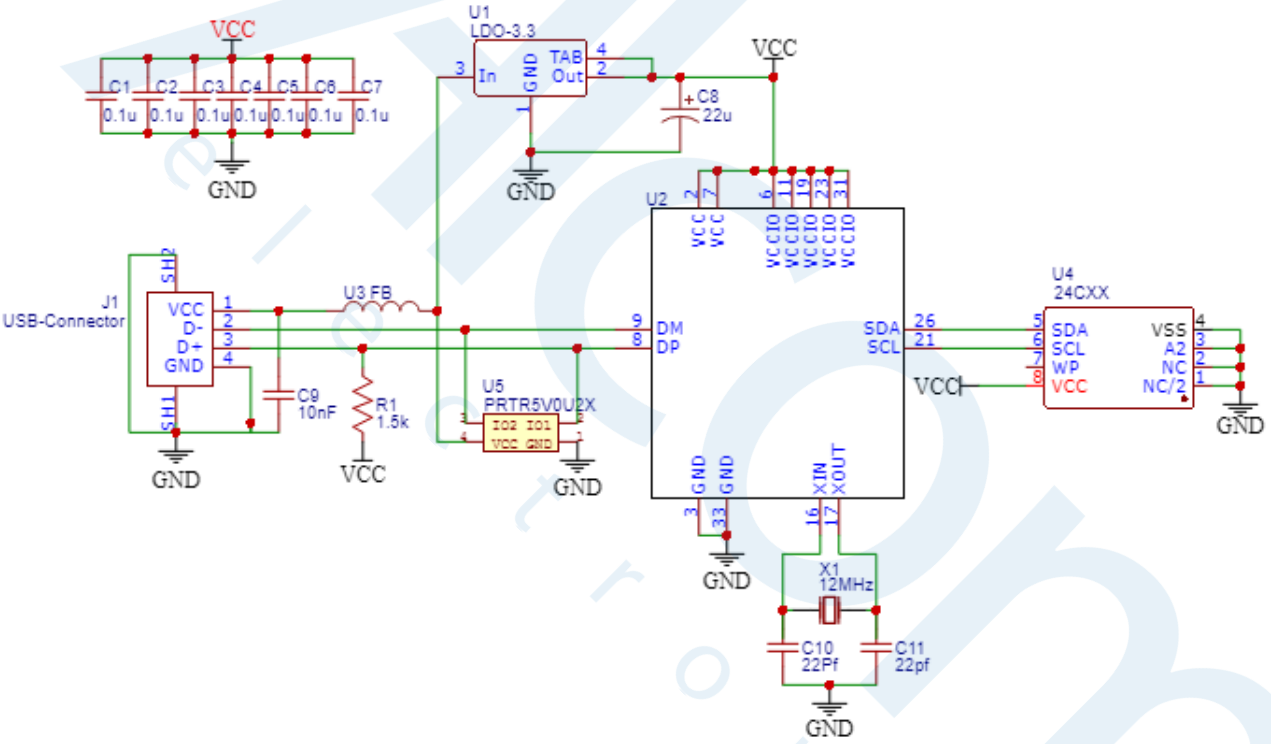
5.4 ESD Parameters

Table 5-4 ESD Paramrters

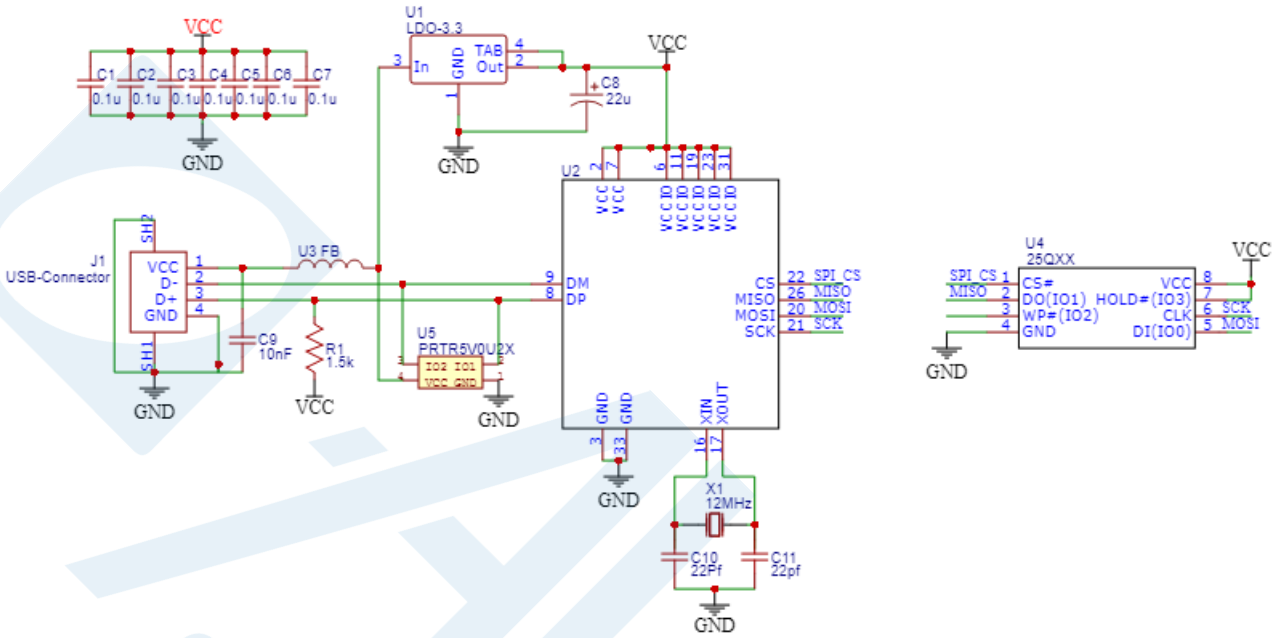
Parameter	Description	Min.	Typ.	Max.	Unit
HBM	Human Body Model	1000	-	-	V
CDM	Charged Device Model	500	-	-	V

6 Typical Applications

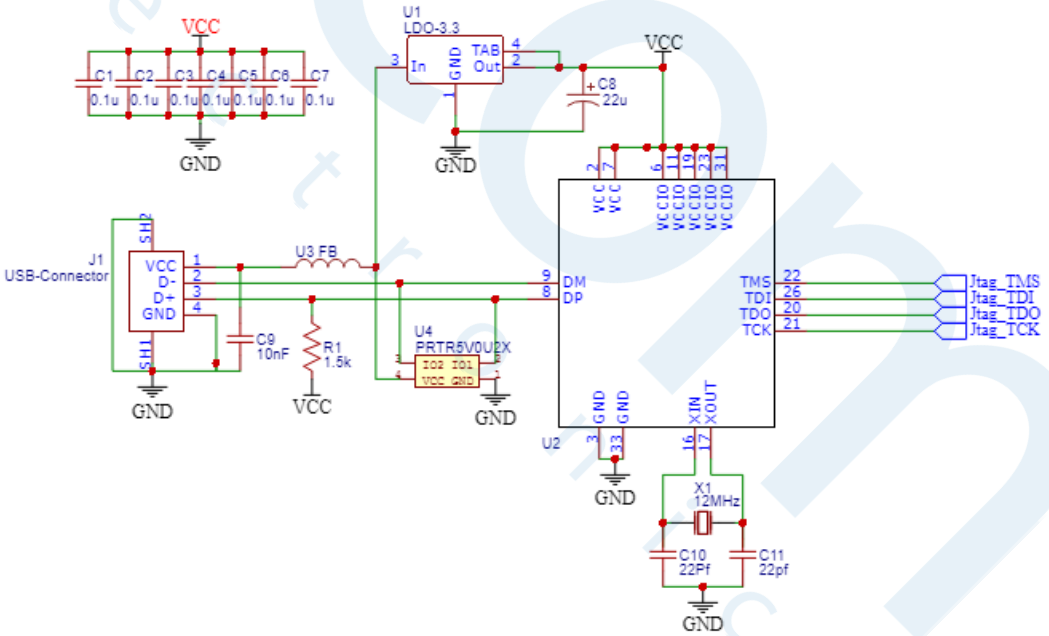
6.1 I²C Application



6.2 SPI Application



6.3 JTAG Application



Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in .

Table A -1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ASSP	Application Specific Standard Product
JTAG	Joint Test Action Group
I^2C	Inter-Integrated Circuit
SPI	Serial Peripheral Interface
GPIO	Gowin Programmable I/O
QN	Quad Flat No-lead Package
ESD	Electronic Static Discharge

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