A New Approach: Single-Chip Control of Multiple High-Performance Servo Motors

The microcontroller is a remarkable workhorse of embedded electronics, the closest that design engineers have to a 'do everything' component. There are limits, however, even to the range of functions that an MCU can address: motor control is one of those applications which stretches the capabilities even of high-end MCUs.

This is an inherent feature of the MCU, which executes threaded instructions in sequence; motor control calls for deterministic control of both motor position/speed and motor current in real-time. As a result, a low-end MCU alone can generally only control a single servo motor.

For applications calling for the control of multiple servo motors, an FPGA can provide a more appropriate hardware environment because of its ability to execute two or more time-critical functions concurrently in parallel.

The commercial options on the FPGA market, however, have in the past put the designer in a dilemma: when implementing a demanding motor system design, OEMs have a strong preference for a single-chip solution, but the kind of FPGA which can run position, speed, and current control routines concurrently is at the high-density end of the range – and these high-end FPGAs are both large and expensive.

In multi-motor designs, a single MCU offers insufficient performance, while a single high-end FPGA provides sufficient performance but at a high cost.

New developments in the low-density FPGA market are now, however, offering a way for design engineers to square the circle, and to realize an affordable, single-chip solution to the problem of controlling multiple servo motors.

Varied Approaches to Bringing the MCU Inside the FPGA

Faced with the high cost of implementing a single-chip motor control system based on a high-end FPGA, designers have typically resorted to a two-chip approach, combining an MCU with a small, low-density, affordable FPGA. In this architecture (see Figure 1), the MCU typically handles the position and speed control function, and the FPGA manages the current control loop and the interface to the motor's position sensor (an encoder, Hall sensor or optical position sensor).

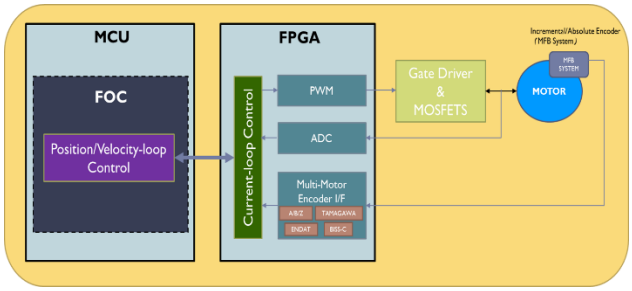

Fig. 1: typical two-chip architecture used for controlling a high-performance electric motor

This two-chip solution provides for deterministic control, but entails a more difficult board layout, a more complex supply chain, and higher bill-of-materials cost than the equivalent single-chip solution.

Manufacturers of low-end and mid-range FPGAs have responded to this dilemma by bringing an MCU inside their products, typically in the form of Arm® Cortex®-M MCU IP built into the FPGA. In some applications, the provision of an MCU core implemented in FPGA fabric can prove very useful, but for motor control routines, this soft-core MCU's struggle to provide the deterministic performance and timing that are required. In a soft-core MCU implementation, the rate at which the control loop is updated is typically lowered, limiting such a single-FPGA solution's ability to maintain reliable and smooth performance.

A New Hybrid Single-Chip Motor Solution

This has driven the development of innovation at the low-density end of the FPGA market: the GW5AS25 from GOWIN Semiconductor. This device combines a 288MHz Arm Cortex-M4-based MCU, the AT32F437 from Artery, with an Arora-V FPGA containing 23,040 logic elements in a single 256-pin package measuring 14mm x 14mm. The FPGA is fabricated in a low-power TSMC 22nm process.

The GW5AS25's system-in-package (SiP) configuration allows the motor system designer to partition system functionality between the MCU performing position/speed control, and the FPGA running the current control loops of one or two motors (see Figure 2).

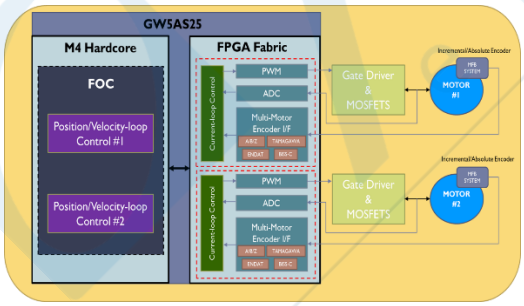

Fig. 2: multi-motor control in a single chip

As Figure 2 shows, this solution provides sufficient control-loop bandwidth to manage two motors operating at high speed, yet avoids the high cost and size penalties incurred by the use of a high-end FPGA to perform the same functions.

This hard-core MCU and FPGA SiP does more than provide a hardware platform for high-speed motor control: it is also supported by resources which help to accelerate the design of a single or dual permanent magnet synchronous motor (PMSM). These include:

- Reference design IP for implementing various forms of current loop control. Using this IP, the designer can achieve PWM switching frequency in excess of 20kHz.
- Built-in support for high-speed, real-time communication via an industrial Ethernet interface

In addition, encoder manufacturers supply VHDL and Verilog code for the interface to their products, simplifying their integration into an FPGA-based control system.

Single-Chip Solution Ready for Evaluation

Design engineers can experiment with the operation of the GW5AS25 by using a development kit, the DK_MOTOR_GW5AS-EV25UG256_V1.0 (see Figure 3). This kit includes a current control loop IP, an encoder controller, an industrial Ethernet interface, an ADC implemented in the FPGA, position/speed control loops, and Ethernet stack implemented in the MCU.

Fig. 3: the DK_MOTOR_GW5AS-EV25UG256_V1.0 enables rapid development of a multi-motor control system

This development kit demonstrates the feasibility of reducing the cost, size, and complexity of a multi-motor system design by implementing a single-chip control solution based on an FPGA and hard-core MCU in a compact SiP.