SENSYLINK Microelectronics

(CHS40100)
HR and SpO2 measurement

The CHS40100 is an ultra-low-power, completely integrated, optical data-acquisition system. It is ideal for smart wearable device

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1. Description

The CHS40100 is an ultra-low-power, completely integrated, optical data-acquisition system. On the transmitter side, the CHS40100 has three high current LED drivers. On the receiver side, CHS40100 consists of a high efficiency PIN photo-diode and an optical readout channel.

The optical readout has a low-noise signal conditioning analog front-end (AFE), including ADC(*resolution 19bits*) and an industry-lead ambient light cancellation (ALC) circuit. Due to the low power consumption, compact size, easy, flexible-to-use, and industry lead ambient light rejection capability of the CHS40100, the device is ideal for a wide variety of optical sensing applications such as heart rate detection and pulse oximetry.

The CHS40100 operates on a 1.7V to 3.6V VDD and a 3.0v to 3.6v VLED supply voltage. It can communicate at I2C- bus speeds up to 400 KHz. Each device has a large *256*-word built-in FIFO.

Available Package: 2.05mm x 2.505mm x 0.55mm, 8-pin OLGA package.

2. Features

- Analog Front-End (AFE) for PPG applications
- Integrated analog-domain ambient light cancellation
- Analog-to-Digital Conversion (ADC) with 19 bits resolution
- Three Low-Noise 7-Bit LED Current DACs
- Ultra-Low-Power Operation for Wearable Devices
- Temperature Range: -40˚C to 85˚C

3. Applications

- Headset devices
- True wireless stereo (TWS) earphones
- Mobile devices

4. Pin Configuration (Top View)

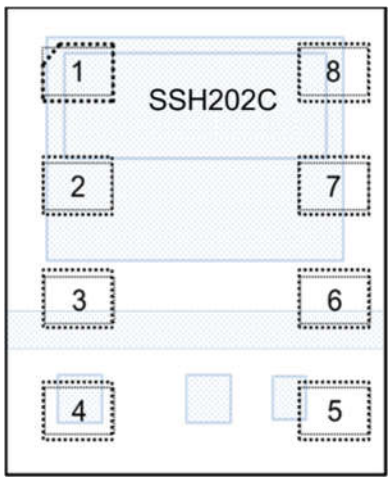


Figure1. Pin Configuration OLGA-8 package

5. Typical Application

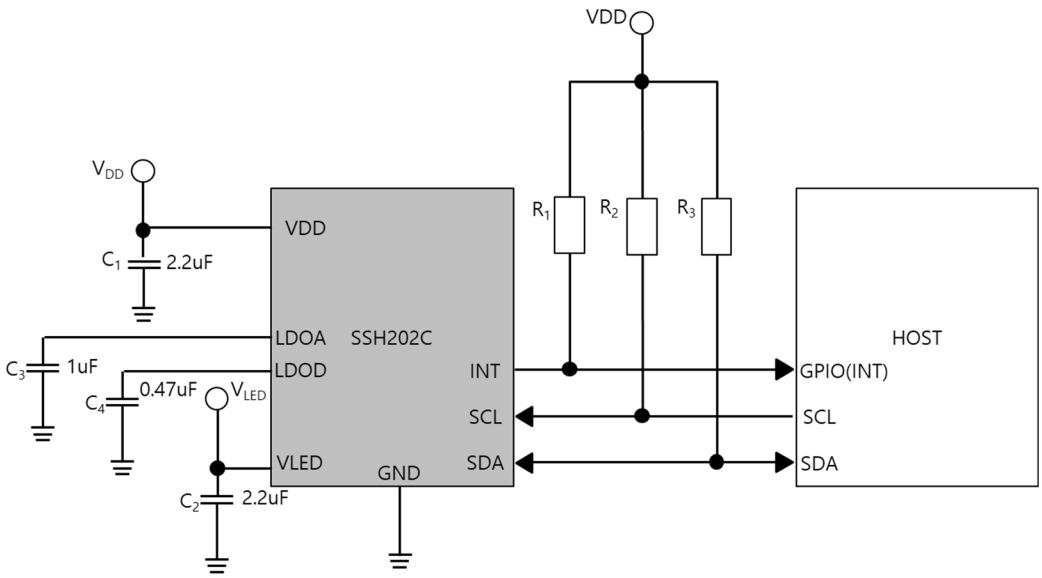


Figure2. Typical Application of CHS40100

Note:

1. Power supply decoupling capacitors (C1 ~ C4) must be placed as close to the VDD, VLED, LDOA and LDOD pin as possible.
2. PCB pattern of VDD and GND must be short and wide as much as possible.
3. Recommend resistor value is in the range of 0.9KΩ and 10KΩ. *@ (VIN=1.8V ~ 3.3V)*

6. Pin Description

PIN	*Name*	*Description*
1	VDD	Power
2	INT	Interrupt pin (Active Low)
3	LDOD	Digital 1.5V Low Drop Output Regulator
4	VLED	Power for LED
5	GND	Ground (Double bonding)
6	LDOA	Analog 1.5V Low Drop Output Regulator
7	SDA	I2C interface input / output (DATA)
8	SCL	I2C interface input (CLOCK).

7. Specification

7.1 Absolute Maximum Ratings

Over recommended operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	*Description*	*MIN*	*MAX*	*UNIT*
VDD	Power supply voltage	-0.3	4.0	V
VLED	Power supply voltage for LED	-0.3	4.0	V
SCL/SDA/INT	Logic Pins	-0.3	4.0	V
ESD(HBM)	ESD rating, HBM	±2000		V
ESD(MM)	ESD rating, MM	±200		V
ESD(CDM)	ESD rating, CDM	±500		V
TOPR	Operating temperature range	-20	85	℃
TSTG	Storage Temperature Range	-40	125	℃

7.2 Recommended Operating Conditions

SYMBOL	*Description*	*MIN*	*Typ*	*MAX*	*UNIT*
VDD	Power supply voltage	1.8	3.3	3.6	V
VLED	Power supply voltage for LED	3.0	3.3	3.6	V
Ta	Operating ambient temperature	-20		85	℃

7.3 Electrical Characteristics

(VDD = 3.3V, VLED = 3.3V, Sample_rate = 25sps, TA = 25°C, unless otherwise noted.)

SYMBOL	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
VDD	Power supply voltage		1.7	3.3	3.6	V
VLED	LED Supply Voltage		3.0	3.3	3.6	V
LDOD	LDOD Output Voltage			1.5		V
LDOA	LDOA Output Voltage			1.5		V
I_{DD}	Active Mode(1) Idle Mode(2)	Active state		1000. 2.5		uA
Read Out Channel						
RES_PPG	PPG Data			19		bits
RES_PROX	Proximity Data			16		bits
IR_{STD}	ADC Noise	Dark room, LED disable INT time = 16us		10		Counts
RED_{STD}						
$GREEN_{STD}$						
	ADC Integration Time		0.5		256	us
	PPG Sample Rate		25		4096	sps
	Maximum DC Ambient Light Rejection				50	uA
LED Driver						
I_{LED}	Full Scale LED Current				70(3)	mA
IR LED Characteristics(4)						
V_F	Forward voltage	If = 20 mA	1.2		1.7	V
Wp	Peak wavelength	If = 20 mA	935	940	945	nm
Iv	Radiant intensity	If = 20 mA	2.1	2.5	3.0	mW/sr
RED LED Characteristics(4)						
V_F	Forward voltage	If = 20 mA	1.8		2.5	V
Wp	Peak wavelength	If = 20 mA	655	660	665	nm
Iv	Radiant intensity	If = 20 mA	3.1	3.5	4.0	mW/sr
GREEN LED Characteristics(4)						
V_F	Forward voltage	If = 20 mA	2.4		3.0	V
Wd	Peak wavelength	If = 20 mA	520	528	535	nm
Iv	Radiant intensity	If = 20 mA	1200	1400	1700	mcd
PHOTODIODE Characteristics(4)(External)						
λ_{Smax}	Wavelength of max. sensitivity			890		nm
$\lambda_{10\%}$	Spectral range of sensitivity			400 to 1100		nm
On chip oscillator properties						
F_{OSC}	Oscillator Frequency	Internal oscillator	7.6	8.0	8.4	Mhz
DIGITAL I/O						

V_{IH}	SCL/SDA Input High Voltage		1.26			V
V_{IL}	SCL/SDA Input Low Voltage				0.54	V
V_{OL}	SDA/INT Output low voltage				0.4	V

Note:
1, Active Mode : Active state is MEAS_ON is enabled, the internal oscillator and PPG Sensing circuitry are active.
2, Idle Mode : Idle state is device initializes and enters the low power
3, Maximum current of Green LED is 20mA @ VLED = 3.3V.
4, For design guidance only.

7.4 I2C Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	*Parameter*	*Conditions*	*Min*	*Typ*	*Max*	*Unit*
f_{SCL}	SCL clock frequency			400		kHz
t_{BUS}	Bus free time between STOP condition and START condition		1.3		--	μs
t_{LOW}	LOW period of the SCL clock		1.3		--	μs
t_{HIGH}	HIGH period of the SCL clock		0.6		--	μs
t_{HDSTA}	Hold time (repeated) START condition		0.6		--	μs
t_{SUSTA}	Set-up time (repeated) START condition		0.6		--	μs
t_{SUSTO}	Set-up time for STOP condition		0.6		--	μs
t_{HDDAT}	Data hold time		50		--	ns
t_{SUDAT}	Data set-up time		100		--	ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter		0		50	ns

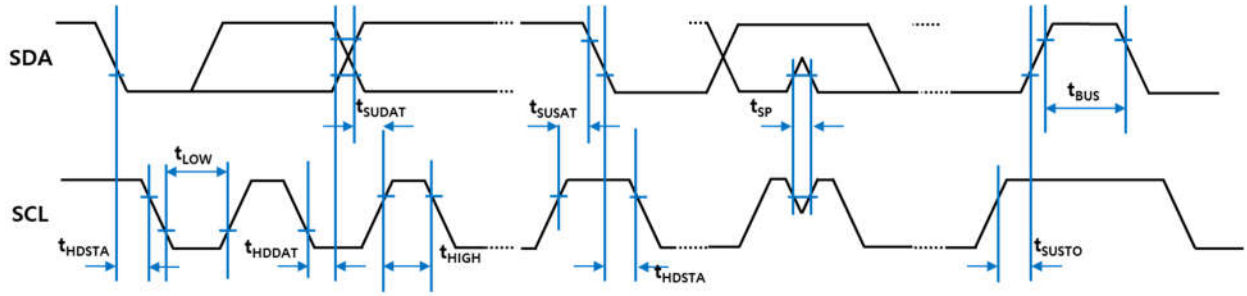


Figure3. I2C Timing Diagrams

8. Application Information

8.1 Overview

The CHS40100 is an ultra-low-power, completely integrated, optical data-acquisition system. On the transmitter side, the CHS40100 has three high current LED drivers. On the receiver side, CHS40100 consists of a high efficiency PIN photo-diode and an optical readout channel.

8.2 Functional Block Diagram

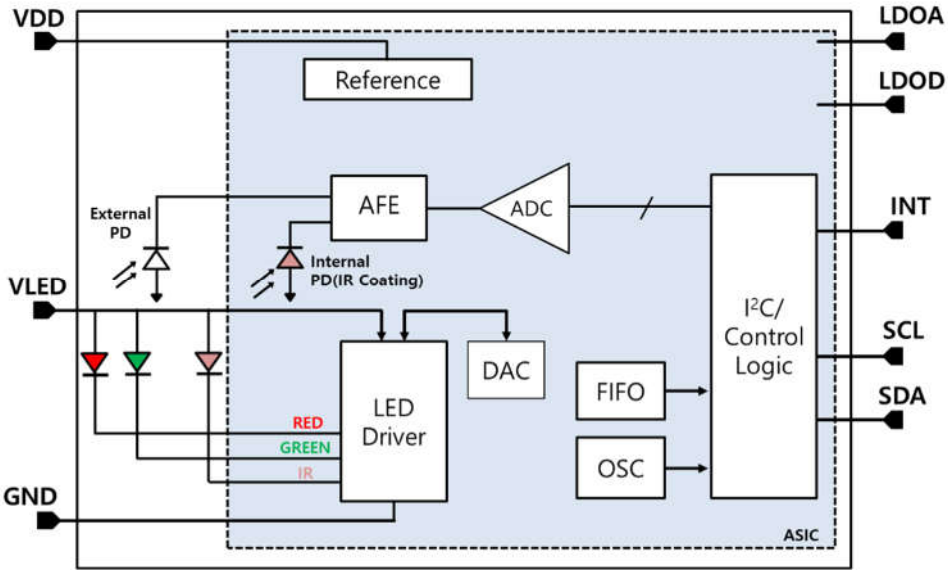


Figure4. Function Block Diagram

8.3 Operation Mode selection (0x00)

The CHS40100 can be selected operating sequence from MODE(0x00) register.

Table 1: Mode Register

Operating Sequence	MODE[2:0]	Description		
		SEQ0	SEQ1	SEQ2
PPG only	000	PPG0	-	-
	001	PPG0	PPG1	-
	010	PPG0	PPG1	PPG2
	011	-	PPG1	-
	100	-	PPG1	PPG2
Prox Only	101	PROX	-	-
Prox + PPG	110	PROX	PPG1	-
	111	PROX	PPG1	PPG2

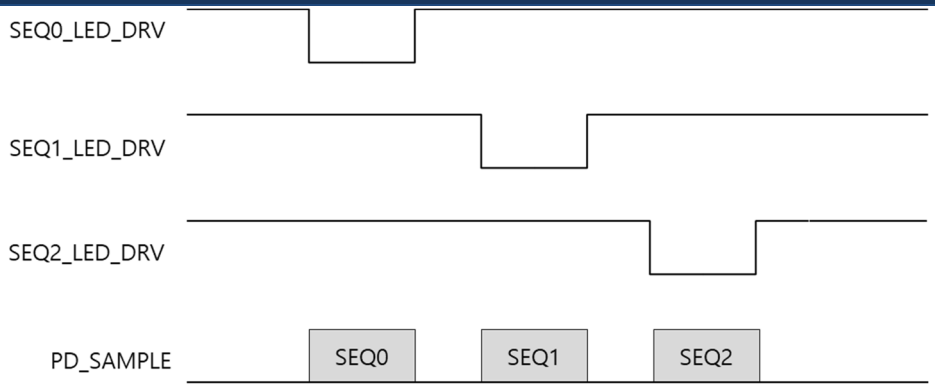


Figure5. Timing measurement (Mode: 010)

8.4 LED Driver

The CHS40100 integrates three precision LED driver current DACs that modulate LED pulses for a variety of optical measurements. The LED current DACs have 7 bits of dynamic range with five full-scale ranges of 16.7mA, 30.1mA, 43.4mA, 56.7mA and 70.0mA. The LED drivers are low dropout current sources allowing for low-noise, power-supply independent LED currents to be sourced at the lowest supply voltage possible, minimizing LED power consumption. The LED pulse width can be controlled from 0.5μs to 256μs(0.5 μs step).

8.4.1. LED Sequence Control (0x22)

The CHS40100 may select an LED light source corresponding to each SEQ through the SEQn_LED_SEL register.

Table 1 . SEQn_LED_SEL register

SEQn_LED_SEL[1:0]	LED Light Sources
00	RED (LED0)
01	GREEN (LED1)
10	IR (LED2)
11	Setting disable

8.5 FIFO Configuration

The FIFO has 256 sample depth. Each sample width is 3 bytes, which includes a 4-bit tag width. The tag embedded in the FIFO_DATA is used to identify the source of each sample data. The description of each tag is as shown in Table 3.

Index to the data within a sample identifies the input to the PPG channels.

Table 2 . FIFO Data Format

[23 : 20]	[19]	[18 :16]	[15 : 8]	[7 : 0]
Header[2] [3:0]	Flag[1]	SEQn Meas ADC Data / DAC / Time stamp[3] [18:0]		

Note:
1, Refer to Table 5
2, Refer to Table 4
3, When enabling the TIME_STAMP_EN register, the number of measurements can be read.

Table 3 . Header[3:0] description of FIFO data format

Header[3:0]	description
0000	Proximity
0001	SEQ0
0010	SEQ1
0011	SEQ2
0100	Reserved
0101	SEQ0_DAC
0110	SEQ1_DAC
0111	SEQ2_DAC
1000	Ambient of Proximity
1001	Ambient of SEQ0
1010	Ambient of SEQ1
1011	Ambient of SEQ2
1100	Reserved
1101	Reserved
1110	Reserved
1111	TIME_STAMP

Table 4 . Flag description of FIFO data format

Flag	description
0	No Saturated
1	Saturation Occurs

8.6 Write Pointer (register 0x10)

FIFO_WR_PTR[7:0] points to the FIFO location where the next item is written. This pointer advances for each item pushed on to the FIFO by the internal conversion process. The write pointer is a 8-bit counter and wraps around to count 0x00 on the next item after count 0xFF.

8.6.1. Read Pointer (register 0x11)

FIFO_RD_PTR[7:0] points to the location from where the next item from the FIFO is read using the serial interface. This advances each time an item is read from the FIFO.
The read pointer is a read-only register. The read pointer is updated from a 8-bit counter and wraps around to count 0x00 from count 0xFF.

8.6.2. Overflow Counter (register 0x12)

OVF_COUNTER[7:0] logs the number of items lost if the FIFO is not read in a timely fashion. This counter holds/saturates at count value 0xFF. When a complete item is popped from the FIFO (when the read pointer advances), the OVF_COUNTER is reset to zero. This counter is essentially a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred.

8.6.3. FIFO Data Counter (register 0x13)

FIFO_DATA_COUNT[7:0] is a read-only register that holds the number of items available in the FIFO for the host to read. This increments when a new item is pushed to the FIFO and decrements when the host reads an item from the FIFO.

8.6.4. FIFO Data (register 0x14)

FIFO_DATA[7:0] is a read-only register used to retrieve data from the FIFO. It is important to burst read the item from the FIFO. Each item is three bytes. So burst reading three bytes at FIFO_DATA register using the serial interface advances the FIFO_RD_PTR. The format and data type of the data stored in the FIFO is determined by the tag associated with the data. The readout from the FIFO follows a progression defined by the Sequence Control registers as well.

8.6.5. FIFO_A_FULL (0x15)

The FIFO_A_FULL[7:0] field in the FIFO Configuration(7.6) register (0x15) sets the watermark for the FIFO and determines when the A_FIFO_FULL bit in the Interrupt_Status register (0x05) gets asserted. The A_FIFO_FULL(0x05) bit is set when the FIFO contains 256 minus FIFO_A_FULL[7:0] items.

When the FIFO is almost full, if the A_FIFO_FULL_EN mask bit in the Interrupt_Enable register (0x04) is set, then A_FIFO_FULL bit gets asserted in the Interrupt Status register (0x05) and this bit is routed to the INT pin on the serial interface. This condition should prompt the applications processor to read samples off of the FIFO before it fills. The A_FIFO_FULL bit is cleared when the status register is write "1". (INT_CLR_MODE = 1)

The application processor can read both the FIFO_WR_PTR and FIFO_RD_PTR to calculate the number of items available in the FIFO, or just read the OVF_COUNTER and FIFO_DATA_COUNT registers, and read as many items as it needs to empty the FIFO. Alternatively, if the applications always responds much faster than the selected sample rate, it could just read 256 minus FIFO_A_FULL[7:0] items when it gets A_FIFO_FULL interrupt and be assured that all data from the FIFO are read.

8.6.6. FLUSH_FIFO (0x17)

The FIFO Flush bit is used for flushing the FIFO. The FIFO becomes empty and the FIFO_WR_PTR[7:0], FIFO_RD_PTR[7:0], FIFO_DATA_COUNT[7:0] and OVF_COUNTER[7:0] get reset to zero. FLUSH_FIFO is a self-clearing bit.

8.6.7. TIME_STAMP_EN (0x2F)

When the TIME_STAMP_EN bit is set to 1, the 2 bits time stamp gets pushed to the FIFO along with its tag for every sample. This time stamp is useful for aligning data from two devices after the host reads the FIFOs of those devices. When the TIME_STAMP_EN bit is set to 0, the sample counter is not pushed to FIFO.

8.7 Proximity Function

The CHS40100 includes an optical proximity function that could significantly reduce energy consumption and extend battery life when the sensor is not in contact with the skin. The proximity function can be used by setting the MODE bits filed over 5(Table 1). Proximity mode is enabled by setting the PROX_INT_EN bit field to 1 and setting a threshold in the *PROX_TH_HIGH register(0x46~0x47).*

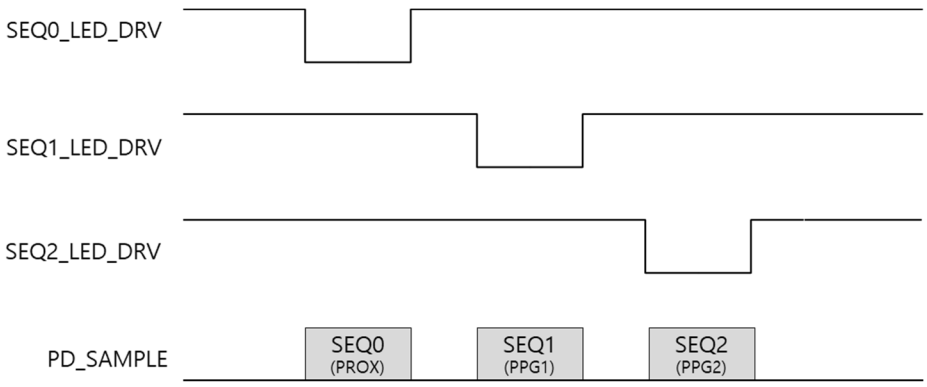


Figure6. Timing measurement (mode: 111)

When Proximity MODE is activated and the measurement exceeds *PROX_TH_HIGH,* CHS40100 also generates a proximity detection interrupt. In this case, the CHS40100 switches to the normal mode and changes the sampling rate to the speed allocated in the PPG register bit field Sample_Rate.

The *PROX_TH_HIGH* must be much lower than the signal available at the maximum LED current applied to the SEQ0_LED but high enough not to be triggered by noise from distant objects. In addition, the current assigned to the SEQ0_LED must be much lower than the current assigned to the SEQn_LED in normal mode. This ensures that the signal obtained from SEQ0 drops significantly when entering the proximity mode, thus providing sufficient hysteresis to eliminate multiple interrupts that occur during the proximity-normal mode transition.

CHS40100 in order to successfully switch from proximity mode to normal mode, *PROX_TH_HIGH* should be low enough and SEQ0_LED should be high enough for devices mounted on the darkest skin to return signals higher than PROX_TH_HIGH at SEQ0_LED current.

The proximity data is obtained by reading 0x1A and 0x1B. There are two ways to remove crosstalk compensation: analog and digital. Analog crosstalk compensation can be done through a register called PROX_DAC[7:0] at 0xA5. Digital crosstalk compensation can be done through a register called PROX_OFS[13:0] at 0x4C~0x4D.

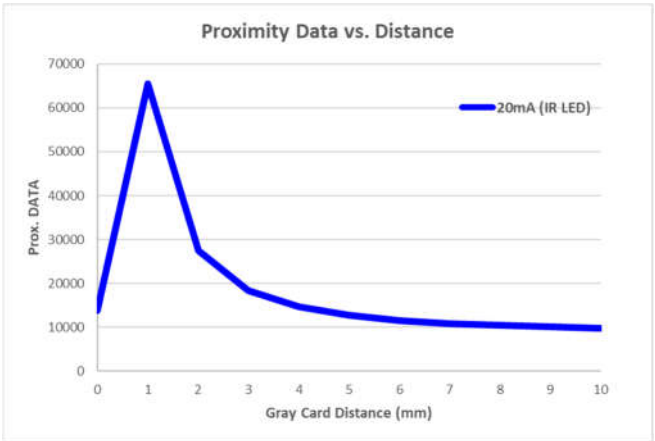


Figure7. Proximity Data vs. Distance (Gray Card) (T.B.D.)

Test Condition: Gray Card = O 社, LED = IR LED, PD = Internal PD, PROX_D_GAIN_EN = 1, PROX_D_GAIN =1 (x1)

8.8 Proximity Interrupt

The CHS40100 supports two proximity interrupt modes: threshold mode and state mode.
The INT_MODE (0x02) set to 0 enters threshold mode.

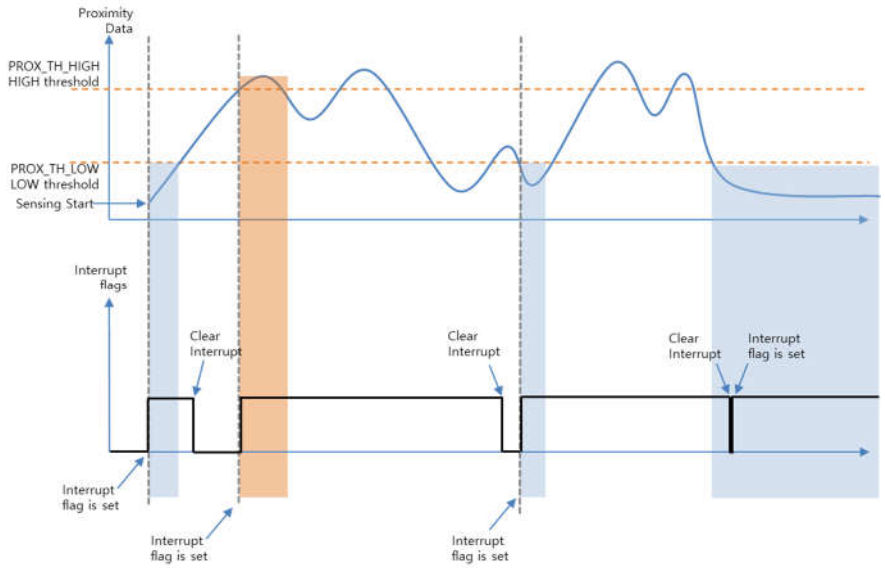


Figure8. Proximity Interrupt : threshold mode

The INT_MODE (0x02) set to 1 enters state mode.

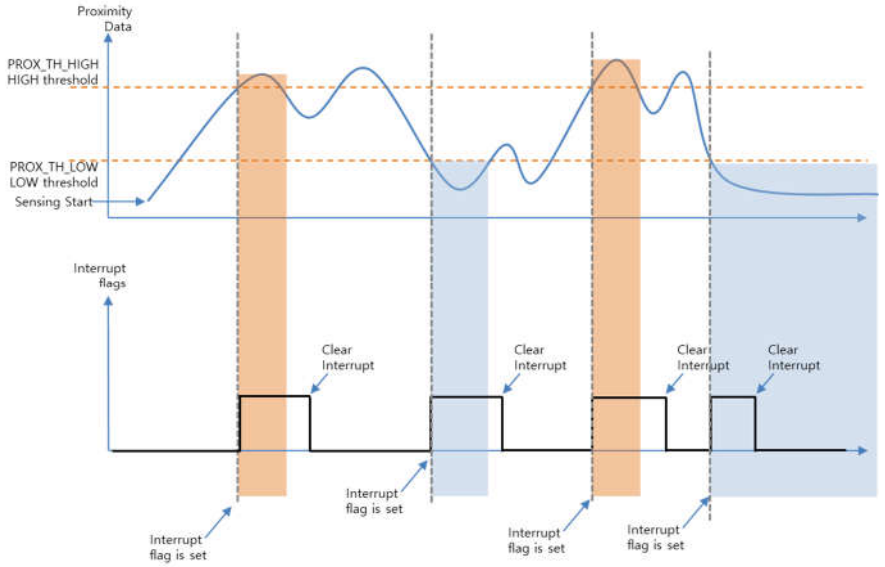


Figure9. Proximity Interrupt : state mode

8.9 Auto Control DAC

When the PPG measurement ADC value is saturation, the DAC value is automatically controlled. The meaning of saturation corresponds to when the intensity of ambient light is large and the signal measured by the set DAC value is large or small outside the measurable range. This range may be set through the PPG_TH_SEL register. By automatically adjusting the DAC value according to the ADC value output through the PPG_TH_SEL register, the range of the output measurements can be adjusted.

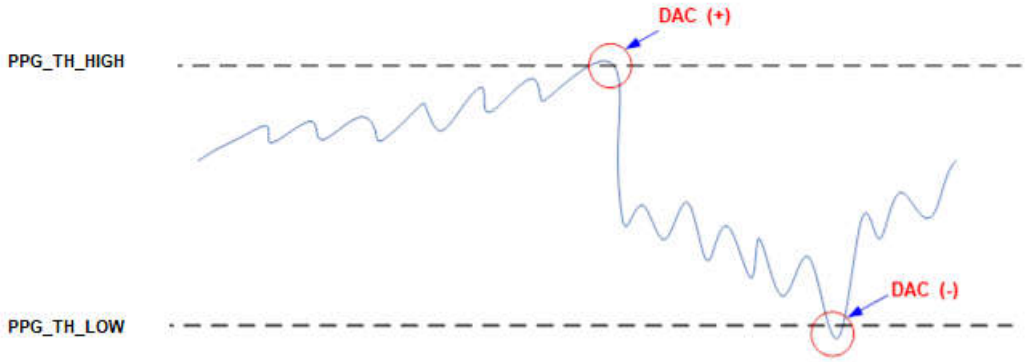


Figure10. Auto Control DAC

The PPG data is automatically scaled by the DAC value and the measured ADC value. The SEQn_DC_EXTEND_OFF(0xBA, 0xBC, 0xBE) can be set to 1 to disable the ability to expand.

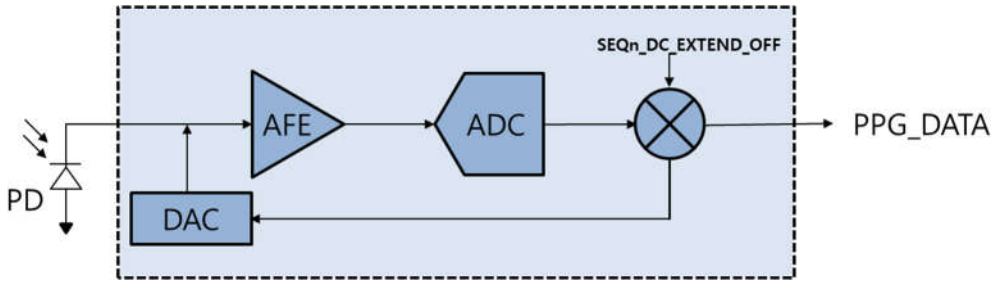


Figure11. PPG DATA

8.10 Simplified CHS40100 Diagram

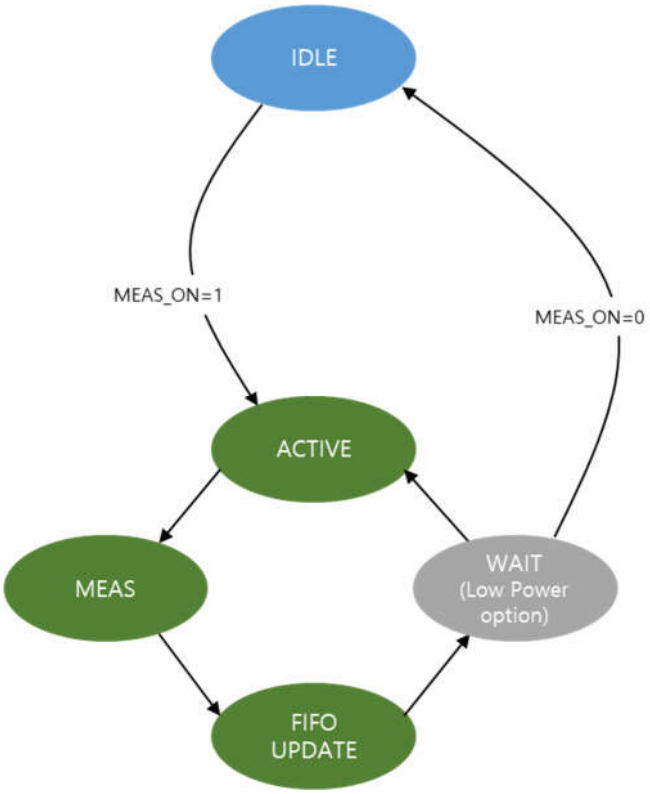


Figure12. CHS40100 Diagram

8.11 Power on / off sequence

The CHS40100 sensor needs that power supply VDD and VLED.

Upon power-up, the device initializes and enters the low power IDLE mode state.

In this operational state the internal oscillator and other circuitry are not active, resulting in low power consumption.

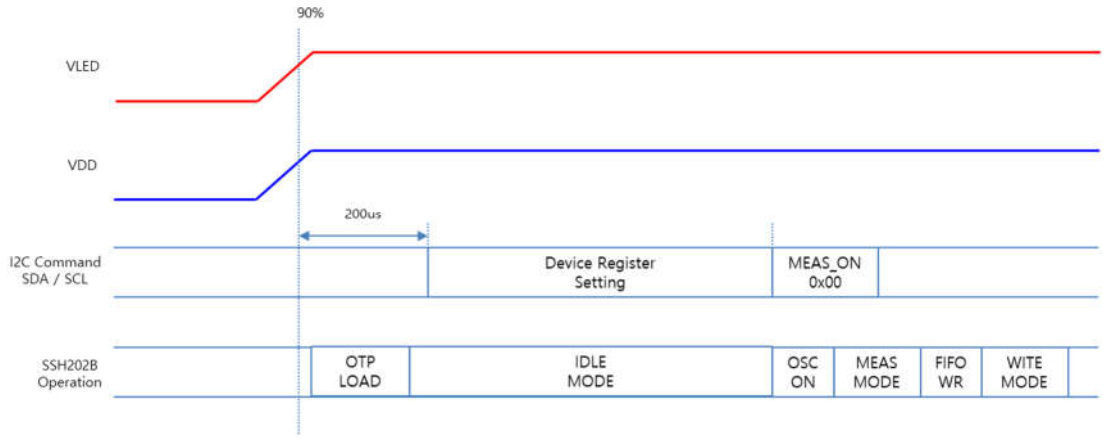


Figure13. Power On Sequence

Re-start after VDD goes to 0V and at least 2ms after power down.

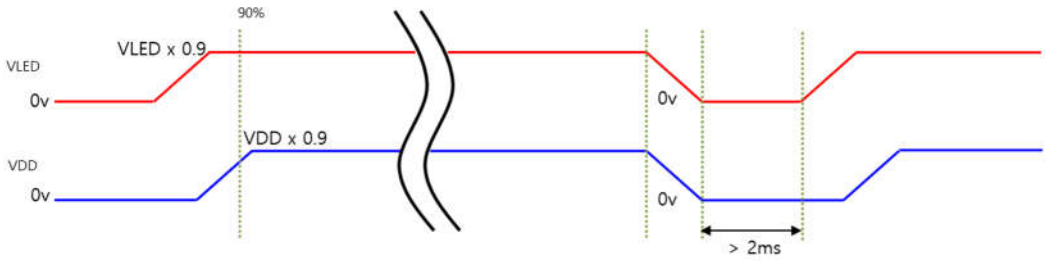


Figure14. Power Off Sequence

9. Register Map

9.1 Register Table

ADD (HEX)	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
0x00	RW	-	MODE[2:0]			MEAS_ON	LP_MODE	-	-	00
0x01	RWC	-	-	-	-	-	-	-	SW RESET	00
0x02	RW	-	-	-	INT_MODE	-	-	-	INT_CLR_MODE	01
0x03	RW	-	-	-	PROX_STATE_MODE	-	-	PROX_PERSISTENCE[1:0]		00
0x04	RW	A_FIFO_FULL_EN	FIFO_DATA_RDY_EN	ALC_SAT_EN	PPG_SAT_EN	PROX_SAT_EN	-	PROX_INT_EN	-	B8
0x05	RWC	A_FIFO_FULL	FIFO_DATA_RDY	ALC_SAT	PPG_SAT	PROX_SAT	-	PROX_INT_H	PROX_INT_L	00
0x10	RW	FIFO_WR_PTR[7:0]								00
0x11	RO	FIFO_RD_PTR[7:0]								00
0x12	RO	OVF_COUNTER[7:0]								00
0x13	RO	FIFO_DATA_COUNT[7:0]								00
0x14	RO	FIFO_DATA[7:0]								00
0x15	RW	FIFO_A_FULL[7:0]								C0
0x16	RW	-	-	-	-	-	-	FIFO_OV_WR	-	00
0x17	RWC	-	-	-	-	-	-	-	FLUSH_FIFO	00
0x1A	RO	PROX_DATA[15:8]								00
0x1B	RO	PROX_DATA[7:0]								00
0x20	RW	-	-	-	-	SAMPLE_RATE[3:0]				00
0x22	RW	-	-	SEQ0_LED_SEL[1:0]		SEQ1_LED_SEL[1:0]		SEQ2_LED_SEL[1:0]		24
0x23	RW	-	SEQ0_LED_CUR[6:0]							00
0x24	RW	-	-	-	-	-	SEQ0_LED_RANGE[2:0]			00
0x25	RW	-	SEQ1_LED_CUR[6:0]							00
0x26	RW	-	-	-	-	-	SEQ1_LED_RANGE[2:0]			04
0x27	RW	-	SEQ2_LED_CUR[6:0]							00
0x28	RW	-	-	-	-	-	SEQ2_LED_RANGE[2:0]			04
0x2E	RW	-	-	-	PPG_FILTER_RST_EN	-	-	PPG_FILTER_ON	PPG_FILTER_MODE	00
0x2F	RW	TIME_STAMP_EN	-	-	-	-	-	PROX_FILTER_ON	PROX_FILTER_SEL	00
0x30	RW	-	-	-	-	-	-	-	SEQ0_INT_TIME[8]	00
0x31	RW	SEQ0_INT_TIME[7:0]								0F

ADD (HEX)	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
0x32	RW	-	-	-	-	-	-	-	SEQ1_INT_TIME[8]	00
0x33	RW	SEQ1_INT_TIME[7:0]								0F
0x34	RW	-	-	-	-	-	-	-	SEQ2_INT_TIME[8]	00
0x35	RW	SEQ2_INT_TIME[7:0]								0F
0x3C	RW	PPG_OFS_EN	PPG_OFS_SIGN	PPG_OFS[13:8]						20
0x3D	RW	PPG_OFS[7:0]								00
0x3F	RW	1(1)	0 (1)	SEQ0_PDSEL[1:0]		SEQ1_PDSEL[1:0]		SEQ2_PDSEL[1:0]		85
0x40	RW	PROX_TH_LOW[15:8]								00
0x41	RW	PROX_TH_LOW[7:0]								00
0x42	RW	PROX_TH_HIGH[15:8]								FF
0x43	RW	PROX_TH_HIGH[7:0]								FF
0x4C	RW	PROX_OFS_EN	PROX_OFS_SIGN	PROX_OFS[13:8]						20
0x4D	RW	PROX_OFS[7:0]								00
0x50	RW	-	-	-	-	-	-	ALC_STEP_OFS[9:8]		01
0x51	RW	ALC_STEP_OFS[7:0]								00
0x5A	RW	DC_CUT_MODE [1:0]		0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	00
0x73	RW	SA_SEL[1:0]		0 (1)	0 (1)	0 (1)	0 (1)	TRIM_STATUS[1:0]		03
0xA0	RW	-	SEQ0_ADAC_RANGE[2:0]			-	-	SEQ0_DDAC_RANGE [1:0]		30
0xA1	RW	-	SEQ1_ADAC_RANGE[2:0]			-	-	SEQ1_DDAC_RANGE [1:0]		30
0xA2	RW	-	SEQ2_ADAC_RANGE[2:0]			-	-	SEQ2_DDAC_RANGE [1:0]		30
0xA5	RW	PROX_DAC[7:0]								00
0xB1	RW	-	-	-	-	-	-	PPG_TH_SEL [1:0]		00
0xB6	RW	-	-	-	-	PROX_D_GAIN_EN	PROX_D_GAIN_OP	PROX_D_GAIN [1:0]		09
0xB7	RW	-	-	-	-	0 (1)	PROX_FIFO_OFF	DAC_FIFO_ON	FIFO_AMB_WR	00
0xBA	RW	SEQ0_DC_EXTEND_OFF	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	00
0xBC	RW	SEQ1_DC_EXTEND_OFF	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	00
0xBE	RW	SEQ2_DC_EXTEND_OFF	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	0 (1)	00
0xFA	RO	CHIP_ID[7:0]								A3

Note:
1, Must be set to default value.

9.2 Register Description

<table>
<tr><th rowspan="2">ADD (HEX)</th><th rowspan="2">Bit Width</th><th colspan="3">Register Description</th></tr>
<tr><th>Name</th><th>Description</th><th>Default (hex)</th></tr>
<tr><td>0x00</td><td>[6:4]</td><td>MODE[2:0]</td><td>These bits set the operating Mode.
<table>
<tr><th rowspan="2">Operating Sequence</th><th rowspan="2">MODE[2:0]</th><th colspan="3">Description</th></tr>
<tr><th>SEQ0</th><th>SEQ1</th><th>SEQ2</th></tr>
<tr><td rowspan="5">PPG only</td><td>000</td><td>PPG0</td><td>-</td><td>-</td></tr>
<tr><td>001</td><td>PPG0</td><td>PPG1</td><td>-</td></tr>
<tr><td>010</td><td>PPG0</td><td>PPG1</td><td>PPG2</td></tr>
<tr><td>011</td><td>-</td><td>PPG1</td><td>-</td></tr>
<tr><td>100</td><td>-</td><td>PPG1</td><td>PPG2</td></tr>
<tr><td>Prox Only</td><td>101</td><td>PROX</td><td>-</td><td>-</td></tr>
<tr><td rowspan="2">Prox + PPG</td><td>110</td><td>PROX</td><td>PPG1</td><td>-</td></tr>
<tr><td>111</td><td>PROX</td><td>PPG1</td><td>PPG2</td></tr>
</table></td><td>0x0</td></tr>
<tr><td>x00</td><td>[3]</td><td>MEAS_ON</td><td>This bit sets the operation of measurement.
0 : disable measurement (default)
1 : enable measurement</td><td>0x0</td></tr>
<tr><td>0x00</td><td>[2]</td><td>LP_MODE</td><td>This bit sets the Low power option for Active Mode .
It reduces the power of AFE block when wait state.
0 : disable (default)
1 : enable</td><td>0x0</td></tr>
<tr><td>0x01</td><td>[0]</td><td>SW_RESET</td><td>This bit set the software reset and after auto clear.
0 : normal (default)
1 : software reset</td><td>0x0</td></tr>
<tr><td>0x02</td><td>[4]</td><td>INT_MODE</td><td>Interrupt assert condition
0 : clear after conti (default)
1 : clear after next event</td><td>0x0</td></tr>
<tr><td>0x02</td><td>[0]</td><td>INT_CLR_MODE</td><td>Interrupt clear method
0 : 0x05 command read
1 : 0x05 command write “H” then interrupt status cleared (default)</td><td>0x1</td></tr>
<tr><td>0x03</td><td>[4]</td><td>PROX_STATE_MODE</td><td>Select Interrupt mode.
It’s valid when Prox MODE is activated.
0 : threshold mode (default)
1 : hysteresis mode (H -> L -> H…)</td><td>0x0</td></tr>
<tr><td>0x03</td><td>[1:0]</td><td>PROX_PERSISTENCE[1:0]</td><td>sample number of threshold judgments
It’s valid when Proximity MODE is activated.
0 : interrupt status is updated if Any value outside proximity thresholds. (default)
1 : interrupt status is updated if 2 consecutive threshold judgments are the same.
2 : interrupt status is updated if 4 consecutive threshold judgments are the same.
3 : interrupt status is updated if 8 consecutive threshold judgments are the same.</td><td>0x0</td></tr>
<tr><td>0x04</td><td>[7]</td><td>A_FIFO_FULL_EN</td><td>Enable “A_FIFO_FULL” interrupts.</td><td>0x1</td></tr>
<tr><td>0x04</td><td>[6]</td><td>FIFO_DATA_RDY_EN</td><td>Enable “FIFO_DATA_RDY” interrupts</td><td>0x0</td></tr>
<tr><td>0x04</td><td>[5]</td><td>ALC_SAT_EN</td><td>Enable “ALC_SAT” interrupts</td><td>0x1</td></tr>
<tr><td>0x04</td><td>[4]</td><td>PPG_SAT_EN</td><td>Enable “PPG_SAT” interrupts</td><td>0x1</td></tr>
<tr><td>0x04</td><td>[3]</td><td>PROX_SAT_EN</td><td>Enable “PROX_SAT” interrupts</td><td>0x1</td></tr>
<tr><td>0x04</td><td>[1]</td><td>PROX_INT_EN</td><td>Enable “ PROX_INT_H/L” interrupts</td><td>0x0</td></tr>
</table>

ADD (HEX)	Bit Width	Register Description		
		Name	Description	Default (hex)
0x05	[7]	A_FIFO_FULL	This bit is cleared by writing “H” the Interrupt Status (0x05) Register. (INT_CLR_MODE = 1) 0 : Normal Operation 1 : Indicates that the FIFO buffer will overflow the threshold set by FIFO_A_FULL[7:0] on the next sample.	0x0
0x05	[6]	FIFO_DATA_RDY	This bit is cleared by writing “H” the Interrupt Status (0x05) Register. (INT_CLR_MODE = 1) 0 : Normal Operation 1 : This interrupt triggers when there is a new data in the FIFO.	0x0
0x05	[5]	ALC_SAT	This bit is cleared by writing “H” the Interrupt Status (0x05) Register. (INT_CLR_MODE = 1) 0 : Normal Operation 1 : This interrupt triggers when the ambient light cancellation function of the photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC.	0x0
0x05	[4]	PPG_SAT	This bit is cleared by writing “H” the Interrupt Status (0x05) Register. (INT_CLR_MODE = 1) 0 : Normal Operation 1 : This interrupt triggers when the signal of measurement of the photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC.	0x0
0x05	[3]	PROX_SAT	This bit is cleared by writing “H” the Interrupt Status (0x05) Register. (INT_CLR_MODE = 1) 0 : Normal Operation 1 : This interrupt triggers when the proximity signal of measurement of the photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC.	0x0
0x05	[1]	PROX_INT_H	This bit is cleared by writing “H” the Interrupt Status (0x05) Register. (INT_CLR_MODE = 1) 0 : Normal Operation 1 : This interrupt is triggered when the "PROX_TH_HIGH " function is completed.	0x0
0x05	[0]	PROX_INT_L	This bit is cleared by writing “H” the Interrupt Status (0x05) Register. (INT_CLR_MODE = 1) 0 : Normal Operation 1 : This interrupt is triggered when the "PROX_TH_LOW" function is completed.	0x0
0x10	[7:0]	FIFO_WR_PTR[7:0]	This points to the location where the next sample is to be written. This pointer advances for each sample pushed on to the circular FIFO.	0x0
0x11	[7:0]	FIFO_RD_PTR[7:0]	Read Only. The FIFO Read Pointer points to the location from where the processor gets the next sample from the FIFO using the serial interface.	0x0
0x12	[7:0]	OVF_COUNTER[7:0]	When FIFO is full any new samples will result in new or old samples getting lost depending on FIFO_RO. OVF_COUNTER counts the number of samples lost. It saturates at 0xFF.	0x0
0x13	[7:0]	FIFO_DATA_COUNT[7:0]	This is a read-only register which holds the number of items available in the FIFO for the host to read. This increments when a new item is pushed to the FIFO, and decrements when the host reads an item from the FIFO.	0x0
0x14	[7:0]	FIFO_DATA[7:0]	These are read-only register and is used to get data from the FIFO. It will change FIFO_RD_PTR if read 3-byte units from continuous mode.	0x0
0x15	[7:0]	FIFO_A_FULL[7:0]	These bits indicate how many new samples can be written to the FIFO before the interrupt is asserted. For example, if set to 0xF, the interrupt triggers when there is 15 empty space left (241 entries), and so on.	0xC0
0x16	[1]	FIFO_OV_WR	This bit determines whether data is overwritten when FIFO is full. 0 : overwrite off (default) 1 : overwrite on	0x0
0x17	[0]	FLUSH_FIFO	FIFO Clear	0x0
0x1A	[7:0]	PROX_DATA[15:8]	This is a read-only register and is used to get high bytes of proximity data when proximity mode is set.	0x0
0x1B	[7:0]	PROX_DATA[7:0]	This is a read-only register and is used to get low bytes of proximity data when proximity mode is set.	0x0

ADD (HEX)	Bit Width	Register Description		
		Name	Description	Default (hex)
0x20	[3:0]	SAMPLE_RATE[3:0]	These bits set the effective sampling rate of the PPG sensor 0 : 32 sps (default) 1 : 64 sps (LP_MODE : 63.5 sps) 2 : 128 sps (LP_MODE : 125 sps) 3 : 192 sps (LP_MODE : 190.5 sps) 4 : 256 sps (LP_MODE : 250 sps) 5 : 512 sps (LP_MODE : 500 sps) 6 : 25 sps 7 : 50 sps 8 : 100 sps 9 : 200 sps 10 : 400 sps 11 : 500 sps 12 : 4096 sps (LP_MODE : 500 sps) 13 : setting disable 14 : setting disable 15 : setting disable When LP_MODE enable,	0x0
0x22	[5:4]	SEQ0_LED_SEL[1:0]	These bits set the LED source selection in the measurement area PROX or SEQ0. 0 : RED 1 : GREEN 2 : IR (default) 3 : setting disable	0x2
0x22	[3:2]	SEQ1_LED_SEL[1:0]	These bits set the LED source selection in the measurement area SEQ2. 0 : RED 1 : GREEN (default) 2 : IR 3 : setting disable	0x1
0x22	[1:0]	SEQ2_LED_SEL[1:0]	These bits set the LED source selection in the measurement area SEQ1. 0 : RED(default) 1 : GREEN 2 : IR 3 : setting disable	0x0
0x23	[6:0]	SEQ0_LED_CUR[6:0]	These bits set a LED current that the measurement of SEQ0 area. SEQ0_LED_RANGE x (SEQ0_LED_CUR + 1) / 128	0x0
0x24	[2:0]	SEQ0_LED_RANGE[2:0]	This bit sets the maximum range of LED current in the measurement area SEQ0. 000 : 16.7mA (default) 001 : 30.1mA 010 : 43.4mA 011 : 56.7mA 100 : 70.0mA 101 : Setting Disable 110 : Setting Disable 111 : Setting Disable	0x0
0x25	[6:0]	SEQ1_LED_CUR[6:0]	These bits set a LED current that the measurement of SEQ1 area. SEQ1_LED_RANGE x (SEQ1_LED_CUR + 1) / 128	0x0
0x26	[2:0]	SEQ1_LED_RANGE[2:0]	This bit sets the maximum range of LED current in the measurement area SEQ1. 000 : 16.7mA 001 : 30.1mA 010 : 43.4mA 011 : 56.7mA 100 : 70.0mA (default) 101 : Setting Disable 110 : Setting Disable 111 : Setting Disable	0x4
0x27	[6:0]	SEQ2_LED_CUR[6:0]	These bits set a LED current that the measurement of SEQ2 area. SEQ2_LED_RANGE x (SEQ2_LED_CUR + 1) / 128	0x0
0x28	[2:0]	SEQ2_LED_RANGE[2:0]	This bit sets the maximum range of LED current in the measurement area SEQ2. 000 : 16.7mA 001 : 30.1mA 010 : 43.4mA 011 : 56.7mA 100 : 70.0mA (default) 101 : Setting Disable 110 : Setting Disable 111 : Setting Disable	0x4

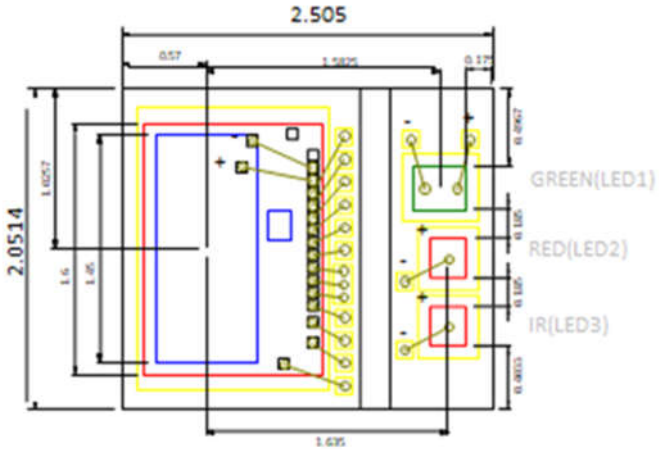
ADD (HEX)	Bit Width	Register Description		
		Name	Description	Default (hex)
0x2E	[4]	PPG_FILTER_RST_EN	Enable the PPG_FILTER reset function when using the PPG_FILTER. 0 : Reset disable (default) 1 : Reset enable (Not guarantee PPG Data)	0x0
0x2E	[1]	PPG_FILTER_ON	Enable the PPG_FILTER function. 0 : disable (default) 1 : enable	0x0
0x2E	[0]	PPG_FILTER_MODE	This bit sets the PPG FILTER mode. 0 : PPG Filter Mode 0 (default) 1 : PPG Filter Mode 1	0x0
0x2F	[7]	TIME_STAMP_EN	Enable the TIME_STAMP function. Refer to Table 3.	0x0
0x2F	[1]	PROX_FILTER_ON	Enable the Moving average Filter when using the Proximity function. 0 : disable (default) 1 : enable	0x0
0x2F	[0]	PROX_FILTER_SEL	This bit sets the window size of number in the Moving Average Filter. 0 : 4 (default) 1 : 8	0x0
0x30	[0]	SEQ0_INT_TIME[8]	These bits set the integrate time in the measurement area SEQ0. (N+1) x 0.5us	0x0
0x31	[7:0]	SEQ0_INT_TIME [7:0]	These bits set the integrate time in the measurement area SEQ0. (N+1) x 0.5us	0xF
0x32	[0]	SEQ1_INT_TIME[8]	These bits set the integrate time in the measurement area SEQ1. (N+1) x 0.5us	0x0
0x33	[7:0]	SEQ1_INT_TIME[7:0]	These bits set the integrate time in the measurement area SEQ1. (N+1) x 0.5us	0xF
0x34	[0]	SEQ2_INT_TIME[8]	These bits set the integrate time in the measurement area SEQ2. (N+1) x 0.5us	0x0
0x35	[7:0]	SEQ2_INT_TIME[7:0]	These bits set the integrate time in the measurement area SEQ2. (N+1) x 0.5us	0xF
0x3C	[7]	PPG_OFS_EN	This bit sets the offset function in the PPG data.	0x0
0x3C	[6]	PPG_OFS_SIGN	This bit sets the sign of the direction in the offset function. 0 : PPG Data + OFS (default) 1 : PPG Data - OFS	0x0
0x3C	[5:0]	PPG_OFS[13:8]	These bits set the offset value.	0x20
0x3D	[7:0]	PPG_OFS[7:0]	These bits set the offset value.	0x0
0x3F	[5:4]	SEQ0_PDSEL[1:0]	These bits set the PD selection in the measurement area SEQ0. 0 : Internal PD (default) : This PD is include ROIC. 1 : External PD 2 : setting disable	0x0
0x3F	[3:2]	SEQ1_PDSEL[1:0]	These bits set the PD selection in the measurement area SEQ1. 0 : Internal PD : This PD is include ROIC. 1 : External PD (default) 2 : setting disable	0x1
0x3F	[1:0]	SEQ2_PDSEL[1:0]	These bits set the PD selection in the measurement area SEQ2. 0 : Internal PD : This PD is include ROIC. 1 : External PD (default) 2 : setting disable	0x1
0x40	[7:0]	PROX_TH_LOW[15:8]	This register sets the high byte of the PROX_MIN threshold.	0x0
0x41	[7:0]	PROX_TH_LOW[7:0]	This register sets the low byte of the PROX_MIN threshold.	0x0
0x42	[7:0]	PROX_TH_HIGH[15:8]	This register sets the high byte of the PROX_MAX threshold.	0xFF
0x43	[7:0]	PROX_TH_HIGH[7:0]	This register sets the low byte of the PROX_MAX threshold.	0xFF
0x4C	[7]	PROX_OFS_EN	This bit sets the offset function in the PROX data.	0x0
0x4C	[6]	PROX_OFS_SIGN	This bit sets the sign of the direction in the offset function. 0 : PROX Data + OFS (default) 1 : PROX Data - OFS	0x0
0x4C	[5:0]	PROX_OFS[13:8]	These bits set the offset value.	0x20
0x4D	[7:0]	PROX_OFS[7:0]	These bits set the offset value.	0x0

ADD (HEX)	Bit Width	Register Description		
		Name	Description	Default (hex)
0x50	[1:0]	ALC_STEP_OFS[9:8]	These bits set the ADAC target margin.	0x1
0x51	[7:0]	ALC_STEP_OFS[7:0]	These bits set the ADAC target margin.	0x0
0x5A	[7:6]	DC_CUT_MODE[1:0]	These bits set the minus value for extended PPG DATA. When 0 and 1 are set, automatically remove DC values of PPG DATA. 0 : extended PPG DATA - (current DAC - 1) = PPG DATA (default) 1 : extended PPG DATA - (current DAC - 2) = PPG DATA 2 : extended PPG DATA = PPG DATA	0x0
0x73	[7:6]	SA_SEL[1:0]	These bits set the slave address of I2C. 0 : 0x3A (default) 1 : 0x3B 2 : 0x38 3 : 0x39	0x0
0x73	[1:0]	TRIM_STATUS[1:0]	Read only These bits can read the Trim status. 00 : The trim is not yet. 11 : The trim is done.	0x3
0xA0	[6:4]	SEQ0_ADAC_RANGE[2:0]	This bit sets the maximum range of ADAC current in the measurement area SEQ0. 0 : 6.38 uA 1 : 12.75 uA 2 : 19.13 uA 3 : 25.50 uA (default) 4 : 31.88 uA 5 : 38.25 uA 6 : 44.63 uA 7 : 51.00 uA *Design guarantee	0x3
0xA0	[3:0]	SEQ0_DDAC_RANGE[2:0]	This bit sets the maximum range of DDAC current in the measurement area SEQ0. 0 : 200 uA (default) 1 : 210 uA 2 : 220 uA 3 : 230 uA *Design guarantee	0x0
0xA1	[7:4]	SEQ1_ADAC_RANGE[2:0]	This bit sets the maximum range of ADAC current in the measurement area SEQ1. 0 : 6.38 uA 1 : 12.75 uA 2 : 19.13 uA 3 : 25.50 uA (default) 4 : 31.88 uA 5 : 38.25 uA 6 : 44.63 uA 7 : 51.00 uA *Design guarantee	0x3
0xA1	[3:0]	SEQ1_DDAC_RANGE[2:0]	This bit sets the maximum range of DDAC current in the measurement area SEQ1. 0 : 200 uA (default) 1 : 210 uA 2 : 220 uA 3 : 230 uA *Design guarantee	0x0
0xA2	[7:4]	SEQ2_ADAC_RANGE[2:0]	This bit sets the maximum range of ADAC current in the measurement area SEQ2. 0 : 6.38 uA 1 : 12.75 uA 2 : 19.13 uA 3 : 25.50 uA (default) 4 : 31.88 uA 5 : 38.25 uA 6 : 44.63 uA 7 : 51.00 uA *Design guarantee	0x3

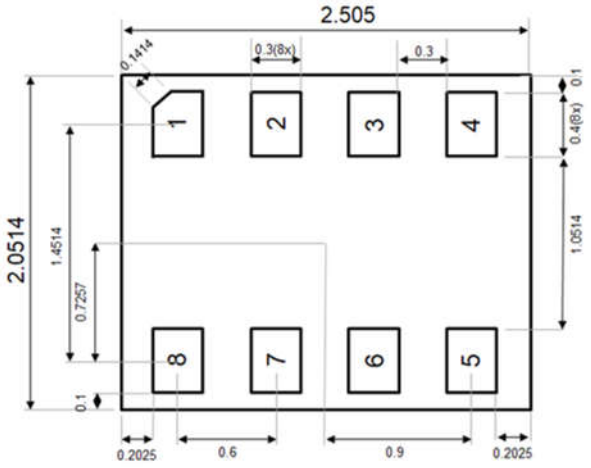
ADD (HEX)	Bit Width	Register Description		
		Name	Description	Default (hex)
0xA2	[3:0]	SEQ2_DDAC_RANGE[2:0]	This bit sets the maximum range of DDAC current in the measurement area SEQ2. 0 : 200 uA (default) 1 : 210 uA 2 : 220 uA 3 : 230 uA *Design guarantee	0x0
0xA5	[7:0]	PROX_DAC [7:0]	These bits set the DAC value when using PROX function. This register functions to remove the value corresponding to Crosstalk using DAC.	0x0
0xB1	[1:0]	PPG_TH_SEL [1:0]	These bits set threshold value for finding DAC in PPG mode. (Refer to 7.9. Auto Control DAC) 0 : PPG_TH_HIGH = 95% , PPG_TH_LOW = 5% (default) 1 : PPG_TH_HIGH = 90% , PPG_TH_LOW = 10% 2 : PPG_TH_HIGH = 85% , PPG_TH_LOW = 15% 3 : PPG_TH_HIGH = 80% , PPG_TH_LOW = 20%	0x0
0xB6	[3]	PROX_D_GAIN_EN	This bit sets the offset function in the digital gain for prox data. 0 : disable 1 : enable (default)	0x1
0xB6	[2]	PROX_D_GAIN_OP	Select Over-Sampling mode. It's valid when PROX_D_GAIN_EN is activated. 0 : disable (default) 1 : enable	0x0
0xB6	[1:0]	PROX_D_GAIN[1:0]	This register sets the bits of digital gain for prox data. 0 : x1/2 1 : x1 (default) 2 : x2 3 : x4	0x1
0xB7	[2]	PROX_FIFO_OFF	Options for updating Proximity to a FIFO. 0 : Update Proximity Data to a FIFO (default) 1 : Don't update Proximity Data to a FIFO	0x0
0xB7	[1]	DAC_FIFO_ON	Options for updating DAC to a FIFO. 0 : Don't update DAC Data to a FIFO (default) 1 : Update DAC Data to a FIFO	0x0
0xB7	[0]	FIFO_AMB_WR	Options for updating AMB to a FIFO. 0 : Don't update AMB Data to a FIFO (default) 1 : Update AMB Data to a FIFO	0x0
0xBA	[7]	SEQ0_DC_EXTEND_OFF	PPG data extension options by DAC (area SEQ0) 0 : Extension (default) 1 : disable	0x0
0xBC	[7]	SEQ1_DC_EXTEND_OFF	PPG data extension options by DAC (area SEQ1) 0 : Extension (default) 1 : disable	0x0
0xBE	[7]	SEQ2_DC_EXTEND_OFF	PPG data extension options by DAC (area SEQ2) 0 : Extension (default) 1 : disable	0x0
0xFA	[7:0]	CHIP_ID[7:0]	Read-Only These bits can read the Device identification.	0xA3

10. Package Outline Dimensions Information and Recommend Land Pattern Layout

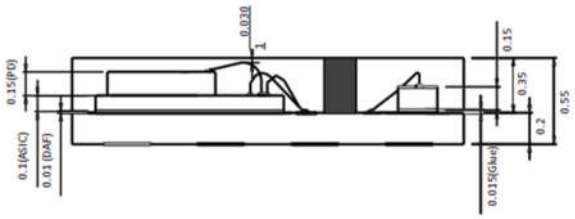
Top View



Bottom View



Side View



11. Revision History

Version	Date	Change Content
Ver0.1	2025/04	Preliminary Version

SENSYLINK

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