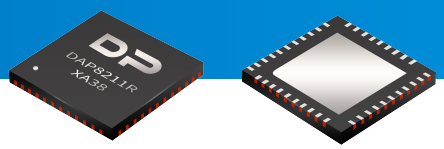
Ethernet Transceiver - DAP8211R

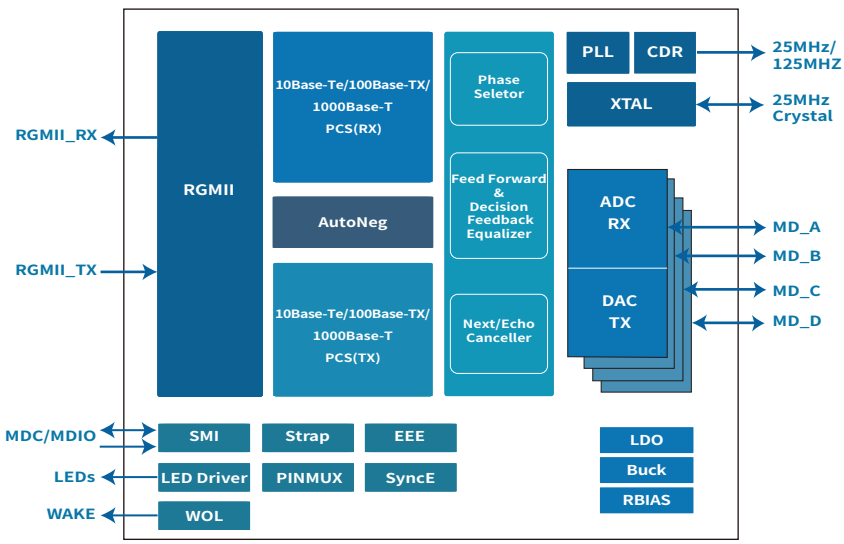
Ethernet PHY chip is an Ethernet physical layer transceiver, which modulates and demodulates the optoelectronic signal and synchronizes the clock. It is the channel for the Ethernet MAC chip to send and receive data.



Key Features

- RGMII MAC interface
- 1000BASE-T IEEE 802.3ab /100BASE-TX IEEE 802.3u/10BASE-Te IEEE 802.3 Compliant
- EEE(IEEE 802.3az-2010)
- Supports SyncE
- WoL (Wake-on-LAN)
- Sleep Mode
- Crossover Detection & Auto-Correction
- Supports Parallel Detection
- Supports Base Line Wander Correction
- Supports Interrupt function
- Automatic polarity correction
- Integrate Linear/Buck Switching Regulator
- 120 meters at 1000Mbps over CAT.5E cable
- Configurable I/O voltage (3.3 V, 2.5 V, 1.8 V) signaling for RGMII
- 3.3V single power supply
- 3 LEDs for Network Status
- 25MHz external crystal/oscillator
- Output 25MHz/125MHz clock for MAC
- Operation Temperature Range: 0℃ ~ +70℃
- Package: QFN 40-pin (5mm x 5mm)

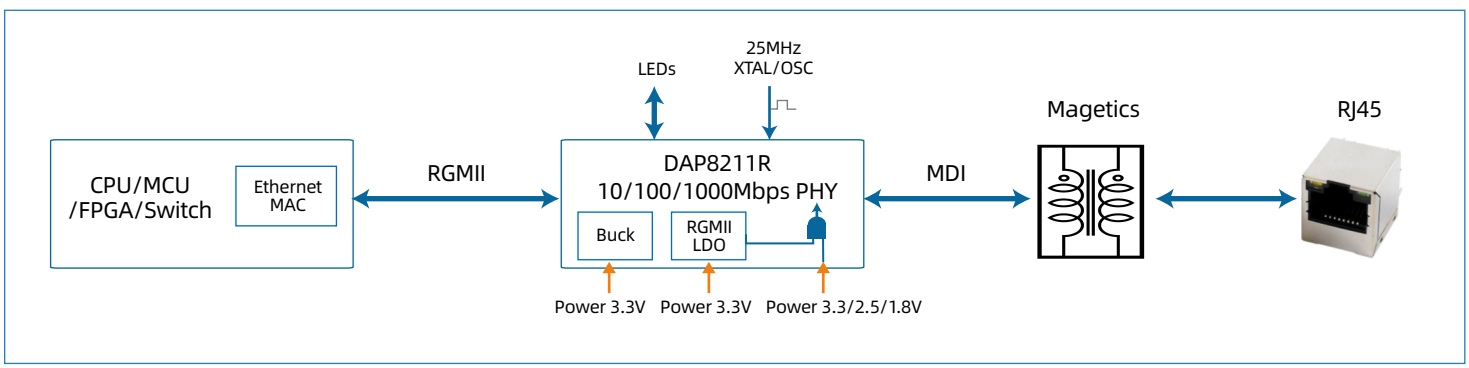
Architecture



Application

- **DTV (Digital TV)**
- **MAU (Media Access Unit)**
- **Game Console**
- **Printer and Office Machine**
- **CNR (Communication and Network Riser)**
- **LED Display, DVD Player and Recorder**
- **Ethernet Hub, Ethernet Switch**

Application Diagram



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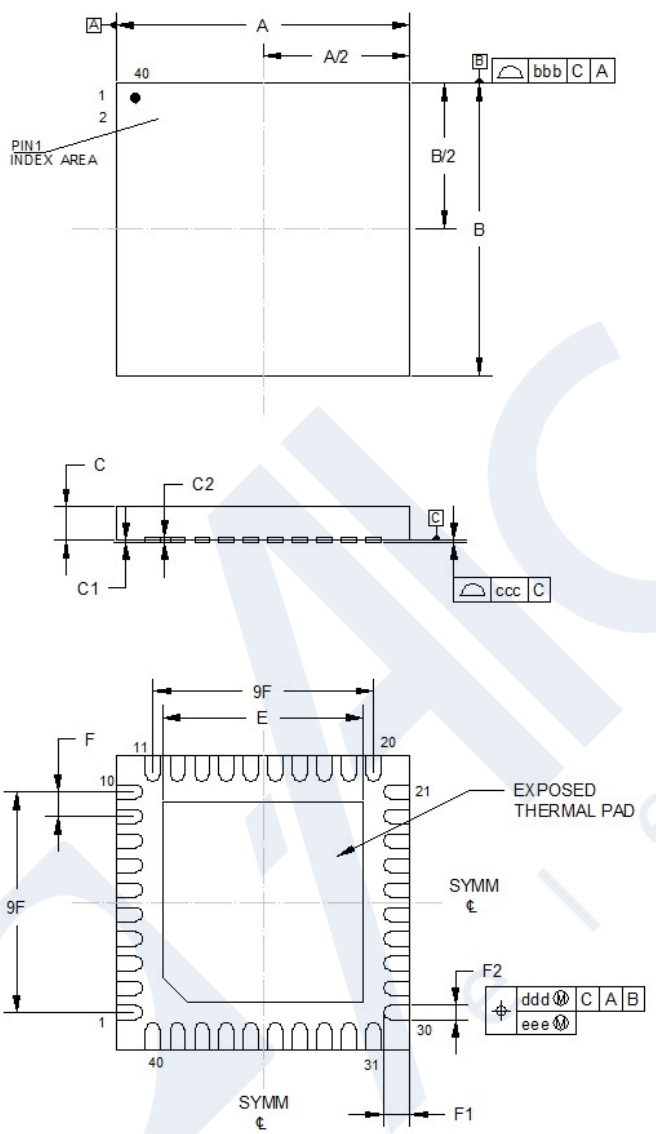
Product Number

PN	RGMII to Copper	1000Base -T	100Base -TX	10Base -Te	WoL	SyncE	EEE	Operation Temp.	Integrated Regulator	Package
DAP8211R	●	●	●	●	●	●	●	0℃ ~ +70℃	Buck	QFN40

Mechanical Dimensions



Dimension	Min.	Typ.	Max.
A	4.90	5.00	5.10
B	4.90	5.00	5.10
C	0.80	0.85	0.90
C1	--	0.02	0.05
C2	--	0.20	--
E	3.50	3.70	3.90
F	0.40BSC		
F1	0.30	0.40	0.50
F2	0.15	0.20	0.25

(Unit: mm)