ARM® Cortex®-M
32-bit Microcontroller

KM1M7BF00/02 Series
Data Sheet

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1. Overview

1.1 Overview

The KM1M7 function is a 32-bit micro controller with internal Flash memory. It is intended for development of the C programming language with object-oriented program and is easy to use. It has fast feedback processing required for control of power supply and motor.

This LSI adopts the Arm Cortex-M7 to the 32-bit micro controller part and are equipped with internal memory(Flash and RAM) to instruction / data, DMA controller, clock generator, bus controller, interrupt controller, standard peripheral circuits (timer and serial interface and so on), PWM control circuit specialized for power supply and motor control, and high accuracy / high speed analog circuit.

As system safety design, this LSI has the various safety mechanisms (Memory-ECC, clock error detection, power supply voltage detection, window watchdog timer, etc.).

1.2 Product Summary

The LSI shown in Table 1.2-1 is described in this manual.

Table 1.2-1 Product Summary

LSI series	LSI product number	Pins	ROM [KB]		RAM [KB]		VGA	Package
			Instruction	Data	Instruction	Data		
KM1M7BF0 series	KM1M7BF00N	144	512	64	64	64	O	144 pins HQFP 20 mm x 20 mm
	KM1M7BF00M		384			48		
	KM1M7BF00K		256			32		
	KM1M7BF02N	100	512			64		100pins HQFP 14 mm x 14 mm
	KM1M7BF02M		384			48		
	KM1M7BF02K		256			32		

1.2.1 Function Summary

Table 1.2-2 shows the functions of each product.

Table 1.2-2 The List of Function

Function		144 pins	100 pins
CPU		Arm Cortex-M7	
General purpose pin		123	82
Operation mode	Active mode	NORMAL	
	Standby mode	SLEEP, DEEPSLEEP	
Debugger I/F	Interface	SWD	
DMA	Module/CH number	2 / 16	
Interrupt	External interrupt	20	18
Timer	16-bit timer (timer 0 to 13)	14	
	16-bit timer (timer 20 to 25)	6	
	Power control PWM (GPWM 0 to B)	12	10
Noise filter	Target pin	External interrupt, Timer input	
Communication I/F	Clock synchronous/IIC (serial 0)	1	
	Clock synchronous/UART/LIN (serial 1)	1	
	Clock synchronous/UART (serial 2, 5, 6)	3	2
	Clock synchronous/SPI/UART (serial 3 ,4)	2	
	Clock synchronous/SPI/ UART/IIC (serial 7)	1	
	SM Bus	1	-
12-bit A/D	AD0 CH number	16	12
	AD1 CH number	16	11
	AD2 CH number	16	13
	Total CH number	32	23
Programmable gain amplifi-er(VGA)	Module number/CH number	5 / 5	
Comparator	Module number/CH number	10 / 5	
8-bit D/A	Module number	10 (for generating comparator reference voltage) 5 (for generating VGA reference voltage)	
10-bit D/A	Module number/CH number	2 / 2	

Function		144 pins	100 pins
Safety function	Flash memory	ECC, Data protection	
	RAM	ECC	
	Access area	MPU (Area management, Protection), Register protect (Protection)	
	System	Window watchdog timer	
	Clock	Clock monitoring (External oscillation, PLL error detection)	
	Communication	CRC caluculation function	
	A/D converter	A/D converter error detection	
	Power supply voltage	POR, Power supply voltage detection	
	Reset	Detection of reset factor immediately before by reset factor register	

1.3 Features

The features of this LSI are described.

Functions	Features
CPU	- Arm Cortex-M7 Equipped with FPU: Double precision floating point unit, IEEE754 compliant Equipped with MPU: Memory protect unit, 16 area can be set - Cache Instruction: 4 KB, Data: 4 KB
Memory	- ROM access I-FLASH area: 160 MHz 2 wait access D-FLASH area: 160 MHz 8 wait access - RAM access ITCM/DTCM area: 160 MHz No-wait access
Clock	- Base clock(BASECLK) External oscillation (4 to 20 MHz), Internal oscillation(10 MHz) Multiplication by PLL circuit - CPU clock(CPUCLK) 1 to 8 dividing of base clock - Peripheral clock(IOCLK) 2 to 16 dividing of CPU clock Clock operation/stop can be selected for each peripheral module
Reset	- Hardware reset Power-on reset - System reset Reset by external pin(NRST) Reset by register setting Reset by error detection(WDT overflow, Clock error detection) - CPU generation reset Reset by writing to AIRCR, Reset by CPU Lockup - Reset factor can be monitored
Low power consumption	- SLEEP mode: Stop CPU clock only - DEEP SLEEP mode: Stop clocks including BASECLK
Interrupt	- Interrupt level: 16 levels - External interrupt: High/Low level, Rising/Falling/Both edge
DMA	- Transfer mode: Single word transfer mode, Burst transfer mode - Transfer unit: 8 bits/16 bits/32 bits - Maximum transfer count: 65535 words - Transfer factor: External interrupt, Peripheral module factor - Register reload count: Maximum 65535 times - Interrupt: DMA completion, reload count completion, bus error, transfer request overflow, invalid DMA transfer request
Noise filter	- External interrupt, sampling type noise filter is inserted to timer input - Select sampling clock

Functions	Features
16-bit timer (timer 0 to timer 13)	- Interval timer count, Event count, Up-down pulse count, Phase difference pulse count - Timer Output, PWM/complement Output(wave mode: saw-tooth waves), 1-shot Output - Input capture by external input - Timer count start by start trigger - A/D conversion start trigger Output(only for timer 0 to 2) - 32-bit cascade connection - Output protection: High/Low/Hi-z Output can be selected - Timer interrupt Output control
16-bit timer (timer 20 to timer 25)	- Interval timer count, Event count, Up-down pulse count, Phase difference pulse count - Timer Output, PWM/Complementary PWM Output (Wave mode: saw-tooth waves), 1-shot Output - Input capture by external input - Timer count start by start trigger - A/D conversion start trigger Output - 32-bit cascade connection - Output protection: H/L/Hi-z Output can be selected, reading edge blanking can be set - Timer interrupt Output control - Task overflow detection function - PWM Output: Dead time insert, Output shift, Duty cut, Period cut
Power control PWM (GPWM0 to GPWMB)	- Complementary PWM Output (Wave mode: Triangular and saw-tooth waves) - Dead time insert, Output shift, H/L level Output can be set - Synchronous A/D conversion trigger - Interrupt Output control - Output protection: H/L/Hi-z Output can be select - Duty cut, period cut - Double buffer update
Synchronous SIF/SPI	- 2-wire/3-wire(4-wire can be selected only at serial 3, 4, 7) - Transfer bits(2 bits to 8 bits) - MSB/LSB transfer - Clock polarity selection - Continuous communication - Output level after the final bit transmission(H/L/final data) - Maximum transfer rate: 5.0 Mbps, 10 Mbps(only for serial 7 master)
UART	- 1-wire/2-wire - Character bits(7-bit/8-bit) - Stop bits(1-bit/2-bit) - Parity bit: Enabled/Disabled, Parity bit type: 0/1/Even parity/Odd parity - MSB/LSB transfer - Maximum transfer rate: 2.5 Mbps, 3.3 Mbps(only for serial 7) - Output communication data which corresponding AMI driver IC(only for serial 5)
IIC	- Master/Slave communication - Start condition selection: Enable/Disable - MSB/LSB transfer selection - Transfer format: 7-bit address format, 10-bit address format(only for serial 7) - Maximum transfer rate: Standard Mode: 100 kbps, Fast Mode: 400 kbps, Fast Mode Plus: 1 Mbps(only for serial 7)
SMBus interface	- Conform to System Management Bus v2.0 - Timeout detection, Packet error detection - Return from CPU standby mode by detecting start condition - Maximum transfer rate: 100 kHz

Functions	Features
LIN controller	- Master/Slave communication - Wake Up signal transmission/reception - Synch Break field transmission/reception - Synch field transmission/reception - ID field transmission/reception - Error detection: Check sum error, Bit error, Timeout
12-bit A/D	- Timer 20 to 25, GPWM0 to B etc can be started synchronously - Conversion error detection - Conversion state Output - Start trigger reduction function
VGA	- Gain selection(1, 2, 3, 4, 5, 6, 8, 10, 20 times) - Set Output offset voltage by 8-bit DAC - Offset cancellation by input Short-circuit
Comparator	- Hysteresis ON/OFF - Set reference voltage by 8-bit DAC - Sampling type noise filter is inserted to comparator Output
8-bit D/A	- VGA Output offset voltage can be generated - Comparator reference voltage can be generated
10-bit D/A	- Output the set DC voltage
Multi feedback assist	- Set the start timing of timer 20 to 25, GPWM 0 to B individually - Detect/Automatically avoid the competition of timer 20 to 25, GPWM 0 to B and AD conversion start - Mask(Blanking) the external interrupt detection, comparator of GPWM0 to B Output
CRC caluculation	- CRC-32, CRC-16-CCITT, CRC-16, CRC-8-ATM symbol can be generated
Safety function	- ECC function Check area: Cache, I-FLASH, D-FLASH, ITCM, DTCM, Message RAM for CAN 1 bit correction, 2 bit random error detection - Flash Erase/Program protect function - Function to protect write access to main register - Clock monitor function - Window watchdog timer(internal oscillation count) - Power supply voltage detection - ADC fault diagnosis function which is used for internal power supply

1.4 Pins

The specifications of pins in this LSI are described as follows.

- Pin configuration
- Pin function

1.4.1 Pin Configuration

Figure 1.4-1 shows the pin configuration of 144 pins.

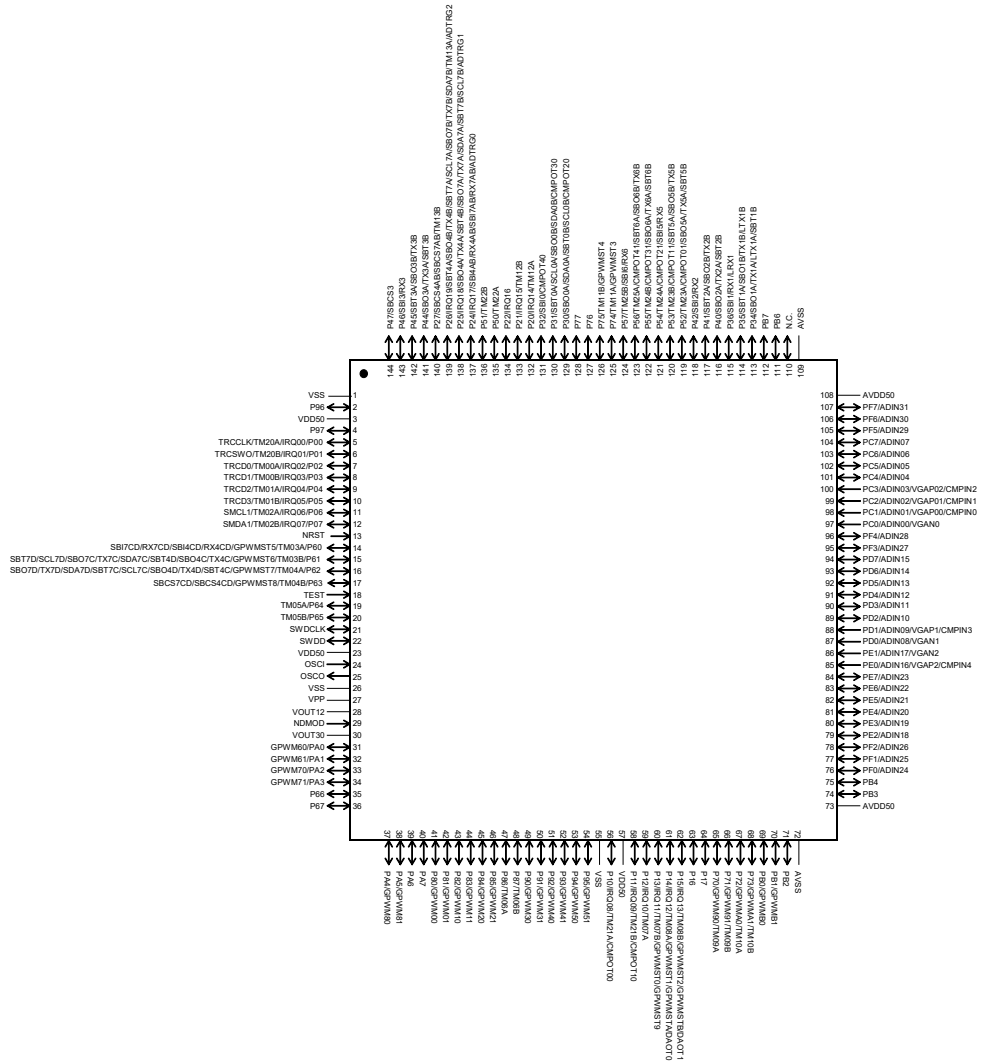

Figure 1.4-1 Pin Configuration Figure of 144 pins

Figure 1.4-2 shows the pin configuration of 100 pins.

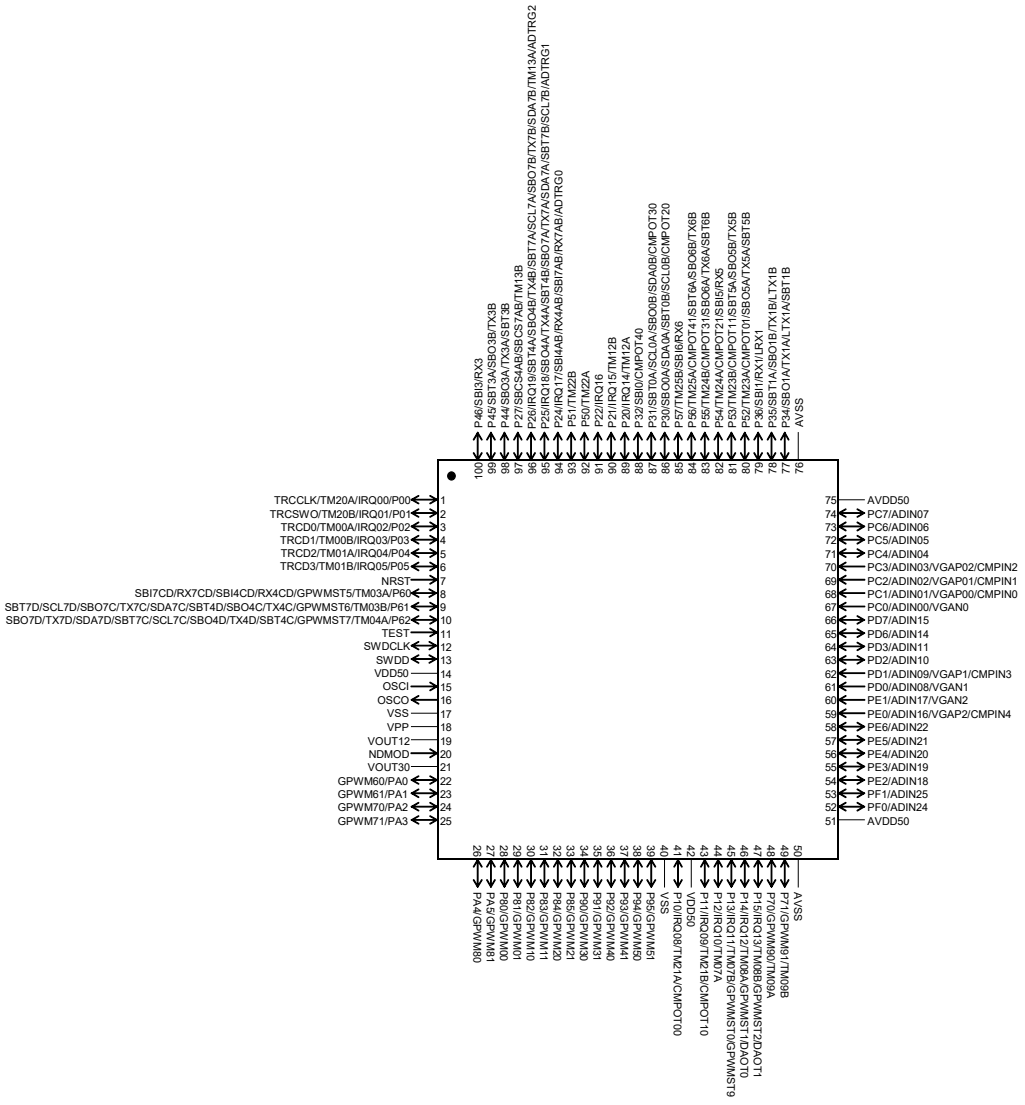

Figure 1.4-2 Pin Configuration Figure of 100 pins

1.4.2 Pin Functions

The pin functions are listed in Table 1.4-1 .

Table 1.4-1 Pin Functions

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
External power pin	VDD50	3 23 57	14 42	Input	-
Power pin for analog	AVDD50	73 108	51 75	Input	-
Power pin for internal circuit	VOUT30	30	21	Output	-
	VOUT12	28	19	Output	-
GND	VSS	1 26 55	17 40	Input	-
GND for analog	AVSS	72 109	50 76	Input	-
Debugger	NDMOD	29	20	Input	-
	SWDCLK	21	12	Input	-
	SWDD	22	13	I/O	-
	TRCCLK	5	1	Output	P00/IRQ00/TM20A
	TRCSWO	6	2	Output	P01/IRQ01/TM20B
	TRCD0	7	3	Output	P02/IRQ02/TM00A
	TRCD1	8	4	Output	P03/IRQ03/TM00B
	TRCD2	9	5	Output	P04/IRQ04/TM01A
	TRCD3	10	6	Output	P05/IRQ05/TM01B
External oscillation Input pin	OSCI	24	15	Input	-
External oscillation Output pin	OSCO	25	16	Output	-
Reset	NRST	13	7	Input	-
Mode pin	TEST	18	11	Input	-
Input pin for flash memory	VPP	27	18	Input	-
External interrupt	IRQ00	5	1	Input	P00//TM20A/TRCCLK
	IRQ01	6	2	Input	P01/TM20B/TRCSWO
	IRQ02	7	3	Input	P02/TM00A/TRCD0
	IRQ03	8	4	Input	P03/TM00B/TRCD1
	IRQ04	9	5	Input	P04/TM01A/TRCD2
	IRQ05	10	6	Input	P05/TM01B/TRCD3
	IRQ06	11	-	Input	P06/TM02A/SMCL1
	IRQ07	12	-	Input	P07/TM02B/SMDA1
	IRQ08	56	41	Input	P10/TM21A/CMPOT00
	IRQ09	58	43	Input	P11/TM21B/CMPOT10
	IRQ10	59	44	Input	P12/TM07A
	IRQ11	60	45	Input	P13/TM07B/GPWMST0/GPWMST9

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
External interrupt	IRQ12	61	46	Input	P14/TM08A/GPWMST1/GPWMSTA /DAOT0
	IRQ13	62	47	Input	P15/TM08B/GPWMST2/GPWMSTB /DAOT1
	IRQ14	132	89	Input	P20/TM12A
	IRQ15	133	90	Input	P21/TM12B
	IRQ16	134	91	Input	P22
	IRQ17	137	94	Input	P24/SBI4AB/RX4AB/SBI7AB /RX7AB/ADTRG0
	IRQ18	138	95	Input	P25/SBO4A/TX4A/SBT4B /SBO7A/TX7A/SDA7A/SBT7B /SCL7B/ADTRG1
	IRQ19	139	96	Input	P26/SBT4A/SBO4B/TX4B /SBT7A/SCL7A/SBO7B/TX7B /SDA7B/TM13A/ADTRG2
16-bit timer	TM00A	7	3	I/O	P02/IRQ02/TRCD0
	TM00B	8	4	I/O	P03/IRQ03/TRCD1
	TM01A	9	5	I/O	P04/IRQ04/TRCD2
	TM01B	10	6	I/O	P05/IRQ05/TRCD3
	TM02A	11	-	I/O	P06/IRQ06/SMCL1
	TM02B	12	-	I/O	P07/IRQ07/SMDA1
	TM03A	14	8	I/O	P60/GPWMST5/RX4CD/SBI4CD /RX7CD/SBI7CD
	TM03B	15	9	I/O	P61/GPWMST6/TX4C/SBO4C /SBT4D/SBO7C/TX7C/SDA7C /SBT7D/SCL7D
	TM04A	16	10	I/O	P62/GPWMST7/SBT4C/TX4D /SBO4D/SBT7C/SCL7C/SBO7D /TX7D/SDA7D
	TM04B	17	-	I/O	P63/GPWMST8/SBCS4CD/SBCS7CD
	TM05A	19	-	I/O	P64
	TM05B	20	-	I/O	P65
	TM06A	47	-	I/O	P86
	TM06B	48	-	I/O	P87
	TM07A	59	44	I/O	P12/IRQ10
	TM07B	60	45	I/O	P13/IRQ11/GPWMST0/GPWMST9
	TM08A	61	46	I/O	P14/IRQ12/GPWMST1/GPWMSTA /DAOT0
	TM08B	62	47	I/O	P15/IRQ13/GPWMST2/GPWMSTB /DAOT1
	TM09A	65	48	I/O	P70/GPWM90
	TM09B	66	49	I/O	P71/GPWM91
	TM10A	67	-	I/O	P72/GPWMA0
	TM10B	68	-	I/O	P73/GPWMA1
	TM11A	125	-	I/O	P74/GPWMST3
	TM11B	126	-	I/O	P75/GPWMST4
	TM12A	132	89	I/O	P20/IRQ14
	TM12B	133	90	I/O	P21/IRQ15

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
16-bit timer	TM13A	139	96	I/O	P26/IRQ19/SBT4A/SBO4B /TX4B/SBT7A/SCL7A/SBO7B /TX7B/SDA7B/ADTRG2
	TM13B	140	97	I/O	P27/SBCS4AB/SBCS7AB
	TM20A	5	1	I/O	P00/IRQ00/TRCCLK
	TM20B	6	2	I/O	P01/IRQ01/TRCSWO
	TM21A	56	41	I/O	P10/IRQ08/CMPOT00
	TM21B	58	43	I/O	P11/IRQ09/CMPOT10
	TM22A	135	92	I/O	P50
	TM22B	136	93	I/O	P51
	TM23A	119	80	I/O	P52/CMPOT01/SBO5A/TX5A /SBT5B
	TM23B	120	81	I/O	P53/CMPOT11/SBT5A/SBO5B /TX5B
	TM24A	121	82	I/O	P54/CMPOT21/SBI5/RX5
	TM24B	122	83	I/O	P55/CMPOT31/SBO6A/TX6A /SBT6B
	TM25A	123	84	I/O	P56/CMPOT41/SBT6A/SBO6B /TX6B
	TM25B	124	85	I/O	P57/SBI6/RX6
Power control PWM pin	GPWM00	41	28	Output	P80
	GPWM01	42	29	Output	P81
	GPWM10	43	30	Output	P82
	GPWM11	44	31	Output	P83
	GPWM20	45	32	Output	P84
	GPWM21	46	33	Output	P85
	GPWM30	49	34	Output	P90
	GPWM31	50	35	Output	P91
	GPWM40	51	36	Output	P92
	GPWM41	52	38	Output	P93
	GPWM50	53	38	Output	P94
	GPWM51	54	39	Output	P95
	GPWM60	31	22	Output	PA0
	GPWM61	32	23	Output	PA1
	GPWM70	33	24	Output	PA2
	GPWM71	34	25	Output	PA3
	GPWM80	37	26	Output	PA4
	GPWM81	38	27	Output	PA5
	GPWM90	65	48	Output	P70/TM09A
	GPWM91	66	49	Output	P71/TM09B
	GPWMA0	67	-	Output	P72/TM10A
	GPWMA1	68	-	Output	P73/GPWMA1/TM10B
	GPWMB0	69	-	Output	PB0
	GPWMB1	70	-	Output	PB1
Power control PWM monitor	GPWMST0	60	45	Output	P13/IRQ11/TM07B/GPWMST9

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
Power control PWM monitor	GPWMST1	61	46	Output	P14/IRQ12/TM08A/GPWMSTA /DAOT0
	GPWMST2	62	47	Output	P15/IRQ13/TM08B/GPWMSTB /DAOT1
	GPWMST3	125	-	Output	P74/TM11A
	GPWMST4	126	-	Output	P75/TM11B
	GPWMST5	14	8	Output	P60/TM03A/RX4CD/SBI4CD /RX7CD/SBI7CD
	GPWMST6	15	9	Output	P61/TM03B/TX4C/SBO4C /SBT4D/SBO7C/TX7C/SDA7C /SBT7D/SCL7D
	GPWMST7	16	10	Output	P62/TM04A/SBT4C/TX4D /SBO4D/SBT7C/SCL7C/SBO7D /TX7D/SDA7D
	GPWMST8	17	-	Output	P63/TM04B/SBCS4CD/SBCS7CD
	GPWMST9	60	45	Output	P13/IRQ11/TM07B/GPWMST0
	GPWMSTA	61	-	Output	P14/IRQ12/TM08A/GPWMST1 /DAOT0
	GPWMSTB	62	-	Output	P15/IRQ13/TM08B/GPWMST2 /DAOT1
Clock Synchro-nous SIF/SPI	SBO0A	129	86	I/O	P30/SDA0A/SBT0B/SCL0B /CMPOT20
	SBT0A	130	87	I/O	P31/SCL0A/SBO0B/SDA0B /CMPOT30
	SBO0B	130	87	I/O	P31/SBT0A/SCL0A/SDA0B /CMPOT30
	SBT0B	129	86	I/O	P30/SBO0A/SDA0A/SCL0B /CMPOT20
	SBI0	131	88	Input	P32/CMPOT40
	SBO1A	113	77	I/O	P34/TX1A/LTX1A/SBT1B
	SBT1A	114	78	I/O	P35/SBO1B/TX1B/LTX1B
	SBO1B	114	78	I/O	P35/SBT1A/TX1B/LTX1B
	SBT1B	113	77	I/O	P34/SBO1A/TX1A/LTX1A
	SBI1	115	79	Input	P36/RX1/LRX1
	SBO2A	116	-	I/O	P40/TX2A/SBT2B
	SBT2A	117	-	I/O	P41/SBO2B/TX2B
	SBO2B	117	-	I/O	P41/SBT2A/TX2B
	SBT2B	116	-	I/O	P40/SBO2A/TX2A
	SBI2	118	-	Input	P42/RX2
	SBCS3	144	-	Output	P47
	SBO3A	141	98	I/O	P44/TX3A/SBT3B
	SBT3A	142	99	I/O	P45/SBO3B/TX3B
	SBO3B	142	99	I/O	P45/SBT3A/TX3B
	SBT3B	141	98	I/O	P44/SBO3A/TX3A
	SBI3	143	100	I/O	P46/RX3
	SBCS4AB	140	97	Input	P27/SBCS7AB/TM13B
	SBO4A	138	95	I/O	P25/IRQ18/TX4A/SBT4B /SBO7A/TX7A/SDA7A/SBT7B SCL7B/ADTRG1

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
Clock Synchro-nous SIF/SPI	SBT4A	139	96	I/O	P26/IRQ19/SBO4B/TX4B /SBT7A/SCL7A/SBO7B/TX7B /SDA7B/TM13A/ADTRG2
	SBO4B	139	96	I/O	P26/IRQ19/SBT4A/TX4B /SBT7A/SCL7A/SBO7B/TX7B /SDA7B/TM13A/ADTRG2
	SBT4B	138	95	I/O	P25/IRQ18/SBO4A/TX4A /SBO7A/TX7A/SDA7A/SBT7B /SCL7B/ADTRG1
	SBI4AB	137	94	Input	P24/IRQ17/RX4AB/SBI7AB /RX7AB/ADTRG0
	SBCS4CD	17	-	Input	P63/TM04B/GPWMST8/SBCS7CD
	SBO4C	15	9	I/O	P61/TM03B/GPWMST6/TX4C /SBT4D/SBO7C/TX7C/SDA7C /SBT7D/SCL7D
	SBT4C	16	10	I/O	P62/TM04A/GPWMST7/TX4D /SBO4D/SBT7C/SCL7C/SBO7D /TX7D/SDA7D
	SBO4D	16	10	I/O	P62/TM04A/GPWMST7/SBT4C /TX4D/SBT7C/SCL7C/SBO7D /TX7D/SDA7D
	SBT4D	15	9	I/O	P61/TM03B/PWMST6/TX4C /SBO4C/SBO7C/TX7C/SDA7C /SBT7D/SCL7D
	SBI4CD	14	8	Input	P60/TM03A/GPWMST5/RX4CD /RX7CD/SBI7CD
	SBO5A	119	80	I/O	P52/TM23A/CMPOT01/TX5A /SBT5B
	SBT5A	120	81	I/O	P53/TM23B/CMPOT11/SBO5B /TX5B
	SBO5B	120	81	I/O	P53/TM23B/CMPOT11/SBT5A /TX5B
	SBT5B	119	80	I/O	P52/TM23A/CMPOT01/SBO5A /TX5A
	SBI5	121	82	Input	P54/TM24A/CMPOT21/RX5
	SBO6A	122	83	I/O	P55/TM24B/CMPOT31/TX6A /SBT6B
	SBT6A	123	84	I/O	P56/TM25A/CMPOT41/SBO6B /TX6B
	SBO6B	123	84	I/O	P56/TM25A/CMPOT41/SBT6A /TX6B
	SBT6B	122	83	I/O	P55/TM24B/CMPOT31/SBO6A /TX6A
	SBI6	124	85	Input	P57/TM25B/RX6
	SBCS7AB	140	97	Input	P27/SBCS4AB/TM13B
	SBO7A	138	95	I/O	P25/IRQ18/SBO4A/TX4A /SBT4B/TX7A/SCL7A/SBT7B SCL7B/ADTRG1
	SBT7A	139	96	I/O	P26/IRQ19/SBT4A/SBO4B /TX4B/SCL7A/SBO7B/TX7B /SDA7B/TM13A/ADTRG2
	SBO7B	139	96	I/O	P26/IRQ19/SBT4A/SBO4B /TX4B/SBT7A/SCL7A/TX7B /SDA7B/TM13A/ADTRG2

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
Clock Synchro-nous SIF/SPI	SBT7B	138	95	I/O	P25/IRQ18/SBO4A/TX4A /SBT4B/SBO7A/TX7A/SDA7A /SCL7B/ADTRG1
	SBI7AB	137	94	Input	P24/IRQ17/SBI4AB/RX4AB /RX7AB/ADTRG0
	SBCS7CD	17	-	Input	P63/TM04B/GPWMST8/SBCS4CD
	SBO7C	15	9	I/O	P61/TM03B/GPWMST6/TX4C /SBO4C/SBT4D/TX7C/SDA7C /SBT7D/SCL7D
	SBT7C	16	10	I/O	P62/TM04A/GPWMST7/SBT4C /TX4D/SBO4D/SCL7C/SBO7D /TX7D/SDA7D
	SBO7D	16	10	I/O	P62/TM04A/GPWMST7/SBT4C /TX4D/SBO4D/SBT7C/SCL7C /TX7D/SDA7D
	SBT7D	15	9	I/O	P61/TM03B/GPWMST6/TX4C /SBO4C/SBT4D/SBO7C/TX7C /SCL7D
	SBI7CD	14	8	Input	P60/TM03A/GPWMST5/RX4CD /SBI4CD/RX7CD
UART	TX1A	113	77	I/O	P34/SBO1A/LTX1A/SBT1B
	TX1B	114	78	I/O	P35/SBT1A/SBO1B/LTX1B
	RX1	115	79	Input	P36/SBI1/LRX1
	TX2A	116	-	I/O	P40/SBO2A/SBT2B
	TX2B	117	-	I/O	P41/SBT2A/SBO2B
	RX2	118	-	Input	P42/SBI2
	TX3A	141	98	I/O	P44/SBO3A/SBT3B
	TX3B	142	99	I/O	P45/SBT3A/SBO3B
	RX3	143	100	Input	P46/SBI3
	TX4A	138	95	I/O	P25/IRQ18/SBO4A/SBT4B /SBO7A/TX7A/SDA7A/SBT7B /SCL7B/ADTRG1
	TX4B	139	96	I/O	P26/IRQ19/SBT4A/SBO4B /SBT7A/SCL7A/SBO7B/TX7B /SDA7B/TM13A/ADTRG2
	RX4AB	137	94	Input	P24/IRQ17/SBI4AB/SBI7AB /RX7AB/ADTRG0
	TX4C	15	9	I/O	P61/TM03B/GPWMST6/SBO4C /SBT4D/SBO7C/TX7C/SDA7C /SBT7D/SCL7D
	TX4D	16	10	I/O	P62/TM04A/GPWMST7/SBT4C /SBO4D/SBT7C/SCL7C/SBO7D /TX7D/SDA7D
	RX4CD	14	8	Input	P60/TM03A/GPWMST5/SBI4CD /RX7CD/SBI7CD
	TX5A	119	80	I/O	P52/TM23A/CMPOT01/SBO5A /SBT5B
	TX5B	120	81	I/O	P53/TM23B/CMPOT11/SBT5A /SBO5B
	RX5	121	82	Input	P54/TM24A/CMPOT21/SBI5
	TX6A	122	83	I/O	P55/TM24B/CMPOT31/SBO6A /SBT6B
	TX6B	123	84	I/O	P56/TM25A/CMPOT41/SBT6A /SBO6B
	RX6	124	85	Input	P57/TM25B/SBI6

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
UART	TX7A	138	95	I/O	P25/IRQ18/SBO4A/TX4A /SBT4B/SBO7A/SDA7A/SBT7B /SCL7B/ADTRG1
	TX7B	139	96	I/O	P26/IRQ19/SBT4A/SBO4B /TX4B/SBT7A/SCL7A/SBO7B /SDA7B/TM13A/ADTRG2
	RX7AB	137	94	Input	P24/IRQ17/SBI4AB/RX4AB /SBI7AB/ADTRG0
	TX7C	15	9	I/O	P61/TM03B/GPWMST6/TX4C /SBO4C/SBT4D/SBO7C/SDA7C /SBT7D/SCL7D
	TX7D	16	10	I/O	P62/TM04A/GPWMST7/SBT4C /TX4D/SBO4D/SBT7C/SCL7C /SBO7D/SCL7D
	RX7CD	14	8	Input	P60/TM03A/GPWMST5/RX4CD /SBI4CD/SBI7CD
LIN	LTX1A	113	77	Output	P34/SBO1A/TX1A/SBT1B
	LTX1B	114	78	Output	P35/SBT1A/SBO1B/TX1B
	LRX1	115	79	Input	P36/SBI1/RX1
IIC	SDA0A	129	86	I/O	P30/SBO0A/SBT0B/SCL0B /CMPOT20
	SCL0A	130	87	I/O	P31/SBT0A/SBO0B/SDA0B /CMPOT30
	SDA0B	130	87	I/O	P31/SBT0A/SCL0A/SBO0B /CMPOT30
	SCL0B	129	86	I/O	P30/SBO0A/SDA0A/SBT0B /CMPOT20
	SDA7A	138	95	I/O	P25/IRQ18/SBO4A/TX4A /SBT4B/SBO7A/TX7A/SBT7B /SCL7B/ADTRG1
	SCL7A	139	96	I/O	P26/IRQ19/SBT4A/SBO4B /TX4B/SBT7A/SBO7B/TX7B /SDA7B/TM13A/ADTRG2
	SDA7B	139	96	I/O	P26/IRQ19/SBT4A/SBO4B /TX4B/SBT7A/SCL7A/SBO7B /TX7B/TM13A/ADTRG2
	SCL7B	138	95	I/O	P25/IRQ18/SBO4A/TX4A /SBT4B/SBO7A/TX7A/SDA7A /SBT7B/ADTRG1
	SDA7C	15	9	I/O	P61/TM03B/GPWMST6/SBO4C /TX4C/SBT4D/SBO7C/TX7C /SBT7D/SCL7D
	SCL7C	16	10	I/O	P62/TM04A/GPWMST7/SBT4C /SBO4D/TX4D/SBT7C/SBO7D /TX7D/SDA7D
	SDA7D	16	10	I/O	P62/TM04A/GPWMST7/SBT4C /SBO4D/TX4D/SBT7C/SCL7C /SBO7D/TX7D
	SCL7D	15	9	I/O	P61/TM03B/GPWMST6/SBO4C /TX4C/SBT4D/SBO7C/TX7C /SDA7C/SBT7D
SM Bus	SMDA1	12	-	I/O	P07/IRQ07/TM02B
	SMCL1	11	-	I/O	P06/IRQ06/TM02A

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
A/D Input	ADIN00	97	67	Input	PC0/VGAN0
	ADIN01	98	68	Input	PC1/VGAP00/CMPIN0
	ADIN02	99	69	Input	PC2/VGAP01/CMPIN1
	ADIN03	100	70	Input	PC3/VGAP02/CMPIN2
	ADIN04	101	71	Input	PC4
	ADIN05	102	72	Input	PC5
	ADIN06	103	73	Input	PC6
	ADIN07	104	74	Input	PC7
	ADIN08	87	61	Input	PD0/VGAN1
	ADIN09	88	62	Input	PD1/VGAP1/CMPIN3
	ADIN10	89	63	Input	PD2
	ADIN11	90	64	Input	PD3
	ADIN12	91	-	Input	PD4
	ADIN13	92	-	Input	PD5
	ADIN14	93	65	Input	PD6
	ADIN15	94	66	Input	PD7
	ADIN16	85	59	Input	PE0/VGAP2/CMPIN4
	ADIN17	86	60	Input	PE1/VGAN2
	ADIN18	79	54	Input	PE2
	ADIN19	80	55	Input	PE3
	ADIN20	81	56	Input	PE4
	ADIN21	82	57	Input	PE5
	ADIN22	83	58	Input	PE6
	ADIN23	84	-	Input	PE7
	ADIN24	76	52	Input	PF0
	ADIN25	77	53	Input	PF1
	ADIN26	78	-	Input	PF2
	ADIN27	95	-	Input	PF3
	ADIN28	96	-	Input	PF4
	ADIN29	105	-	Input	PF5
	ADIN30	106	-	Input	PF6
	ADIN31	107	-	Input	PF7
A/D monitor	ADTRG0	137	94	Output	P24/IRQ17/SBI4AB/RX4AB /SBI7AB/RX7AB
	ADTRG1	138	95	Output	P25/IRQ18/SBO4A/TX4A /SBT4B/SBO7A/TX7A/SDA7A /SBT7B/SCL7B
	ADTRG2	139	96	Output	P26/IRQ19/SBT4A/SBO4B /TX4B/SBT7A/SCL7A/SBO7B /SDA7B/TX7B/TM13A
VGA Input	VGAP00	98	68	Input	PC1/ADIN01/CMPIN0
	VGAP01	99	69	Input	PC2/ADIN02/CMPIN1
	VGAP02	100	70	Input	PC3/ADIN03/CMPIN2
	VGAN0	97	67	Input	PC0/ADIN00
	VGAP1	88	62	Input	PD1/ADIN09/CMPIN3
	VGAN1	87	61	Input	PD0/ADIN08
	VGAP2	85	59	Input	PE0/ADIN16/CMPIN4
	VGAN2	86	60	Input	PE1/ADIN17
Comparator Input	CMPIN0	98	68	Input	PC1/ADIN01/VGAP00
	CMPIN1	99	69	Input	PC2/ADIN02/VGAP01
	CMPIN2	100	70	Input	PC3/ADIN03/VGAP02
	CMPIN3	88	62	Input	PD1/ADIN09/VGAP1
	CMPIN4	85	59	Input	PE0/ADIN16/VGAP2

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
Comparator Output	CMPOT00	56	41	Output	P10/IRQ08/TM21A
	CMPOT01	119	80	Output	P52/TM23A/SBO5A/TX5A /SBT5B
	CMPOT10	58	43	Output	P11/IRQ09/TM21B
	CMPOT11	120	81	Output	P53/TM23B/SBT5A/SBO5B /TX5B
	CMPOT20	129	86	Output	P30/SBO0A/SDA0A/SBT0B /SCL0B
	CMPOT21	121	82	Output	P54/TM24A/SBI5/RX5
	CMPOT30	130	87	Output	P31/SBT0A/SCL0A/SBO0B /SDA0B
	CMPOT31	122	83	Output	P55/TM24B/SBO6A/TX6A /SBT6B
	CMPOT40	131	88	Output	P32/SBI0
	CMPOT41	123	84	Output	P56/TM25A/SBT6A/SBO6B /TX6B
D/A Output	DAOT0	61	46	Output	P14/IRQ12/TM08A/GPWMST1 /GPWMSTA
	DAOT1	62	47	Output	P15/IRQ13/TM08B/GPWMST2 /GPWMSTB
I/O port	P00	5	1	I/O	IRQ00/TM20A/TRCCLK
	P01	6	2	I/O	IRQ01/TM20B/TRCSWO
	P02	7	3	I/O	IRQ02/TM00A/TRCD0
	P03	8	4	I/O	IRQ03/TM00B/TRCD1
	P04	9	5	I/O	IRQ04/TM01A/TRCD2
	P05	10	6	I/O	IRQ05/TM01B/TRCD3
	P06	11	-	I/O	IRQ06/TM02A/SMCL1
	P07	12	-	I/O	IRQ07/TM02B/SMDA1
	P10	56	41	I/O	IRQ08/TM21A/CMPOT00
	P11	58	43	I/O	IRQ09/TM21B/CMPOT10
	P12	59	44	I/O	IRQ10/TM07A
	P13	60	45	I/O	IRQ11/TM07B/GPWMST0/GPWMST9
	P14	61	46	I/O	IRQ12/TM08A/GPWMST1/GPWMSTA /DAOT0
	P15	62	47	I/O	IRQ13/TM08B/GPWMST2/GPWMSTB /DAOT1
	P16	63	-	I/O	-
	P17	64	-	I/O	-

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
I/O port	P20	132	89	I/O	IRQ14/TM12A
	P21	133	90	I/O	IRQ15/TM12B
	P22	134	91	I/O	IRQ16
	P24	137	94	I/O	IRQ17/SBI4AB/RX4AB/SBI7AB /RX7AB/ADTRG0
	P25	138	95	I/O	IRQ18/SBO4A/TX4A/SBT4B /SBO7A/TX7A/SDA7A/SBT7B /SCL7B/ADTRG1
	P26	139	96	I/O	IRQ19/SBT4A/SBO4B/TX4B /SBT7A/SCL7A/SBO7B/TX7B /SDA7B/TM13A/ADTRG2
	P27	140	97	I/O	SBCS4AB/SBCS7AB/TM13B
	P30	129	86	I/O	SBO0A/SDA0A/SBT0B/SCL0B /CMPOT20
	P31	130	87	I/O	SBT0A/SCL0A/SBO0B/SDA0B /CMPOT30
	P32	131	88	I/O	SBI0/CMPOT40
	P34	113	77	I/O	SBO1A/TX1A/LTX1A/SBT1B
	P35	114	78	I/O	SBT1A/SBO1B/TX1B/LTX1B
	P36	115	79	I/O	SBI1/RX1/LRX1
	P40	116	-	I/O	SBO2A/TX2A/SBT2B
	P41	117	-	I/O	SBT2A/SBO2B/TX2B
	P42	118	-	I/O	SBI2/RX2
	P44	141	98	I/O	SBO3A/TX3A/SBT3B
	P45	142	99	I/O	SBT3A/SBO3B/TX3B
	P46	143	100	I/O	SBI3/RX3
	P47	144	-	I/O	SBCS3
	P50	135	92	I/O	TM22A
	P51	136	93	I/O	TM22B
	P52	119	80	I/O	TM23A/CMPOT01/SBO5A/TX5A /SBT5B
	P53	120	81	I/O	TM23B/CMPOT11/SBT5A/SBO5B /TX5B
	P54	121	82	I/O	TM24A/CMPOT21/SBI5/RX5
	P55	122	83	I/O	TM24B/CMPOT31/SBO6A/TX6A /SBT6B
	P56	123	84	I/O	TM25A/CMPOT41/SBT6A/SBO6B /TX6B
	P57	124	85	I/O	TM25B/SBI6/RX6
	P60	14	8	I/O	TM03A/GPWMST5/RX4CD/SBI4CD /RX7CD/SBI7CD
	P61	15	9	I/O	TM03B/GPWMST6/TX4C/SBO4C /SBT4D/SBO7C/TX7C/SDA7C /SBT7D/SCL7D
	P62	16	10	I/O	TM04A/GPWMST7/SBT4C/TX4D /SBO4D/SBT7C/SCL7C/SBO7D /TX7D/SDA7D
	P63	17	-	I/O	TM04B/GPWMST8/SBCS4CD/SBCS7CD
	P64	19	-	I/O	TM05A

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
I/O port	P65	20	-	I/O	TM05B
	P66	35	-	I/O	-
	P67	36	-	I/O	-
	P70	65	48	I/O	GPWM90/TM09A
	P71	66	49	I/O	GPWM91/TM09B
	P72	67	-	I/O	GPWMA0/TM10A
	P73	68	-	I/O	GPWMA1/TM10B
	P74	125	-	I/O	TM11A/GPWMST3
	P75	126	-	I/O	TM11B/GPWMST4
	P76	127	-	I/O	-
	P77	128	-	I/O	-
	P80	41	28	I/O	GPWM00
	P81	42	29	I/O	GPWM01
	P82	43	30	I/O	GPWM10
	P83	44	31	I/O	GPWM11
	P84	45	32	I/O	GPWM20
	P85	46	33	I/O	GPWM21
	P86	47	-	I/O	TM06A
	P87	48	-	I/O	TM06B
	P90	49	34	I/O	GPWM30
	P91	50	35	I/O	GPWM31
	P92	51	36	I/O	GPWM40
	P93	52	37	I/O	GPWM41
	P94	53	38	I/O	GPWM50
	P95	54	39	I/O	GPWM51
	P96	2	-	I/O	-
	P97	4	-	I/O	-
	PA0	31	22	I/O	GPWM60
	PA1	32	23	I/O	GPWM61
	PA2	33	24	I/O	GPWM70
	PA3	34	25	I/O	GPWM71
	PA4	37	26	I/O	GPWM80
	PA5	38	27	I/O	GPWM81
	PA6	39	-	I/O	-
	PA7	40	-	I/O	-
	PB0	69	-	I/O	GPWMB0
	PB1	70	-	I/O	GPWMB1
	PB2	71	-	I/O	-
	PB3	74	-	I/O	-
	PB4	75	-	I/O	-
	PB6	111	-	I/O	-
	PB7	112	-	I/O	-
	PC0	97	67	Input	ADIN00/VGAN0

Functions	Pin name	144 pins Pin No.	100 pins Pin No.	I/O	Other Pins
I/O port	PC1	98	68	Input	ADIN01/VGAP00/CMPIN0
	PC2	99	69	Input	ADIN02/VGAP01/CMPIN1
	PC3	100	70	Input	ADIN03/VGAP02/CMPIN2
	PC4	101	71	I/O	ADIN04
	PC5	102	72	I/O	ADIN05
	PC6	103	73	I/O	ADIN06
	PC7	104	74	I/O	ADIN07
	PD0	87	61	Input	ADIN08/VGAN1
	PD1	88	62	Input	ADIN09/VGAP1/CMPIN3
	PD2	89	63	I/O	ADIN10
	PD3	90	64	I/O	ADIN11
	PD4	91	-	I/O	ADIN12
	PD5	92	-	I/O	ADIN13
	PD6	93	65	I/O	ADIN14
	PD7	94	66	I/O	ADIN15
	PE0	85	59	Input	ADIN16/VGAP2/CMPIN4
	PE1	86	60	Input	ADIN17/VGAN2
	PE2	79	54	I/O	ADIN18
	PE3	80	55	I/O	ADIN19
	PE4	81	56	I/O	ADIN20
	PE5	82	57	I/O	ADIN21
	PE6	83	58	I/O	ADIN22
	PE7	84	-	I/O	ADIN23
	PF0	76	52	I/O	ADIN24
	PF1	77	53	I/O	ADIN25
	PF2	78	-	I/O	ADIN26
	PF3	95	-	I/O	ADIN27
	PF4	96	-	I/O	ADIN28
	PF5	105	-	I/O	ADIN29
	PF6	106	-	I/O	ADIN30
	PF7	107	-	I/O	ADIN31

1.5 Electrical Characteristics

About electrical specifications, standard specifications are described in the manual of this LSI. When using this LSI, consult the staff in our sales offices for the product specifications.

1.5.1 Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
A1	Power supply voltage 1		V_{DD5A}	-0.3 to 7.0	V
A2	Power supply voltage 2		AV_{DD5A}	-0.3 to 7.0	V
A3	Internal power supply voltage 1		V_{OUT3A}	-0.3 to 4.6	V
A4	Internal power supply voltage 2		V_{OUT12A}	-0.3 to 1.6	V
A5	Input pin voltage		V_{I1}	-0.3 to V_{DD5} +0.3 (Upper limit: 7.0)	V
A6	VGA input pin voltage		V_{I2}	-2.5 to V_{DD5} +0.3 (Upper limit: 7.0)	V
A7	I/O pin voltage		V_{I3}	-0.3 to V_{DD5} +0.3 (Upper limit: 7.0)	V
A8	Average Output current	I/O pin 1 *1	I_{O1}(avg)	±12	mA
A9		I/O pin 2 *2	I_{O2}(avg)	±24	mA
A10		Total of all pins	I_{O3}	±70	mA
A11	Power dissipation		P_D	1.04	W
A12	Operating case temperature		T_{copr}	-40 to 110	°C
A13	Storage temperature		T_{stg}	-40 to +125	°C

Note:

Although this LSI has internal ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gate.

This product may sustain permanent damage if it gets stress which is higher than the above stated absolute maximum rating even only for a second. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.

Note:

*1 I/O pin 1 is I/O pin 1 and I/O pin 3 of 1.5.3 DC Characteristics.

Note:

*2 I/O pin 2 is I/O pin 2 and I/O pin 4 to 6 of 1.5.3 DC Characteristics.

1.5.2 Operation Conditions

Power supply voltage during operation			V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B1	External power supply voltage 1	V_{DD5}	V_{RST5N}	5.0	5.5	V
B2	External power supply voltage 2	AV_{DD5}	-	V_{DD5}	-	
B3	Internal power supply voltage 1	V_{OUT3}	-	2.9	-	
B4	Internal power supply voltage 2	V_{OUT12}	-	1.25	-	

Note:

Supply the external power supply pin VDD50 and the analog power supply pin AVDD50 from the same external power supply.

Oscillation pin			V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V, V_{SS} = AV_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B5	External oscillation frequency (Ceramic/Crystal)	F_{OSC}	4.0	-	20.0	MHz
B6	External oscillation Feedback resistor	R_{FB}	-	1.0	-	MΩ

Note:

Oscillation circuit characteristics and peripheral parts(load capacity, damping resister, and feedback resister) are different by each oscillator and substrate. To decide appropriate capacity value for circuit constant, please consult the oscillator manufacturer.

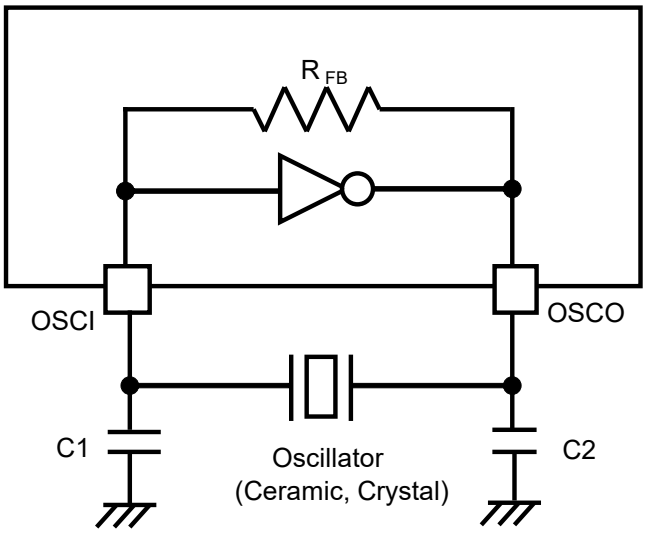

Figure 1.5-1 Oscillation Circuit

External clock input OSCI (OSCO left open)			V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V, V_{SS} = AV_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B7	Clock frequency	F_{CP}	4.0	-	20.0	MHz
B8	High level pulse width	t_{wh1}	20	-	-	ns
B9	Low level pulse width	t_{wl1}	20	-	-	
B10	Rising time	t_{wr1}	-	-	5	
B11	Falling time	t_{wf1}	-	-	5	

Note:
It is necessary to set clock duty ratio from 45 % to 55 %.

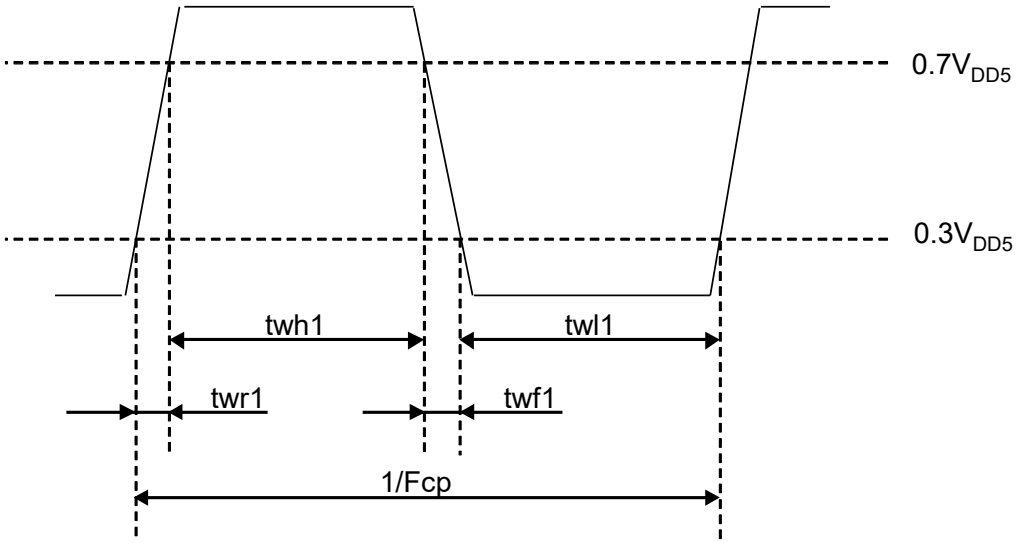

Figure 1.5-2 OSCI Timing Chart

1.5.3 DC Characteristics

Power supply current during operation			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C Output pins left open			
Parameter		Symbol	Conditions	Rating		Unit
				TYP	MAX	
C1	NORMAL mode	I_{DD1}	F_{OSC} = 10 MHz, PLL is used CPUCLK = 160 MHz, IOCLK = 80 MHz CPU and Peripheral circuits are operating. Analog circuits are stopped.	90	190	mA
C2	SLEEP mode	I_{DD2}	FOSC= 10 MHz, PLL is used CPUCLK = 160 MHz, IOCLK = 80 MHz CPU is stopped, Peripheral circuits are operating. Analog circuits are stopped.	60	160	
C3	DEEP SLEEP mode	I_{DD3}	F_{OSC} = 10 MHz, PLL is stopped, CPUCLK = IOCLK = Stop, CPU and Peripheral circuits are stopped. Analog circuits are stopped.	12	120	
C4		I_{DD4}	F_{OSC} is stopped, PLL is stopped.	10	120	

Note:

*1 The measurement conditions are as follows.

- All I/O pins are output state. (No load)

Input pin 1 TEST			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C5	Input voltage "High level"	V_{IH1}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{DD5} × 0.7	-	V_{DD5}	V
C6	Input voltage "Low level"	V_{IL1}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{SS}	-	V_{DD5} × 0.3	
C7	Input leakage current	I_{LK1}	V_{IN} = 0 V to V_{DD5}	-	-	±10	µA

Input pin 2 NDMOD, SWDCLK			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C8	Input voltage "High level"	V_{IH2}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{DD5} × 0.7	-	V_{DD5}	V
C9	Input voltage "Low level"	V_{IH2}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{SS}	-	V_{DD5} × 0.3	
C10	Internal pull-up resis-tor	R_{IO2}	V_{IN} = 0 V	15	30	60	kΩ

Input pin 3 PC0 to PC3, PD0, PD1, PE0, PE1			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C11	Input voltage "High level"	V_{IH3}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{DD5} × 0.7	-	V_{DD5}	V
C12	Input voltage "Low level"	V_{IL3}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{SS}	-	V_{DD5} × 0.3	
C13	Input leakage current	I_{LK3}	V_{IN} = 0 V to V_{DD5}	-	-	±15	µA
C14	Input voltage range	V_{IN3}	VGA is used	-2.0	-	V_{DD5}	V

I/O pin 1 NRST			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C15	Input voltage "High level"	V_{IH4}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{DD5} × 0.7	-	V_{DD5}	V
C16	Input voltage "Low level"	V_{IL4}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{SS}	-	V_{DD5} × 0.3	
C17	Internal pull-up resis-tor	R_{IO4}	V_{IN} = 0 V	15	30	60	kΩ
C18	Output voltage "Low level"	V_{OL4}	V_{DD5} = V_{RST5P} I_{OL} = 3.0 mA	-	-	0.5	V

I/O pin 2 SWDD			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C19	Input voltage "High level"	V_{IH5}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{DD5} × 0.7	-	V_{DD5}	V
C20	Input voltage "Low level"	V_{IL5}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{SS}	-	V_{DD5} × 0.3	
C21	Internal pull-up resis-tor	R_{IO5}	V_{IN} = 0 V	15	30	60	kΩ

I/O pin 2 SWDD			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C22	Output voltage "High level"	V_{OH5}	I_{OH} = -6.0 mA	4.5	-	-	V
C23	Output voltage "Low level"	V_{OL5}	I_{OL} = 6.0 mA	-	-	0.5	

I/O pin 3 P16, P17, P22, P24, P36, P42, P47, P60, P64 to P67,P70 to P77, P86, P87, P96, P97, PA6, PA7, PB0 to PB4,PB6,PB7,PC4 to PC7, PD2 to PD7, PE2 to PE7, PF0 to PF7			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C24	Input voltage "High level"	V_{IH6}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{DD5} × 0.7	-	V_{DD5}	V
C25	Input voltage "Low level"	V_{IL6}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{SS}	-	V_{DD5} × 0.3	
C26	Input leakage current	I_{LK6}	V_{IN} = 0 V to V_{DD5}	-	-	±10	µA
C27	Internal pull-up resis-tor	R_{IO6}	V_{IN} = 0 V	15	30	60	kΩ
C28	Output voltage "High level"	V_{OH6}	I_{OH} = -3.0 mA	4.5	-	-	V
C29	Output voltage "Low level"	V_{OL6}	I_{OL} = 3.0 mA	-	-	0.5	

I/O pin 4 P00 to P05, P10, P11, P25 to P27, P30 to P32, P34, P35,P40, P41, P44 to P46, P50, P51, P54 to P57, P61 to P63,P80 to P85, P90 to P95, PA0 to PA5			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C30	Input voltage "High level"	V_{IH7}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{DD5} × 0.7	-	V_{DD5}	V
C31	Input voltage "Low level"	V_{IL7}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V	V_{SS}	-	V_{DD5} × 0.3	
C32	Input leakage current	I_{LK7}	V_{IN} = 0 V to V_{DD5}	-	-	±10	µA
C33	Internal pull-up resis-tor	R_{IO7}	V_{IN} = 0 V	15	30	60	kΩ

I/O pin 4 P00 to P05, P10, P11, P25 to P27, P30 to P32, P34, P35,P40, P41, P44 to P46, P50, P51, P54 to P57, P61 to P63,P80 to P85, P90 to P95, PA0 to PA5			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C34	Output voltage "High level"	V_{OH7}	I_{OH} = -6.0 mA	4.5	-	-	V
C35	Output voltage "Low level"	V_{OL7}	I_{OL} = 6.0 mA	-	-	0.5	

I/O pin 5 P06, P07, P52, P53			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C36	Input voltage "High level" 1	V_{IH81}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=0	V_{DD5} × 0.7	-	V_{DD5}	V
C37	Input voltage "High level" 2	V_{IH82}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=1	1.35	-	V_{DD5}	
C38	Input voltage "Low level" 1	V_{IL81}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=0	V_{SS}	-	V_{DD5} × 0.3	
C39	Input voltage "Low level" 2	V_{IL82}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=1	V_{SS}	-	0.8	
C40	Input leakage current	I_{LK8}	V_{IN} = 0 V to V_{DD5}	-	-	±10	µA
C41	Internal pull-up resis-tor	R_{IO8}	V_{IN} = 0 V	15	30	60	kΩ
C42	Output voltage "High level"	V_{OH8}	I_{OH} = -6.0 mA	4.5	-	-	V
C43	Output voltage "Low level"	V_{OL8}	I_{OL} = 6.0 mA	-	-	0.5	

I/O pin 6 P12 to P15, P20, P21			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C44	Input voltage "High level" 1	V_{IH91}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=0	V_{DD5} × 0.7	-	V_{DD5}	V
C45	Input voltage "High level" 2	V_{IH92}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=1	V_{DD5} × 0.8	-	V_{DD5}	
C46	Input voltage "Low level" 1	V_{IL91}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=0	V_{SS}	-	V_{DD5} × 0.3	
C47	Input voltage "Low level" 2	V_{IL92}	V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V Register PnILV=1	V_{SS}	-	V_{DD5} × 0.2	
C48	Input leakage current	I_{LK9}	V_{IN} = 0 V to V_{DD5}	-	-	±10	µA
C49	Internal pull-up resistor	R_{IO9}	V_{IN} = 0 V	15	30	60	kΩ
C50	Output voltage "High level"	V_{OH9}	I_{OH} = -6.0 mA	4.5	-	-	V
C51	Output voltage "Low level"	V_{OL9}	I_{OL} = 6.0 mA	-	-	0.5	

1.5.4 Analog Characteristics

This manual shows the electrical characteristics of analog.

1.5.4.1 12bit A/D Converter

ADC0, ADC1, ADC2				V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution	-		-	-	12	Bits
D2	Conversion clock	-		10	-	40	MHz
D3	Integral non-linearity error	$INLE_{AD}$	Sampling time ≥ 150 ns Conversion clock = 40 MHz	-	-	±3	LSB
D4	Differential non-linearity error	$DNLE_{AD}$		-	-	±3	LSB
D5	Zero transition voltage	-		-20	-	20	mV
D6	Full-scale transition voltage	-		4980	-	5020	mV
D7	A/D conversion time	-		0.5	-	-	µs
D8	Input dynamic range	V_{IA}		AV_{SS}	-	AV_{DD5}	V
D9	Power supply current during operation	I_{AD}	Conversion clock = 40 MHz	-	2.5	-	mA/unit

1.5.4.2 Programmable Gain Amplifier (VGA)

VGA00 to 02, VGA1, VGA2			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D10	Gain	G_{VGA}		1	-	20	times
D11	Gain error	G_{ERR1}	G_{VGA} = 1 to 10 times	-	±0.7	±1.5	%
		G_{ERR2}	G_{VGA} = 20 times	-	±1.2	±2.0	
D12	Output offset voltage	V_{OFFG1}	G_{VGA} = 1 to 10 times	-	±80	±120	mV
		V_{OFFG2}	G_{VGA} = 20 times	-	±130	±180	
D13	Output reference voltage range	V_{REFG}		1.0	-	4.0	V
D14	Output dynamic range	V_{OG}		1.0	-	4.0	
D15	Input dynamic range	V_{IG1}	G_{VGA}=1 time	-2.0	-	3.0	
		V_{IG2}	G_{VGA}=2 times	-1.5	-	1.5	
		V_{IG3}	G_{VGA}=3 times	-1.0	-	1.0	
		V_{IG4}	G_{VGA}=4 times	-0.75	-	0.75	
		V_{IG5}	G_{VGA}=5 times	-0.6	-	0.6	
		V_{IG6}	G_{VGA}=6 times	-0.5	-	0.5	
		V_{IG7}	G_{VGA}=8 times	-0.375	-	0.375	
		V_{IG8}	G_{VGA}=10 times	-0.3	-	0.3	
		V_{IG9}	G_{VGA}=20 times	-0.15	-	0.15	
D16	Power supply current during operation	I_G	G_{VGA}=10 times, V_{INP}=V_{INN}=0.0 V	-	2.6	-	mA/ Unit

1.5.4.3 Comparator

CMP00 to CMP41				V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D17	Input offset voltage	V_{OFFC}		-	-	±20	mV
D18	Input dynamic range	V_{IC}		50	-	4950	
D19	Input hysteresis width	V_{HYSC}	CMPNn = 2.5 V	-	30	50	
D20	Minimum comparison voltage	V_{MINC}		20	-	-	
D21	Power supply current during operation	I_C		-	0.3	-	mA/ Unit

1.5.4.4 D/A Converter

8bit D/A Converter DAC00 to DAC41, DACV00 to 02, DACV1, DACV2			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D22	Resolution			-	-	8	Bits
D23	Integral non-linearity error	$INLE_{DA1}$		-	-	±1	LSB
D24	Differential linearity error	$DNLE_{DA1}$		-	-	±1	
D25	Zero scale voltage	-		-20	-	80	mV
D26	Full scale voltage	-		4900	-	5020	
D27	Power supply current during operation	I_{DA1}		-	0.5	-	mA/ Unit

10bit D/A Converter DACA0, DACA1			V_{DD5} = AV_{DD5} = 5.0 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D28	Resolution			-	-	10	Bits
D29	Integral non-linearity error	$INLE_{DA2}$		-	-	±3	LSB
D30	Differential linearity error	$DNLE_{DA2}$		-	-	±3	
D31	Zero scale voltage	-		-20	-	80	mV
D32	Full scale voltage	-		4950	-	5035	
D33	Power supply current during operation	I_{DA2}		-	0.5	-	mA/ Unit

1.5.4.5 Power Supply Voltage Detection(LVD)

				V_{SS} = AV_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D34	Power supply voltage detection level	V_{LVDP}	At rising	4.0	4.2	4.4	V
D35		V_{LVDN}	At falling	3.9	4.1	4.3	
D36	Change rate of power supply voltage(V_{DD5})	ΔV_{DD5P}	At rising			5	V/ms
D37		ΔV_{DD5N}	At falling			1	

1.5.4.6 Power-on Reset

				V_{SS} = AV_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D38	Power supply voltage detection level	V_{RST5P}	At rising	3.6	3.8	4.1	V
D39		V_{RST5N}	At falling	3.5	3.7	4.0	
D40		V_{RST3P}	At rising	2.40	2.55	2.70	
D41		V_{RST3N}	At falling	2.35	2.50	2.65	
D42	Change rate of power supply voltage(V_{DD5})	ΔV_{DD5P}	At rising	-	-	5	V/ms
D43		ΔV_{DD5N}	At falling	-	-	1	

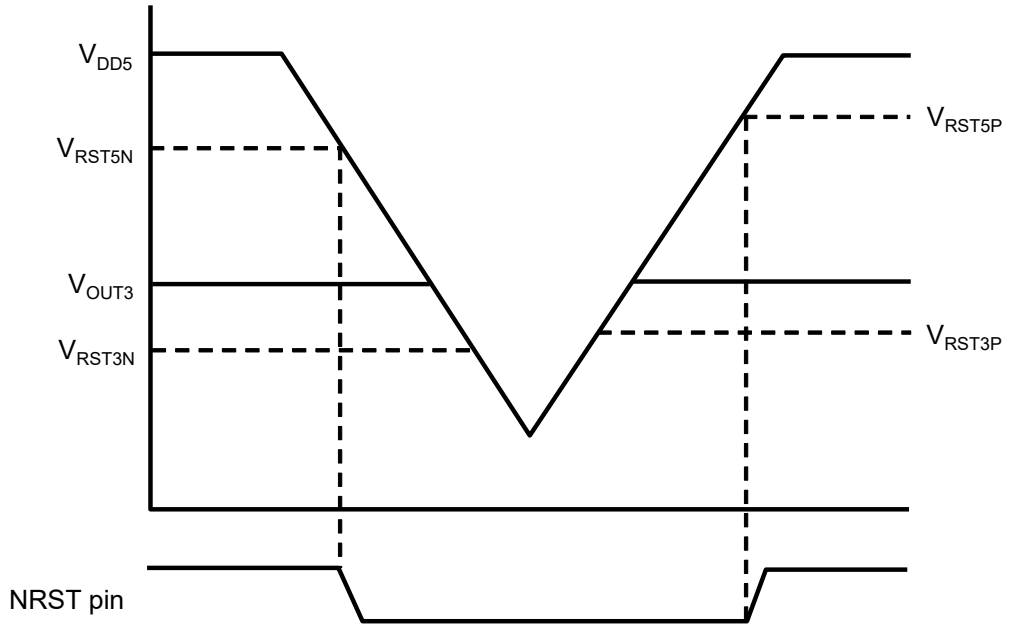

Figure 1.5-3 Characteristics of Power-on Reset Circuit

1.5.4.7 Internal Oscillation

				V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D44	Oscillation frequency	F_{RC}		9	10	11	MHz

1.5.5 AC Characteristics

				V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
E1	Reset signal pulse width	t_{NRSTW}		1	-	-	µs

1.5.6 Flash EEPROM Characteristics

				V_{DD5} = AV_{DD5} = V_{RST5N} to 5.5 V, V_{SS} = AV_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F1	Allowable time of re-writing:1	E_{MAX1}	I-Flash, ECC function enabled	10,000	-	-	times
F2	Allowable times of re-writing:2	E_{MAX2}	D-Flash, ECC function enabled	30,000	100,000	-	
F3	Data retention period 1 (*1)	T_{HLD1}	I-Flash After rewriting E_{MAX1}(MIN) times	20	-	-	years
F4	Data retention period 2 (*1)	T_{HLD2}	D-Flash After rewriting E_{MAX2}(MIN) times	5	-	-	
F5	Data retention period 3 (*1)	T_{HLD3}	D-Flash After rewriting 1,000 times	10	-	-	

Note:

*1 Including time when power is turned off.

1.6 Package Dimension

External dimensions of package are shown as follows.

- HQFP144-20□ Figure 1.6-1

Unit : mm

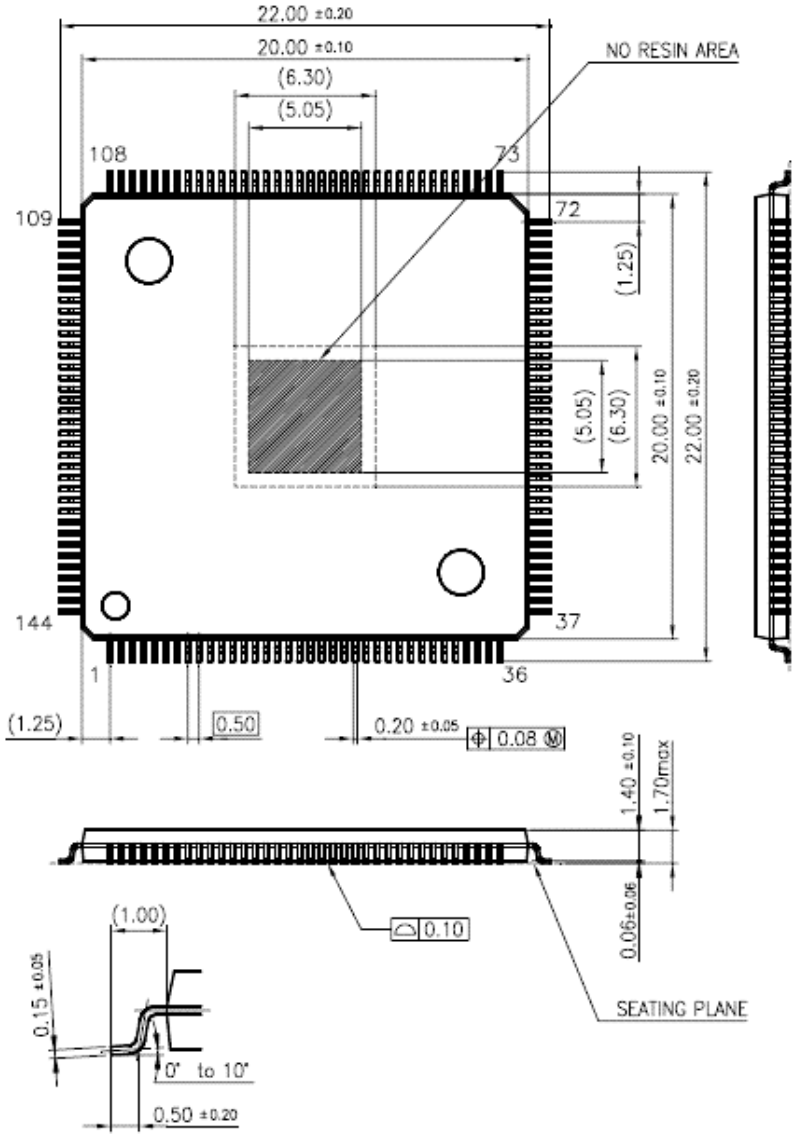

Figure 1.6-1 Package Dimension of HQFP144-20□ (unit: mm)

- HQFP100-14□ Figure 1.6-2

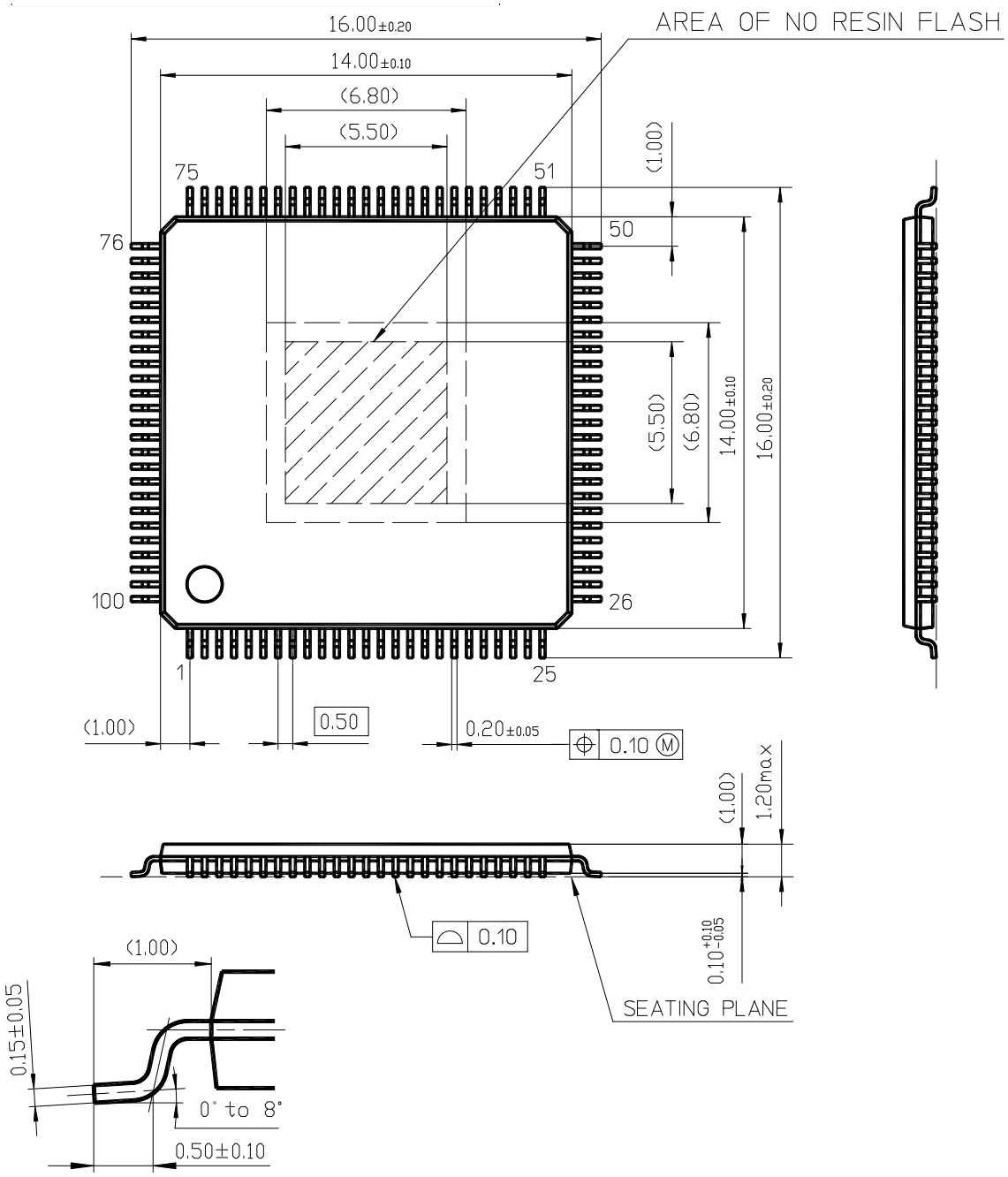

Figure 1.6-2 Package Dimension of HQFP100-14□ (unit: mm)

Note:

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

1.7 Cautions for Circuit Setup

The cautions for circuit setup are described as follows.

- Cautions of Usage
- Pin Connection
- Unused Pin Connection
- Cautions of Power Supply
- Example of Oscillator Connection

1.7.1 Cautions of Usage

When using this LSI, obey the following cautions.

1. Operation temperature should be well considered. If the operation temperature is over the condition, improper operation can occur.
2. Operation voltage should be also well considered.

   - If the operation voltage is over the operating range, duration of the product can be shortened (e.g. the lifetime warranty of a transistor due to the change over time).

   - If the operation voltage is below the operating range, it may operate improperly.
3. If you install the product close to high electrical fields (just below the cathode ray tube, etc.), shield the package surface to ensure normal performance.

1.7.2 Pin Connections

Each pin connection is listed in Table 1.7-1 .

Table 1.7-1 Pin Connections

Pin name	Input/Output	Connection details
VDD50, AVDD50	Input	Connect to 5 V external power supply. Connect the bypass capacitors of 0.1 μF and the decoupling capacitor of 10 μF or more between each pin and VSS pins. (Put the capacitor near the pins)
VSS, AVSS	Input	Short circuit with common GND.
VOUT30, VOUT12	Output	Connect the bypass capacitors of 0.1 μF and the used capacitor of 10 μF to 50 μF for stabilization between each pin and VSS pins. (Put the capacitor near the pins)
OSCI, OSCO	I/O pin	HXOCLK is generated by connecting the oscillator to OSCI and OSCO pins and starting external oscillation(HXO).
SWDCLK, SWDD	Input	Insert a 100 Ω limit resistor between this pin and the external connector. Pull-up connect to V_{DD5} with the resistor of 10 kΩ.
TRCSWO	Output	Insert a 100 Ω limit resistor between this pin and the external connector.
NDMOD	Input	Insert a 100 Ω limit resistor between this pin and the external connector. Pull-up connect to V_{DD5} with the resistor of 2 kΩ.
TEST, VPP	Input	Pull-down connect to VSS with the resistor of 2 kΩ.
NRST	I/O pin	Insert a 100 Ω limit resistor between this pin and the external connector. Connect the capacitor of 0.1μF or more between each pin and VSS pins. (Put the capacitor near the pins)
P65/TM05B	I/O pin	Insert the limit resistor of 3.3 kΩ or more between this pin and the external part.
PC0, PC1, PC2, PC3, PD0, PD1, PE0, PE1	Input	When inserting a limit resistor, insert a resistor of 200 Ω or less.

Note:
Determine how to process each pin by evaluating enough in consideration of the effect of external noise.

Note:
VOUT30 and VOUT12 are pins to connect a capacity for the internal power supply stabilization.

Figure 1.7-1 shows the MCU peripheral recommended circuit. Table 1.7-2 shows the recommended external circuit constants.

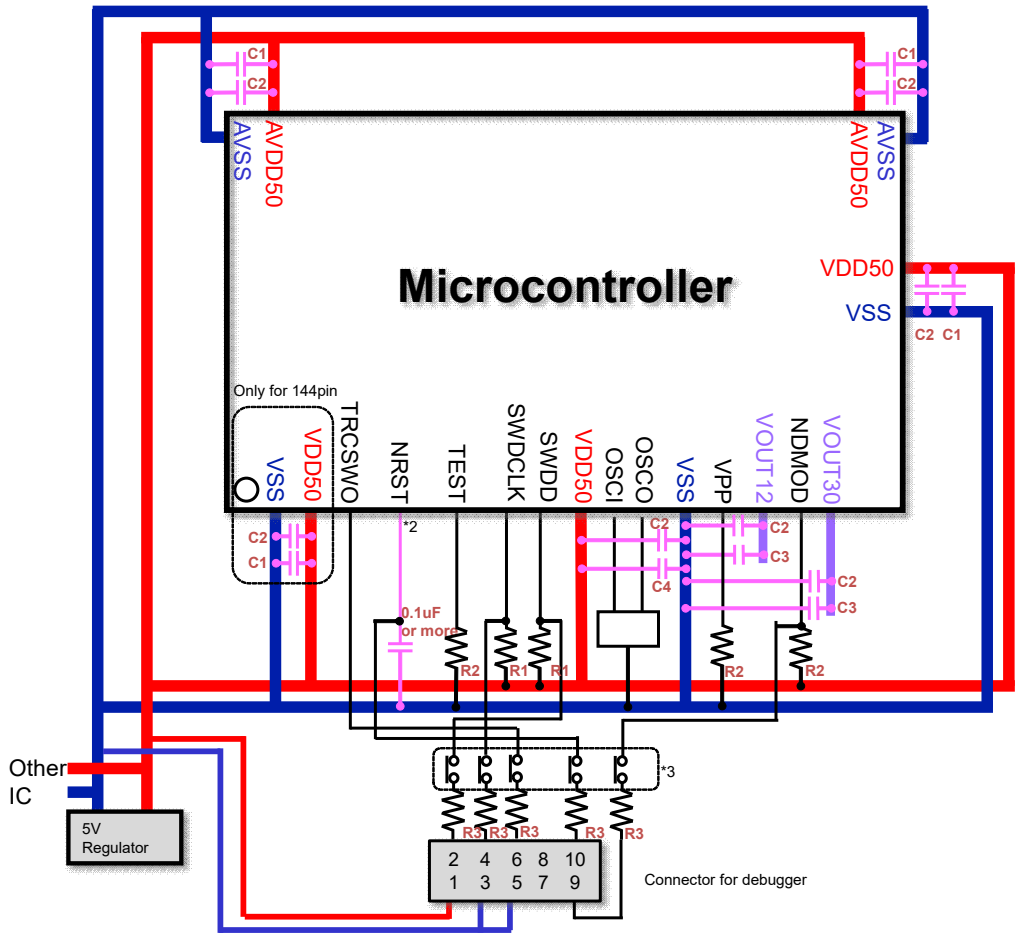

Figure 1.7-1 MCU Peripheral Recommended Circuit

Table 1.7-2 Recommended External Circuit Constants

Sign	Recommended Value	Objective
C1	10 μF	For noise filtering(* 1)
C2	0.1 μF	
C3	10 μF	For the stabilization of internal regulator
C4	more than C3	
R1	10 kΩ	For setting mode pin
R2	2 kΩ	
R3	100 Ω	For preventing noise of communication line

Note:

* 1 Because the most suitable capacity value changes according to the frequency of noise, determine the value by the evaluation from your company.

Note:

* 2 When external reset IC is unused, do not add pull-up resistor to NRST pin.

Note:

* 3 By attaching a jumper etc. near the microcomputer, it is possible to prevent noise coming from the connector and the wiring on the PCB.

1.7.3 Unused pins

It is recommended to use the following procedure to set unused I/O pins to general purpose port function.

First, set unused I/O pins to general purpose port function. Then, set the pins either to I/O disabled state(both input enable and output enable are OFF) or to output state(input enable is OFF and output enable is ON). After that, open the pins. The pins(only for input) which have general purpose port function are also recommended to be set like unused I/O pins. The details are shown in Figure 1.7-2 and Table 1.7-3 .

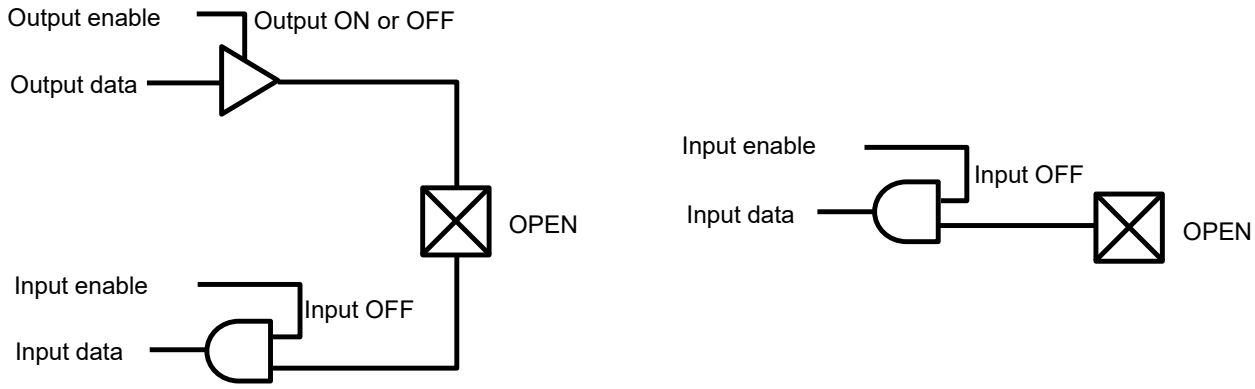

Figure 1.7-2 Unused I/O Pins

Table 1.7-3 Recommended Method of Unused I/O Pins

Pin	Input/ Output	Recommended method of unused pins
PC0 to PC3, PD0 to PD1, PE0 to PE1	Input pin	Set it as general-purpose port function and perform one of the following processing. - Set pins to open in the state of Input/Output prohibition with port control. - Connect the resistor for pull-down in V_{SS} in the state of input with port control. - Connect the resistor for pull-up in V_{DD5} in the state of input with port control.
Other I/O pin	I/O pin	Set it as general-purpose port function and perform one of the following processing. - Set pins to open in the state of Input/Output prohibition with port control. - Set pins to open in the state of "High-level" Output or "Low-level" Output with port control. - Connect the resistor for pull-down in V_{SS} in the state of input with port control. - Connect the resistor for pull-up in V_{DD5} in the state of input with port control.

Note:

Determine how to process each pin by evaluating enough in consideration of the effect of external noise.

1.7.4 Cautions of Power Supply

The cautions of power supply are described as follows.

- Relation between Power Supply and Input Pin Voltage
- Restriction in Power-on
- Power Supply Circuit

1.7.4.1 Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If this order is reversed, a latch up occurs inside of the LSI and the destruction of the LSI by a large current flow can occur.

Relation between power supply and input pin voltage are shown in Figure 1.7-3 .

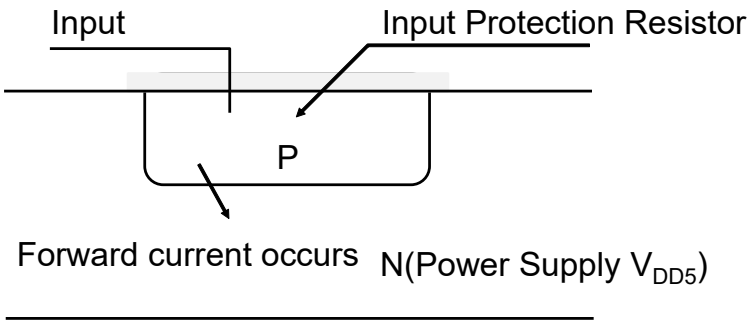

Figure 1.7-3 Relation between Power Supply and Input Pin Voltage

1.7.4.2 Restriction in Power-on

This LSI generates reset when power is applied by power-on reset and operates with the internal power supply generated by internal regulator. Therefore, design the circuit board so that the relation of NRST voltage, power supply voltage(V_{DD5}), and internal power supply voltage(V_{OUT3}, V_{OUT12}) will comply with the following conditions.

- $\Delta V_{DD5P} \leq 5$ V/ms
- $tV_{OUT3} < tV_{RST}$
- $tV_{OUT12} < tV_{RST}$
- $t_{NRSTW} \geq 1$ µs

ΔVDD5P : The rate of power supply voltage (V_{DD5})

tVOUT3 : The time when power supply voltage reaches 2.7V

tVOUT12 : The time when power supply voltage reaches 1.08V

tVRST : The time when power supply voltage reaches the lower limit of power supply voltage level (VRST5P)

tNRSTW : The time that NRST pin maintains "L" level

Figure 1.7-4 shows the relation between power supply voltage and NRST voltage

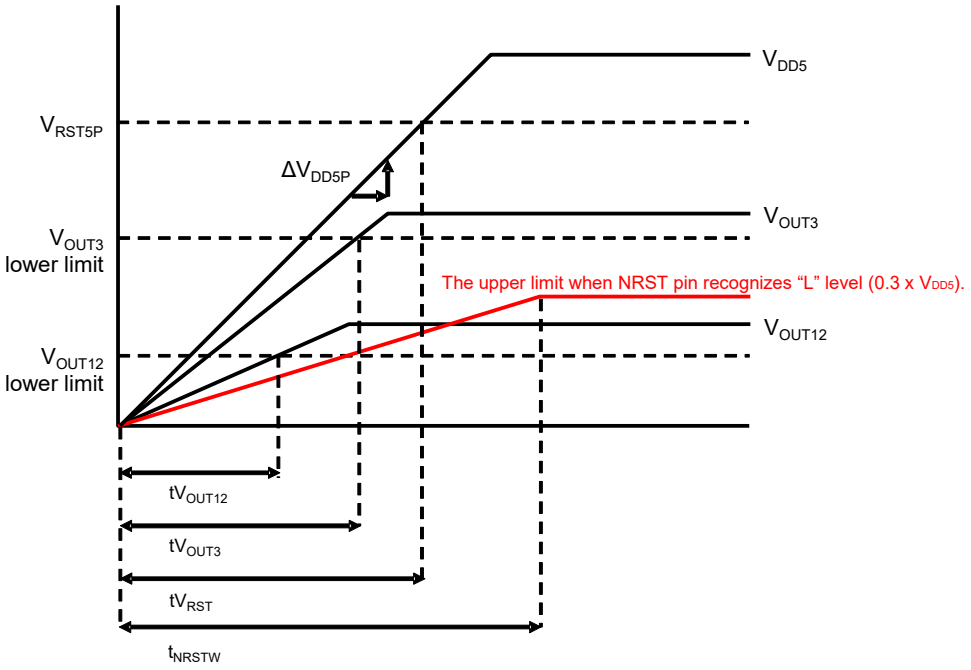

Figure 1.7-4 The Relations between LSI Power Supply and Reset Input Voltage

1.7.4.3 Power Supply Circuit for LSI

The power supply circuit should be designed with a sufficient margin, checking AC line noise evaluation and the ripple when driving an LED and considering the power supply system.

Figure 1.7-5 shows an example for a power supply circuit. (Emitter follower type).

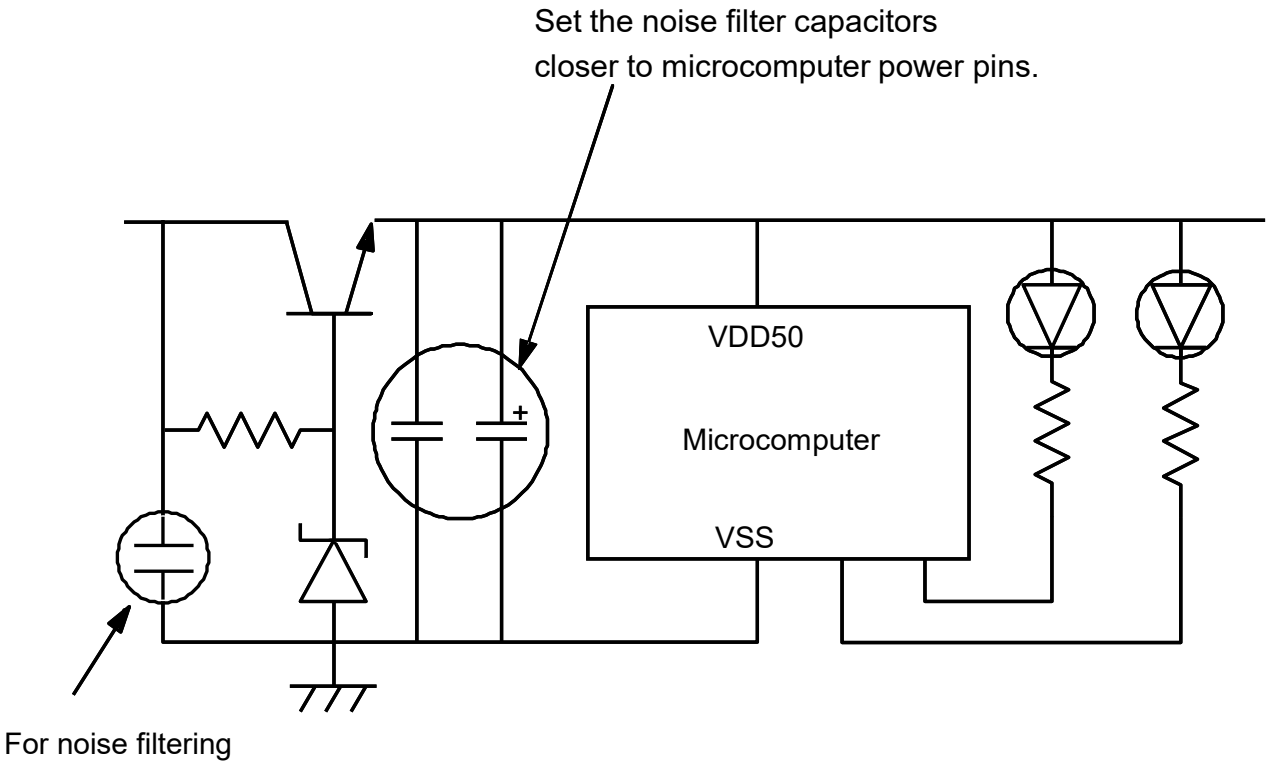

Figure 1.7-5 Power Supply Circuit Example(Emitter Follower Type)

1.7.5 Example of Oscillator Connection

Figure 1.7-6 shows the example of oscillator connection, and Table 1.7-4 shows recommended oscillators
and the circuit constants.

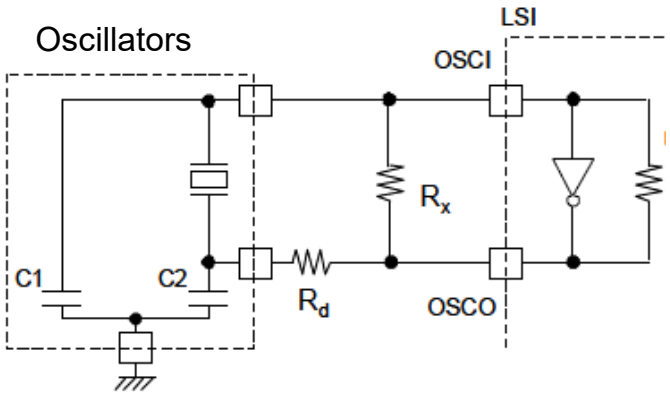

Figure 1.7-6 Example of Oscillator Connection

Table 1.7-4 Recommended Oscillators and The Circuit Constants

Oscillator maker	fre-quen-cy [MHz]	Type	Oscillator Product Number	Recommended circuit constant		
				Load ca-pacity C1 = C2 [pF]	External feedback resistor R_X [Ω]	Dumping re-sistor R_d [Ω]
Murata	20	SMD	CSTNE20M0V530000R0	15 (*1)	Open	150
		Lead	CSTLS20M0X53-B0	15 (*1)	Open	0
	16	SMD	CSTNE16M0V530000R0	15 (*1)	Open	150
		Lead	CSTLS16M0X53-B0	15 (*1)	Open	0
	10	SMD	CSTNE10M0G550000R0	33 (*1)	Open	220
		Lead	CSTLS10M0G56-B0	47 (*1)	Open	220
	8	SMD	CSTNE8M00G550000R0	33 (*1)	Open	330
		Lead	CSTLS8M00G56-B0	47 (*1)	Open	330
	4	SMD	CSTCR4M00G55-R0	39 (*1)	Open	330
		Lead	CSTLS4M00G56-B0	47 (*1)	Open	330

Oscillator maker	frequency [MHz]	Type	Oscillator Product Number	Recommended circuit constant		
				Load capacity C1 = C2 [pF]	External feedback resistor R_X [Ω]	Dumping resistor R_d [Ω]
Kyocera	20	Quartz Crystal Unit	CX3225CA	8	Open	1000
	16				Open	1500
	12		CX5032GA	10	Open	1000
	10			12	Open	0
	8		CX8045GA	20	Open	330
	4				Open	470

The recommended values above are based on the evaluation result of an oscillator for a single unit of this LSI.

(*1) Load capacity of C1 and C2 built-in type

Note:

Consult the oscillator maker for the appropriate circuit constant because the circuit constant of each oscillator, which is connected to OSCI/OSCO, depends on stray capacitance of the oscillator or on the mounting circuit.

Inquiries

If you have questions regarding technical information on this manual, please visit the following URL.

Nuvoton Technology Corporation Japan

URL: https://www.nuvoton.co.jp/en/contact/

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KM1M7BF00/02 Series
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