# MP2731

## Wide Input Range, 4.5A, I²C-Controlled SW Charger with NVDC Power Path and USB OTG

## DESCRIPTION

The MP2731 is a 4.5A, highly integrated switch-mode battery charge management device for single-cell Li-ion or Li-polymer batteries. This device works with NVDC system power path management, and is suitable for a variety of applications, including smartphones, tablets, wireless cameras, and other portable devices. Its low-impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. The I²C serial interface allows the device to be flexibly controlled due to its charging and system settings.

The MP2731 supports a wide range of input sources, including standard USB host ports and high-powered wall adapters with fast charge capabilities. The MP2731 provides USB input type detection via the DP/DM pins.

The device supports USB On-The-Go (OTG) operation by supplying default 5V on the input bus with an output current limit up to 3.0A.

The MP2731 initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in different stages. The charger automatically terminates when a full charge is detected. When the charged battery drops below the recharge threshold, the charger automatically starts another charging cycle.

The charger provides various safety features for battery charging and system operations, including a charging safety timer, battery temperature monitoring, over-voltage and over-current protections. When any fault occurs, the charger asserts an INT signal to host. The device provides BATFET disable control to enter shipping mode, as well as system reset functionality via the DISC pin.

The MP2731 is available in a QFN-26 (3.5mmx3.5mm) package.

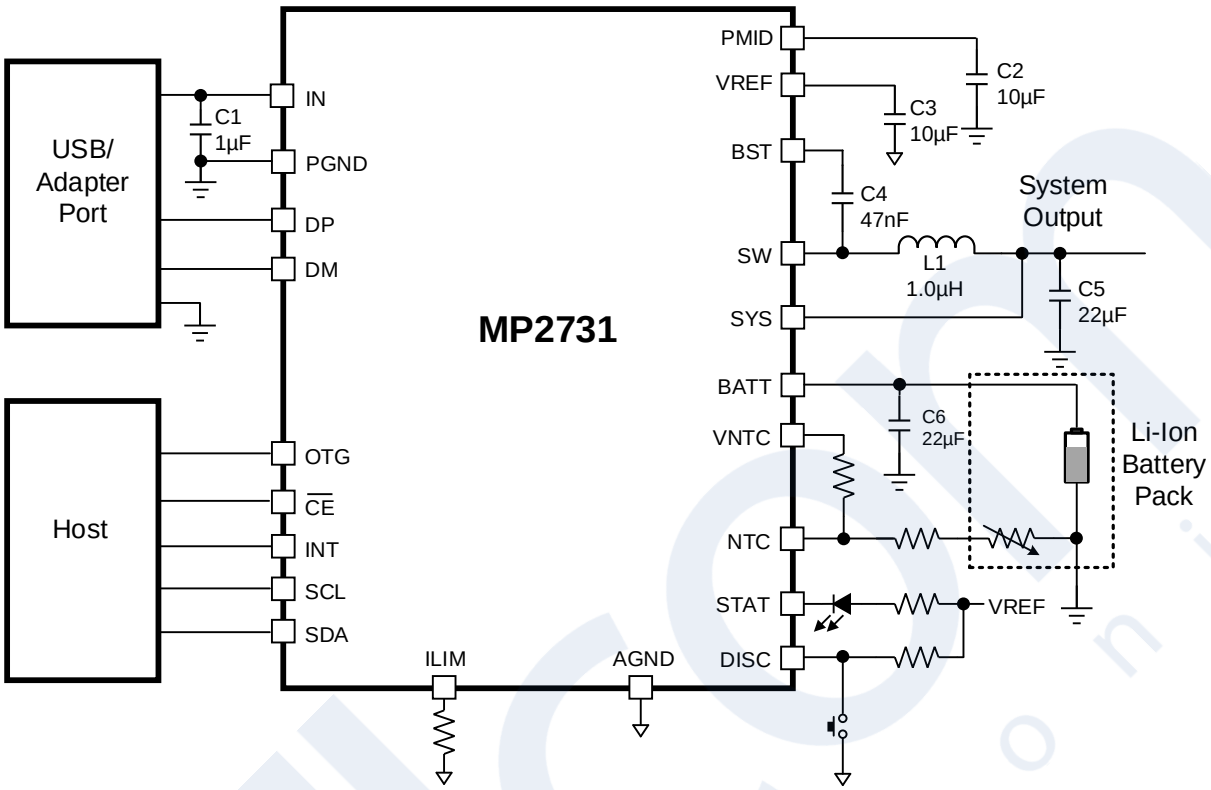
## FEATURES

- 3.7V to 16V Operating Input Voltage Range
- Up to 22V Sustainable Voltage
- **High-Efficiency, 4.5A, 1.35MHz Buck Charger: Up to 92% Charge Efficiency with 3A Charge Current:**
  - Configurable DP/DM for Flexible Fast Charge Protocol Support
- USB OTG with 4.8V to 5.5V Adjustable Output: Up to 3.0A Output, Up to 93% Efficiency with 1.5A Output
- **NVDC Power Path Management:**
  - Instant-On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- High Battery Discharge Efficiency with 14mΩ BATFET Up to 8.5A
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Fully Integrated Power MOSFETs and Current Sensing
- Dedicated DISC Pin to Control Shipping Mode and System Reset
- 13μA Low Battery Leakage Current in Shipping Mode
- Integrated ADC for Monitoring Input Voltage, Input Current, Battery Voltage, Charge Current, System Voltage, and Battery Temperature
- Charging Status Indicator
- Safety Features Including Configurable JEITA for Battery Temperature Protection for Charge Mode, Battery Charging Safety Timer, Thermal Regulation and Thermal Shutdown, Watchdog Monitoring I²C Operation, and Input/System Over-Voltage Protection

## APPLICATIONS

- Tablet PCs
- Smartphones
- Wireless Cameras
- Other Portable Devices

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP2731GQC-xxxx** | QFN-26 (3.5mmx3.5mm) | *See Below* | 1 |

* For Tape & Reel, add suffix -Z (e.g. MP2731GQC-xxxx-Z).

**"-xxxx" is the register setting option. The factory default is "-0001". This content can be viewed in the I²C Register Map on page 29. Contact an MPS FAE to obtain an "-xxxx" value.

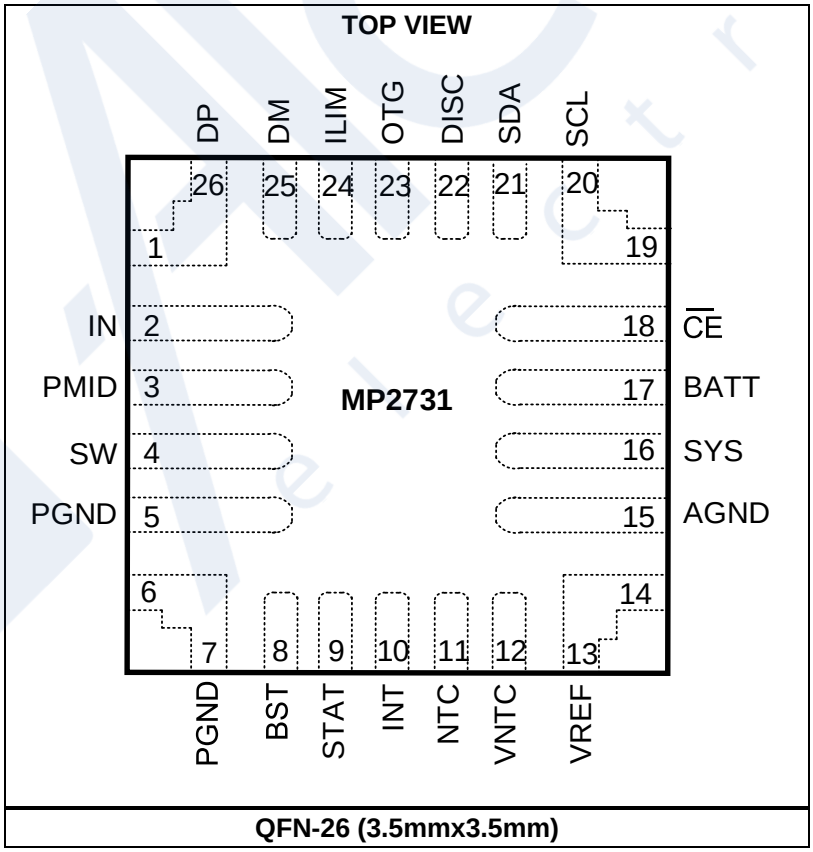
## TOP MARKING

BMAYW

LLLLL

BMA: Product code of MP2731GQC
Y: Year code
W: Week code
LLLLL: Lot number

## PACKAGE REFERENCE




QFN-26 (3.5mmx3.5mm)

## PIN FUNCTIONS

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1, 26 | DP | I/O | **Positive pin of the USB data line pair.** |
| 2 | IN | P | **Power input of the IC.** Place a 1µF ceramic capacitor from IN to PGND, as close as possible to the IC. |
| 3 | PMID | P | **Internal power pin.** Connect PMID to the drain of the reverse-blocking MOSFET and the drain of the high-side MOSFET. Bypass PMID with a 10µF capacitor from PMID to PGND, as close as possible to the IC. |
| 4 | SW | P | **Switching node.** |
| 5, 6, 7 | PGND | P | **Power ground.** |
| 8 | BST | P | **Bootstrap pin.** Connect a 47nF bootstrap capacitor between the BST and SW pins to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage. |
| 9 | STAT | O | **Open-drain charge status output to indicate various charger operations.** Connect STAT to VREF using a 10kΩ resistor. |
| 10 | INT | O | **Open-drain interrupt output**. The INT pin can send charging status and fault interrupt signals to the host. |
| 11 | NTC | I | **Temperature-sense input**. Connect a negative temperature coefficient thermistor to the NTC pin. Program the hot and cold temperature windows with a resistor divider from VNTC to NTC to AGND. Charging is suspended when the NTC pin is out of range. |
| 12 | VNTC | O | **Pull-up voltage bias.** The VNTC pin is the pull-voltage bias of the NTC comparator resistive divider for both the feedback and the reference. |
| 13, 14 | VREF | P | **PWM low-side driver output.** Connect a 10µF ceramic capacitor from VREF to AGND, as close as possible to the IC. |
| 15 | AGND | I/O | **Analog ground.** |
| 16 | SYS | P | **System output.** Connect a 22µF ceramic capacitor from SYS to PGND, as close as possible to the IC. |
| 17 | BATT | P | **Battery positive terminal.** Connect a 22µF ceramic capacitor from BATT to PGND, as close as possible to the IC. |
| 18 | $\overline{CE}$ | I | **Active low charge enable pin.** Battery charging is enabled when the corresponding register is set to active and the $\overline{CE}$ pin is low. |
| 19, 20 | SCL | I | **I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor. |
| 21 | SDA | I/O | **I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor. |
| 22 | DISC | I | **Battery disconnection control pin.** The DISC pin can be used for shipping mode and system resetting. |
| 23 | OTG | I | **Boost mode enable control pin.** The On-The-Go (OTG) function is enabled through the I²C. During boost operation, the OTG pin can go low to suspend boost operation. |
| 24 | ILIM | I | **Configurable input current limit.** To set the maximum input current limit, connect a resistor from ILIM to ground. The actual input current limit is the lower value set by the ILIM pin or the I²C. |
| 25 | DM | I/O | **Negative pin of the USB data line pair.** |

## ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID to GND .....-0.3V to +22V
SW to GND .....-0.3V (-2V for 20ns) to +22V
BST to GND…….....SW to SW + 5V
BATT, SYS to GND……..-0.3V to +6V
All other pins to GND .....-0.3V to +5V
STAT, INT sink current ..... 10mA
Continuous power dissipation ($T_A$ = 25°C) (2) ..... ..... 2.6W
Junction temperature……150°C
Lead temperature (solder) .....260°C
Storage temperature…….. -65°C to +150°C

### *ESD Ratings*

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

### *Recommended Operating Conditions* (3)

$V_{IN}$ to GND ..... 3.7V to 16V (4)
$I_{IN}$.....Up to 3.25A
$I_{SYS}$ .....Up to 4.5A
$I_{CHG}$.....Up to 4.5A
$V_{BATT}$.....Up to 4.67V
$I_{DISCHARGE\ (CONTINUOUS)}$.....Up to 8.5A
$I_{DISCHARGE\ (PULSE)}$.....Up to 9A
Operating junction temp ($T_J$).... -40°C to +125°C

### *Thermal Resistance* (5) $\theta_{JA}$ $\theta_{JC}$

| | | | |
|---|---|---|---|
| QFN-26 (3.5mmx3.5mm)..... | 48 ..... | 11... | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The inherent switching noise voltage should not exceed the absolute maximum rating on either BST or SW pins. A tight layout minimizes switching loss.
5) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Step-Down Converter** | | | | | | |
| Input voltage range | $V_{IN}$ | | 3.7 | | 16 (6) | V |
| Input suspend current | $I_{IN\_SUS}$ | $V_{IN}$ > $V_{IN\_UVLO}$, $V_{IN}$ > $V_{BATT}$, suspend mode, EN_HIZ = 1 | | 1 | 1.5 | mA |
| Input quiescent current | $I_{IN\_Q}$ | $V_{IN}$ > $V_{IN\_UVLO}$, $V_{IN}$ > $V_{BATT}$, $V_{BATT}$ = 3.6V, converter switching, $I_{SYS}$ = 0A | | 4 | | |
| Input under-voltage lockout threshold | $V_{IN\_UVLO}$ | $V_{IN}$ falling | | 3 | 3.2 | V |
| Input under-voltage lockout threshold hysteresis | | $V_{IN}$ rising | | 200 | | mV |
| Input vs. battery voltage headroom | $V_{HDRM}$ | $V_{IN}$ rising | 230 | 300 | 370 | mV |
| | | $V_{IN}$ falling | 120 | 190 | 260 | mV |
| Input over-voltage protection threshold | $V_{IN\_OVLO}$ | $V_{IN}$ rising | 5.8 | 6 | 6.3 | V |
| | | $V_{IN}$ rising, for $V_{IN}$ > 5V | 16.2 | 16.7 | 17.2 | |
| Input over-voltage protection threshold hysteresis | | $V_{IN}$ falling | | 380 | | mV |
| Internal reverse blocking MOSFET on resistance | $R_{ON\_Q1}$ | Measure from IN to PMID | | 20 | | mΩ |
| High-side MOSFET on resistance | $R_{ON\_Q2}$ | Measure from PMID to SW | | 25 | | mΩ |
| Low-side MOSFET on resistance | $R_{ON\_Q3}$ | Measure from SW to PGND | | 25 | | mΩ |
| Switching frequency | $f_{SW}$ | $V_{BATT}$ = 3.7V, $I_{CHG}$ = 2A, REG0Ah, bit[7] = 0 | 1.1 | 1.35 | 1.6 | MHz |
| **SYS Output** | | | | | | |
| Minimum system regulation voltage (I²C) | $V_{SYS\_REG\_MIN}$ | $V_{SYS\_MIN}$ + $V_{TRACK}$, $I_{SYS}$ = 0, $V_{BATT}$ = 3.4V, REG04h, bits[3:1] = 110, REG04h bit[0] = 1 | | 3.82 | | V |
| Battery track voltage | $V_{TRACK}$ | REG04h, bit[0] = 0 | | 100 | | mV |
| | | REG04h, bit[0] = 1 | | 150 | | mV |
| Ideal diode forward voltage in supplement mode | $V_{FWD}$ | 10mA discharge current | | 20 | | mV |
| SYS vs. BATT comparator | $V_{SYS\_GT\_BATT}$ | $V_{SYS}$ falling to enter ideal diode mode | | -20 | | mV |
| SYS vs. BATT comparator hysteresis | | $V_{SYS}$ rising to exit ideal diode mode | | 50 | | mV |
| Battery good comparator (threshold compared with $V_{SYS\_MIN}$) | $V_{BATT\_GD}$ | $V_{BATT}$ rising to the battery FET being turned on fully | | 60 | | mV |
| Battery good comparator hysteresis | | $V_{BATT}$ falling | | 100 | | mV |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Battery Charger** | | | | | | |
| Battery charge voltage regulation (I²C) | $V_{BATT\_REG}$ | Depends on the I²C setting | 3.4 | | 4.67 | V |
| Battery charge voltage regulation accuracy | $V_{BATT\_REG\_ACC}$ | REG07h, bits[7:1] = 1010000, $V_{BATT\_REG}$ = 4.2V | -0.5 | | +0.5 | % |
| | | REG07h, bits[7:1] = 1011111, $V_{BATT\_REG}$ = 4.35V | | | | |
| | | REG07h, bits[7:1] = 1100100, $V_{BATT\_REG}$ = 4.4V | | | | |
| Fast charge current (I²C) | $I_{CC}$ | Depends on the I²C setting | 320 | | 4520 | mA |
| Fast charge current accuracy | $I_{CC\_ACC}$ | $I_{CC}$ bit[6:0] = 0000100, $V_{BATT}$ = 3.8V | 442 | 500 | 558 | mA |
| | | $I_{CC}$ bit[6:0] = 0100110, $V_{BATT}$ = 3.8V | 1739 | 1850 | 1951 | mA |
| | | $I_{CC}$ bit[6:0] = 1000011, $V_{BATT}$ = 3.8V | 2849 | 3000 | 3151 | mA |
| | | $I_{CC}$ bit[6:0] = 1101001, $V_{BATT}$ = 3.8V | 4294 | 4520 | 4750 | mA |
| Pre-charge to fast charge threshold (I²C) | $V_{BATT\_PRE}$ | $V_{BATT}$ rising, REG05h, bit[7] = 1 | 2.8 | 3.0 | 3.1 | V |
| Pre-charge to fast charge hysteresis | | $V_{BATT}$ falling | | 160 | | mV |
| Trickle charge to pre-charge threshold | $V_{BATT\_TC}$ | $V_{BATT}$ rising | 1.9 | 2.0 | 2.1 | V |
| Trickle charge to pre-charge threshold hysteresis | | $V_{BATT}$ falling | | 50 | | mV |
| Trickle-charge current | $I_{TC}$ | $V_{BATT}$ = 1.8V, IPRE bit[0] = 1 | | 185 | | mA |
| | | $V_{BATT}$ = 1.8V, IPRE bit[0] = 0 | | 145 | | |
| Pre-charge current (I²C) | $I_{PRE}$ | Depends on the I²C setting | 150 | | 750 | mA |
| Pre-charge current accuracy | | $V_{BATT}$ = 2.6V, REG06h, bits[7:4] = 0010 | 182 | 225 | 268 | mA |
| Charge termination current threshold (I²C) | $I_{TERM}$ | Depends on the I²C setting | 120 | | 720 | mA |
| Termination current accuracy | | $V_{BATT\_REG}$ = 4.2V, REG06h, bits[3:0] = 0110 | 298 | 360 | 422 | mA |
| Charge termination deglitch time | $t_{TERM\_DGL}$ | | | 200 | | ms |
| Auto-recharge voltage threshold below $V_{BATT\_REG}$ | $V_{RECH}$ | REG07h, bit[0] = 0 | | 110 | | mV |
| Auto-recharge deglitch time | $t_{RECH\_DGL}$ | | | 200 | | ms |
| BATFET on resistance | $R_{ON\_Q4}$ | $V_{BATT}$ = 3.8V | | 14 | | mΩ |
| Battery discharge current limit | $I_{DSCHG\_LMT}$ | $V_{IN}$ = 0V, $V_{BATT}$ = 3.8V, OTG disabled, $I_{SYS}$ rising | 8.5 | | | A |
| Battery discharge function controlled by the DISC pin | $t_{DISC}$ | DISC pin low time to turn off the battery discharge function, REG0Ah, bits[1:0] = 00 | | 8 | | s |
| | | Battery discharge off time to turn on the battery discharge function, REG0Ah, bits[3:2] = 00 | | 0.5 | | |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Voltage and Input Current Regulation** | | | | | | |
| Input minimum voltage regulation (I²C) | $V_{IN\_MIN}$ | | 3.7 | | 15.2 | V |
| Input minimum voltage regulation accuracy | $V_{IN\_MIN\_ACC}$ | REG01h, bits[6:0] = 0000110, $V_{IN\_REG}$ = 4.3V | -3 | | +3 | % |
| Input current limit | $I_{IN\_LIM}$ | USB500 | 400 | 450 | 500 | mA |
| | | USB900 | 750 | 825 | 900 | |
| | | 1A | 840 | 920 | 1000 | |
| | | CDP or 1.5A | 1270 | 1400 | 1500 | |
| | | DCP | 1570 | 1690 | 1800 | |
| | | 2A | 1750 | 1880 | 2000 | |
| | | 2.1A | 1840 | 1970 | 2100 | |
| | | 2.4A | 2050 | 2240 | 2400 | |
| | | 3A | 2640 | 2800 | 3000 | |
| **Protection** | | | | | | |
| Battery over-voltage protection threshold | $V_{BATT\_OVP}$ | Rising, compared to $V_{BATT\_REG}$ | | 103.5 | | % |
| Battery over-voltage protection threshold hysteresis | | Compared to $V_{BATT\_REG}$ | | 1.5 | | % |
| Thermal regulation | $T_{J\_REG}$ | $T_{J\_REG}$ bit[1:0] = 11 | | 112 | | °C |
| Thermal shutdown threshold (6) | $T_{J\_SHDN}$ | $T_J$ rising | | 150 | | °C |
| Thermal shutdown hysteresis (6) | | | | 20 | | °C |
| NTC float threshold | $V_{FLT}$ | As a percentage of VNTC | | 95 | | % |
| NTC float threshold hysteresis | | As a percentage of VNTC | | 3.6 | | % |
| NTC low temp rising threshold | $V_{COLD}$ | As a percentage of VNTC | 71 | 72 | 73 | % |
| NTC low temp rising threshold hysteresis | | As a percentage of VNTC | | 1.3 | | % |
| NTC cool temp rising threshold | $V_{COOL}$ | As a percentage of VNTC | 59 | 60 | 61 | % |
| NTC cool temp rising threshold hysteresis | | As a percentage of VNTC | | 1.3 | | % |
| NTC warm temp falling threshold | $V_{WARM}$ | As a percentage of VNTC | 39.3 | 40.3 | 41.3 | % |
| NTC warm temp falling threshold hysteresis | | As a percentage of VNTC | | 1.5 | | % |
| NTC hot temp falling threshold | $V_{HOT}$ | As a percentage of VNTC | 35.3 | 36.3 | 37.3 | % |
| NTC hot temp falling threshold hysteresis | | As a percentage of VNTC | | 1.5 | | % |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VREF LDO** | | | | | | |
| VREF LDO output voltage | $V_{REF}$ | $V_{IN}$ = 5V, $I_{VREF}$ = 20mA | | 3.6 | | V |
| VREF LDO current limit | $I_{REF\_LMT}$ | $V_{VREF}$ = 3.3V | 40 | | | mA |
| **Battery Discharge Operation** | | | | | | |
| Battery operating range | $V_{BATT}$ | | 2.6 | | 4.75 | V |
| Battery current in shipping mode | $I_{BATT\_SP}$ | $V_{IN}$ < $V_{IN\_UVLO}$, $V_{BATT}$ = 4.2V, BATFET off | | 13 | 16 | µA |
| Battery quiescent current | $I_{BATT\_Q}$ | $V_{IN}$ < $V_{IN\_UVLO}$, $V_{BATT}$ = 4.2V, BATFET on, OTG disabled | | 40 | 47 | µA |
| | | $V_{IN}$ < $V_{IN\_UVLO}$, $V_{BATT}$ = 4.2V, BATFET on, OTG enabled | | 5.0 | | mA |
| OTG output voltage | $V_{IN\_DSCHG}$ | REG03h, bits[5:3] = 011, $I_{OTG}$ = 0A | | 5.07 | | V |
| OTG output voltage accuracy | | As a percentage of $V_{IN\_DSCHG}$, $I_{OTG}$ = 0A | -2 | | +2 | % |
| Battery operation UVLO | $V_{BATT\_UVLO}$ | $V_{BATT}$ falling | 2.35 | 2.45 | 2.55 | V |
| | | $V_{BATT}$ rising | 2.68 | 2.8 | 2.92 | V |
| Battery operation UVLO for OTG | $V_{BATT\_UVLO\_OTG}$ | $V_{BATT}$ falling | 2.45 | 2.55 | 2.65 | V |
| | | $V_{BATT}$ rising | | 3.0 | | V |
| OTG output voltage protection threshold | $V_{INOVP\_DSCHG}$ | $V_{BATT}$ = 3.7V, OTG is enabled, force a voltage at IN until switching is off | | 6.15 | | V |
| OTG output voltage protection threshold hysteresis | | | | 330 | | mV |
| OTG output current limit (I²C) | $I_{IN\_DSCHG}$ | REG03h, bits[2:0] = 000, $V_{BATT}$ = 3.7V | 0.5 | 0.6 | 0.7 | A |
| | | REG03h, bits[2:0] = 011, $V_{BATT}$ = 3.7V | 1.5 | 1.65 | 1.8 | |
| | | REG03h, bits[2:0] = 101, $V_{BATT}$ = 3.7V | 2.1 | 2.25 | 2.4 | |
| | | REG03h, bits[2:0] = 111, $V_{BATT}$ = 3.7V | 3.0 | 3.15 | 3.3 | |
| **Analog-to-Digital Converter (ADC)** | | | | | | |
| Resolution | RES | | | 8 | | bits |
| Input voltage range | $V_{IN}$ | Charge mode or OTG mode | 3.6 | | 15.3 | V |
| Input voltage LSB | $V_{IN\_RES}$ | | | 60 | | mV |
| Input voltage accuracy | $V_{IN\_ACC}$ | Charge mode or OTG mode, $V_{IN}$ = 5V | | 2 | | LSB |
| Battery voltage range | $V_{BATT}$ | Charge mode or OTG mode | 0 | | 5.1 | V |
| Battery voltage LSB | $V_{BATT\_RES}$ | | | 20 | | mV |
| Battery voltage accuracy | $V_{BATT\_ACC}$ | Charge mode or OTG mode, $V_{BATT}$ = 3.8V | | 2 | | LSB |
| Charge current range | $I_{CHG}$ | Charge mode | 0 | | 5.66 | A |
| Charge current LSB | $I_{CHG\_RES}$ | | | 17.5 | | mA |
| Charge current accuracy | $I_{CHG\_ACC}$ | Charge mode, $I_{CHG}$ = 1.84A | | 3 | | LSB |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| System voltage range | $V_{SYS}$ | Charge mode or OTG mode | 0 | | 5.1 | V |
| System voltage LSB | $V_{SYS\_RES}$ | | | 20 | | mV |
| System voltage accuracy | $V_{SYS\_ACC}$ | Charge mode or OTG mode, $V_{SYS}$ = 3.8V | | 2 | | LSB |
| Input current range | $I_{IN}$ | Charge mode | 0 | | 3.39 | A |
| Input current LSB | $I_{IN\_RES}$ | | | 13.3 | | mA |
| Input current accuracy | $I_{IN\_ACC}$ | Charge mode, $I_{IN}$ = 500mA | | 4 | | LSB |
| NTC voltage range | $V_{NTC}$ | Charge mode or OTG mode | 0 | | 100 | % |
| NTC voltage LSB | $V_{NTC\_RES}$ | | | 0.392 | | % |
| NTC voltage accuracy | $V_{NTC\_ACC}$ | Charge mode or OTG mode, $V_{NTC}$ = 50% | | 2 | | LSB |
| **DP/DM USB Detection** | | | | | | |
| DP DCD current source | $I_{DP\_SRC}$ | | 7 | 10 | 14 | uA |
| DM pull-down resistance | $R_{DM\_DOWN}$ | | 14.3 | 20 | 24.8 | kΩ |
| Data detect voltage | $V_{DAT\_REF}$ | | 0.25 | 0.325 | 0.4 | V |
| DP/DM comparator threshold (2.9V) | $V_{TH\_2P9}$ | | 2.8 | 2.9 | 3.0 | V |
| DP/DM comparator threshold (2.4V) | $V_{TH\_2P4}$ | | 2.3 | 2.4 | 2.5 | V |
| DP/DM comparator threshold (2.2V) | $V_{TH\_2P2}$ | | 2.1 | 2.2 | 2.3 | V |
| DP/DM comparator threshold (1.7V) | $V_{TH\_1V7}$ | | 1.6 | 1.7 | 1.8 | V |
| DP voltage source | $V_{DP\_SRC}$ | | 0.5 | 0.6 | 0.7 | V |
| DM voltage source | $V_{DM\_SRC}$ | | 0.5 | 0.6 | 0.7 | V |
| DP sink current | $I_{DP\_SINK}$ | | 70 | 100 | 130 | µA |
| DM sink current | $I_{DM\_SINK}$ | | 70 | 100 | 130 | µA |
| Leakage current input DP/DM pin | $I_{DP\_LKG}$ | | -1 | | +1 | µA |
| | $I_{DM\_LKG}$ | | -1 | | +1 | µA |
| **Logic I/O Pin Characteristics (STAT, INT, OTG, /CE, DISC)** | | | | | | |
| Low logic voltage threshold | $V_{IL}$ | | | | 0.4 | V |
| High logic voltage threshold | $V_{IH}$ | | 1.3 | | | V |
| **I²C Interface (SDA, SCL)** | | | | | | |
| Input high threshold level | $V_{IH}$ | $V_{PULL\ UP}$ = 1.8V, SDA and SCL | 1.3 | | | V |
| Input low threshold level | $V_{IL}$ | $V_{PULL\_UP}$ = 1.8V, SDA and SCL | | | 0.4 | V |
| Output low threshold level | $V_{OL}$ | $I_{SINK}$ = 5mA | | | 0.4 | V |
| I²C clock frequency | $f_{SCL}$ | | | | 400 | kHz |
| **Clock Frequency and Watchdog Timer** | | | | | | |
| Clock frequency | $f_{CLK}$ | | | 5 | | MHz |
| Watchdog timer | $t_{WDT}$ | REG08h, bits[5:4] = 11 | | 160 | | s |

**Note:**

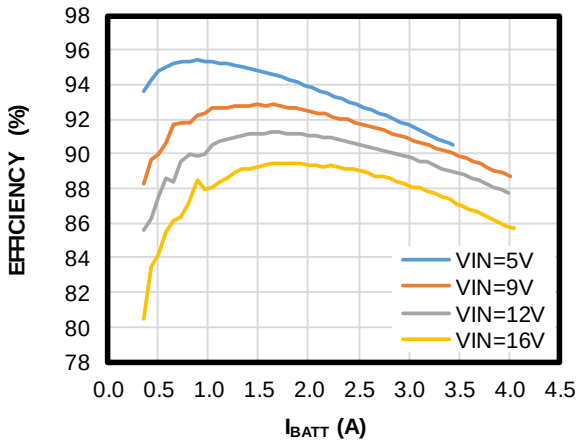
6) Guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 5.0V, $V_{BATT}$ = full range, I²C-controlled, $I_{CHG}$ = 1.84A, $I_{IN\_LIM}$ = 3.0A, $V_{IN\_MIN}$ = 4.3V, L = 1.0μH (DCR = 14.9mΩ), $T_A$ = 25°C, unless otherwise noted.**

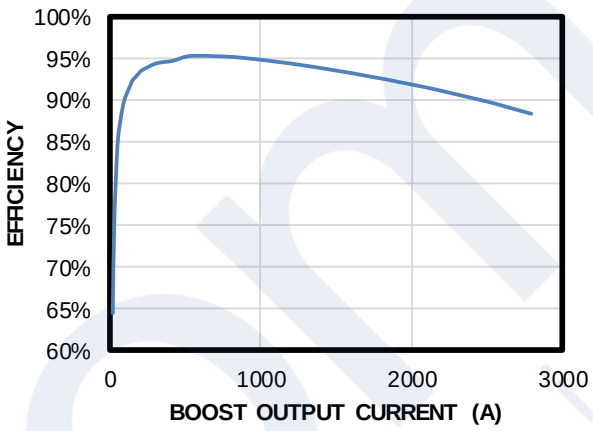
### Charge Efficiency

$V_{BATT}$ = 3.8V

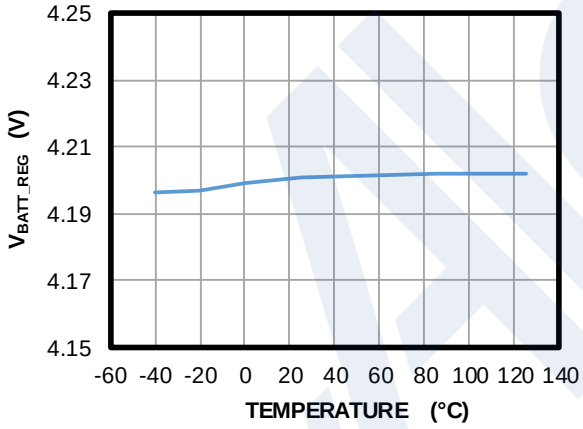



### Boost Efficiency

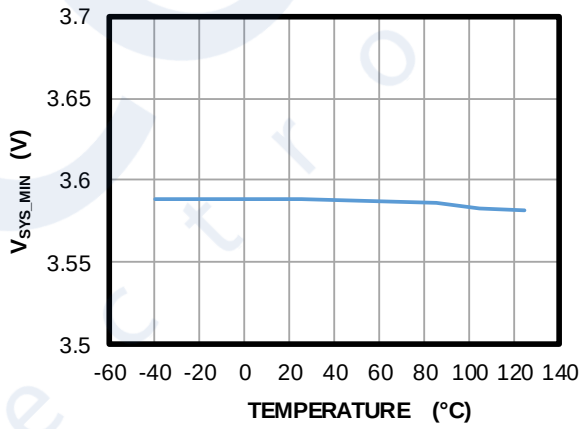
$V_{BATT}$ = 3.8V



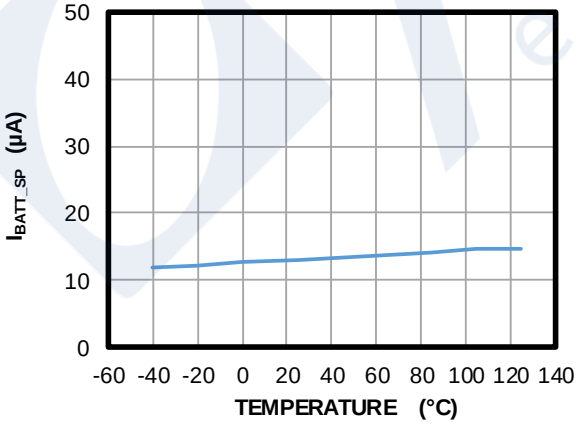

### Battery Regulation Voltage vs. Temperature



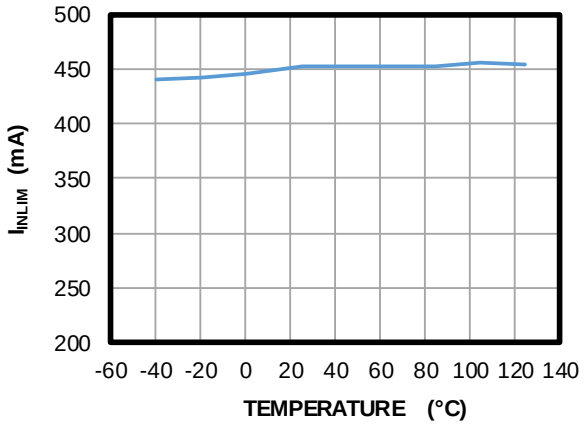

### System Minimum Voltage vs. Temperature




### Battery Current in Shipping Mode vs. Temperature




### 500mA Input Current Limit vs. Temperature

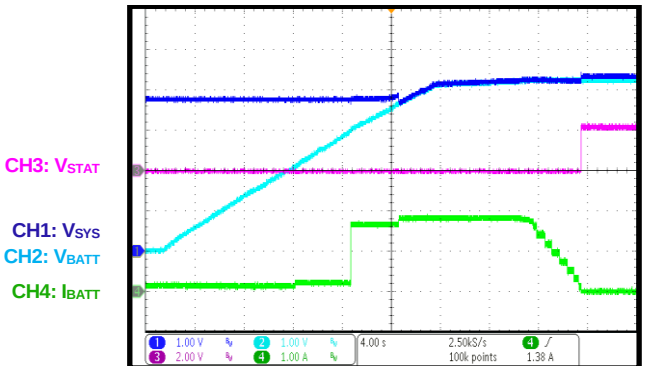


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = full range, I²C-controlled, $I_{CHG}$ = 1.84A, $I_{IN\_LIM}$ = 3.0A, $V_{IN\_MIN}$ = 4.3V, L = 1.0µH (DCR = 14.9mΩ), $T_A$ = 25°C, unless otherwise noted.**

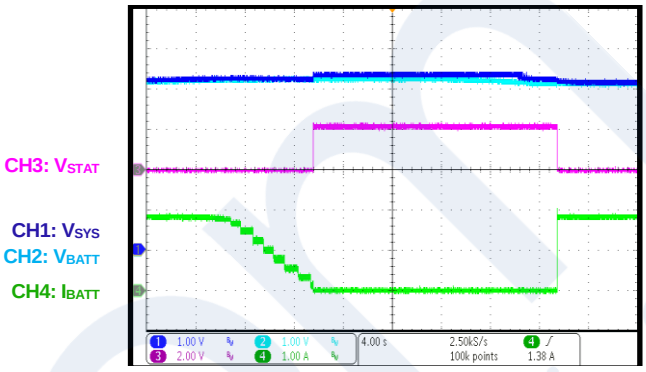
### Battery Charge Curve

$V_{IN}$ = 5V, $V_{BATT\_REG}$ = 4.2V, $I_{SYS}$ = 0A



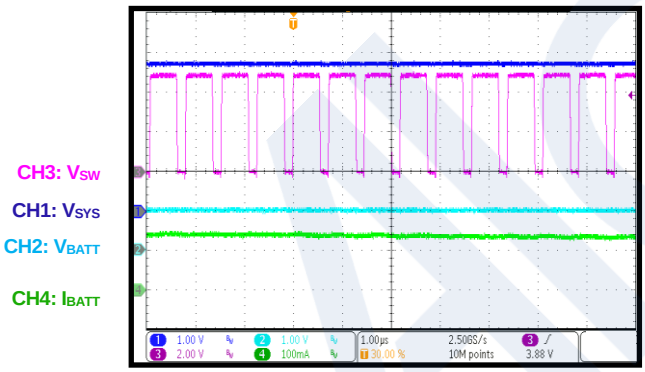

### Auto-Recharge

$V_{IN}$ = 5V, $V_{BATT\_REG}$ = 4.2V, $I_{SYS}$ = 0A



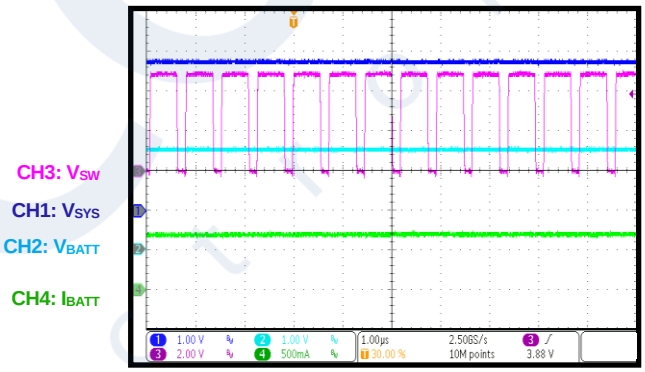

### Trickle Charge

$V_{IN}$ = 5V, $V_{BATT}$ = 1.0V, $I_{TC}$ = 145mA



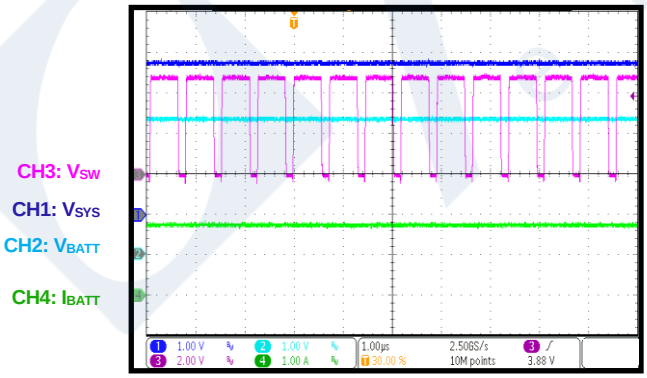

### Pre-Charge

$V_{IN}$ = 5V, $V_{BATT}$ = 2.5V, $I_{PRE}$ = 680mA



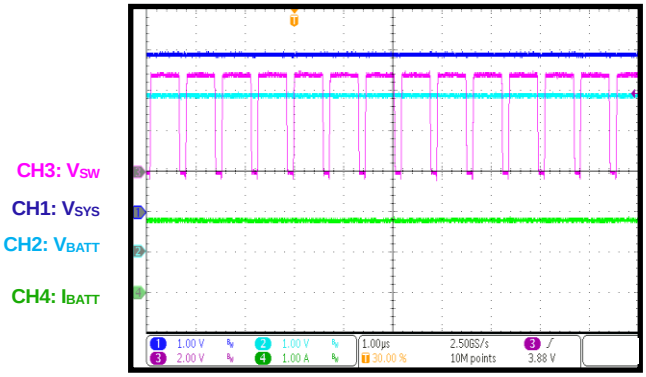

### Constant Current Charge

$V_{IN}$ = 5V, $V_{BATT}$ = 3.3V, $I_{CC}$ = 1840mA




### Constant Current Charge

$V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{CC}$ = 1840mA

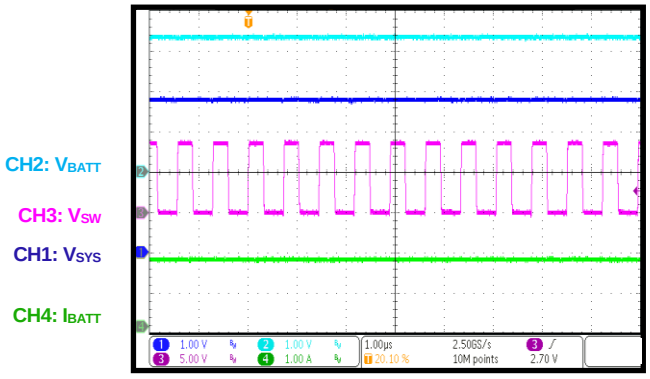


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = full range, I²C-controlled, $I_{CHG}$ = 1.84A, $I_{IN\_LIM}$ = 3.0A, $V_{IN\_MIN}$ = 4.3V, L = 1.0µH (DCR = 14.9mΩ), $T_A$ = 25°C, unless otherwise noted.**

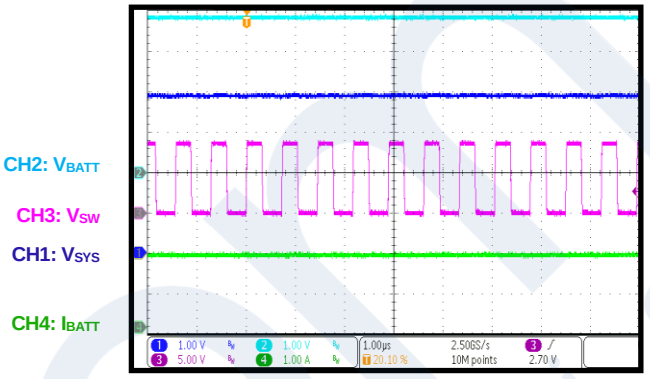
### Constant Current Charge

$V_{IN}$ = 9V, $V_{BATT}$ = 3.3V, $I_{CC}$ = 1840mA



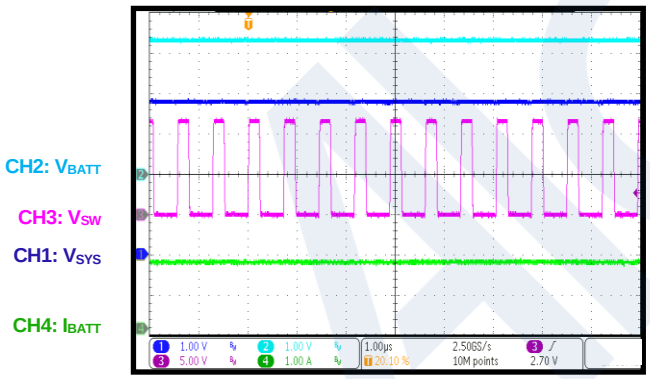

### Constant Current Charge

$V_{IN}$ = 9V, $V_{BATT}$ = 3.8V, $I_{CC}$ = 1840mA



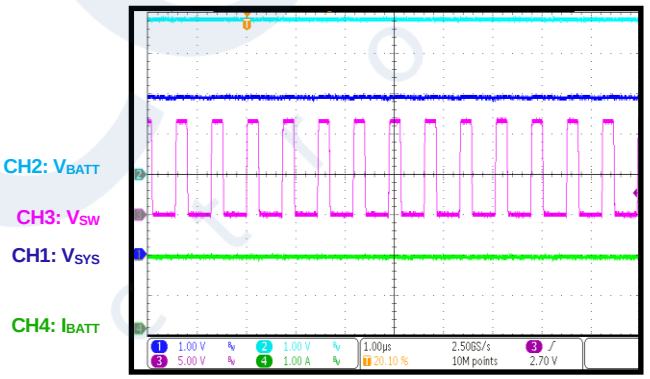

### Constant Current Charge

$V_{IN}$ = 12V, $V_{BATT}$ = 3.3V, $I_{CC}$ = 1840mA



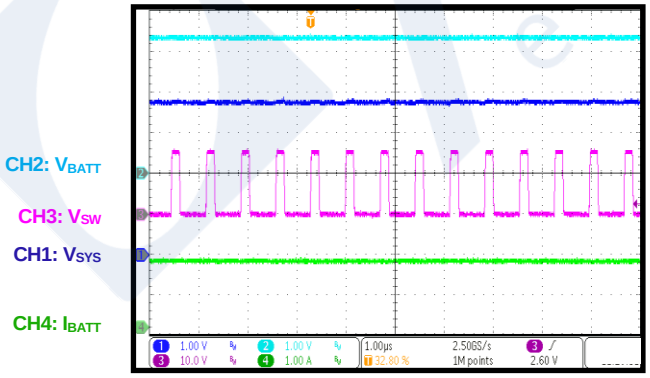

### Constant Current Charge

$V_{IN}$ = 12V, $V_{BATT}$ = 3.8V, $I_{CC}$ = 1840mA



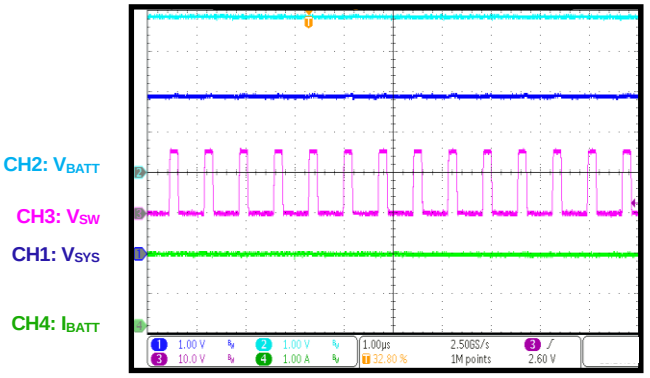

### Constant Current Charge

$V_{IN}$ = 16V, $V_{BATT}$ = 3.3V, $I_{CC}$ = 1840mA




### Constant Current Charge

$V_{IN}$ = 16V, $V_{BATT}$ = 3.8V, $I_{CC}$ = 1840mA

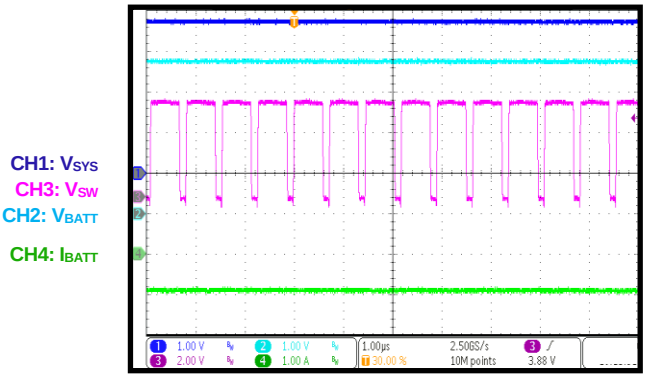


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = full range, I²C-controlled, $I_{CHG}$ = 1.84A, $I_{IN\_LIM}$ = 3.0A, $V_{IN\_MIN}$ = 4.3V, L = 1.0µH (DCR = 14.9mΩ), $T_A$ = 25°C, unless otherwise noted.**

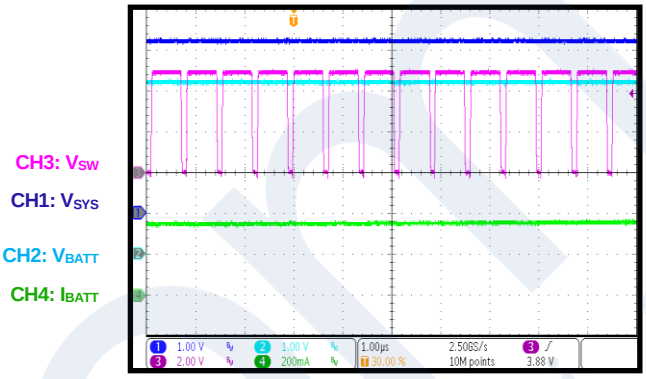
### Battery Supplement Mode

$V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{SYS}$ = 4.5A



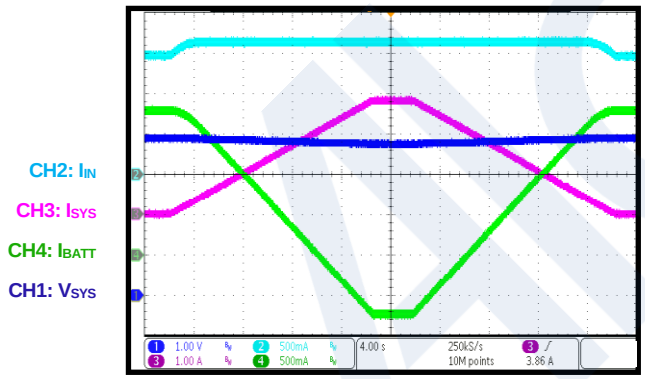

### Constant Voltage Charge

$V_{IN}$ = 5V, $V_{BATT}$ = 4.19V, $I_{SYS}$ = 0A



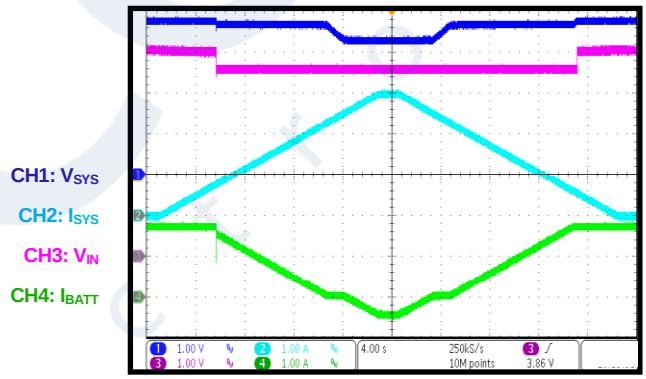

### Input Current Limit

$V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{IN\_LIM}$ = 1800mA



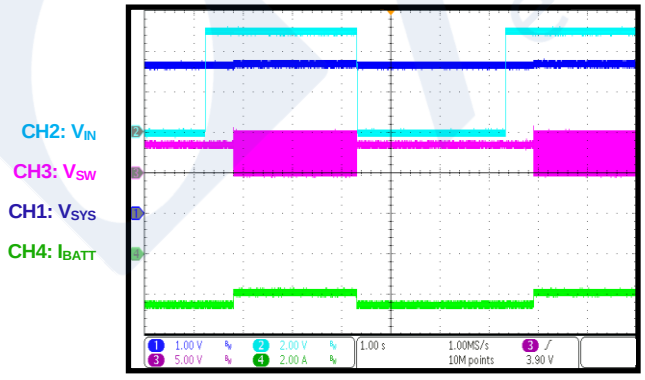

### Input Voltage Limit

$V_{IN}$ = 5V (2A), $V_{BATT}$ = 3.3V, $V_{IN\_MIN}$ = 4.6V



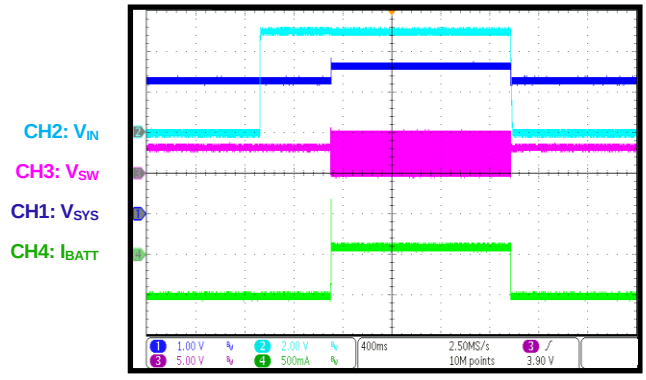

### Power-On/Off Waveform

$V_{IN}$ = 5V, $I_{IN\_LIM}$ = 500mA, $V_{BATT}$ = 3.8V, $I_{SYS}$ = 2.5A




### Power-On/Off Waveform

$V_{IN}$ = 5V, $I_{IN\_LIM}$ = 500mA, $V_{BATT}$ = 3.3V, $I_{SYS}$ = 0.5A

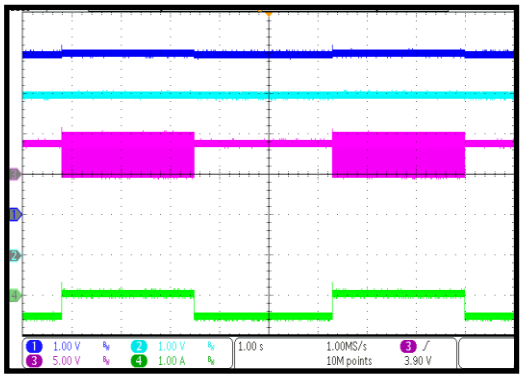


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = full range, I²C-controlled, $I_{CHG}$ = 1.84A, $I_{IN\_LIM}$ = 3.0A, $V_{IN\_MIN}$ = 4.3V, L = 1.0µH (DCR = 14.9mΩ), $T_A$ = 25°C, unless otherwise noted.**

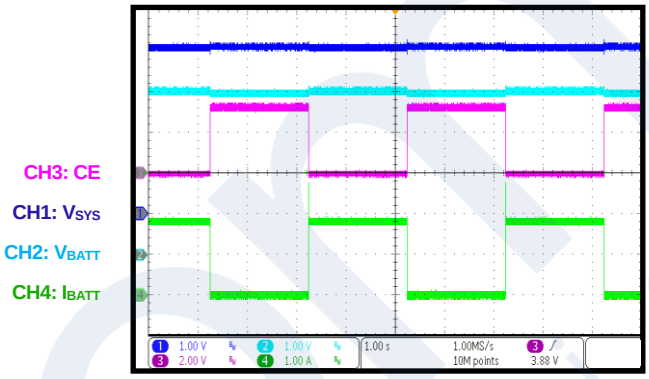
### Suspend Mode On/Off

$V_{IN}$ = 5V, $I_{IN\_LIM}$ = 500mA, $V_{BATT}$ = 4.0V, $I_{SYS}$ = 0.5A



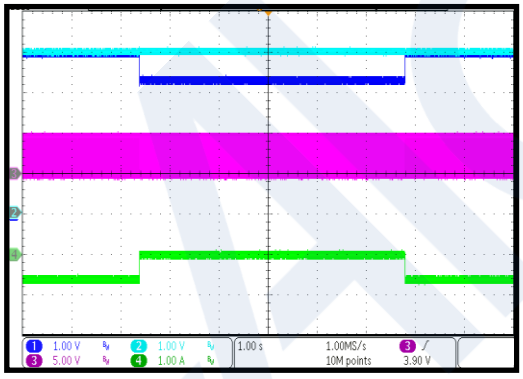

### Charge On/Off

$V_{IN}$ = 5V, $V_{BATT}$ = 4.0V, $I_{SYS}$ = 0A



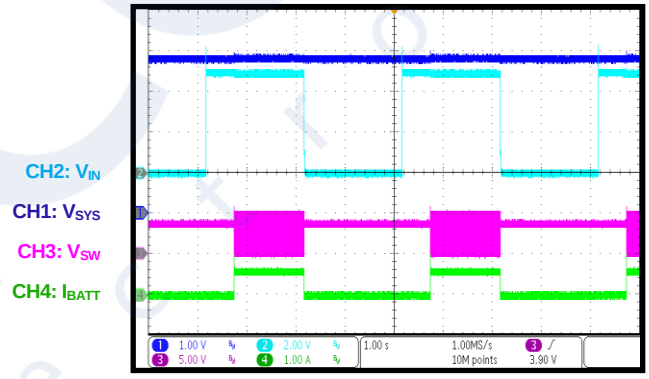

### BATFET On/Off

$V_{IN}$ = 5V, $V_{BATT}$ = 4.0V, $I_{SYS}$ = 4A



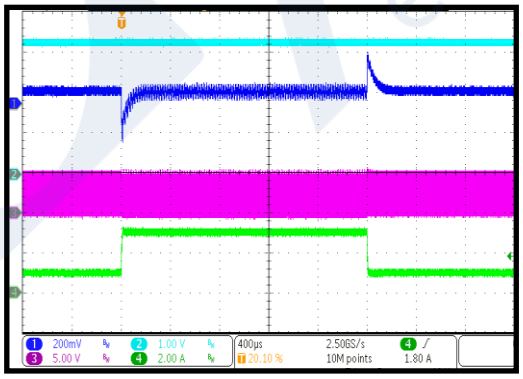

### VIN Hot Insertion/Removal

$V_{IN}$ = 5V, $I_{IN\_LIM}$ = 500mA, $V_{BATT}$ = 3.8V



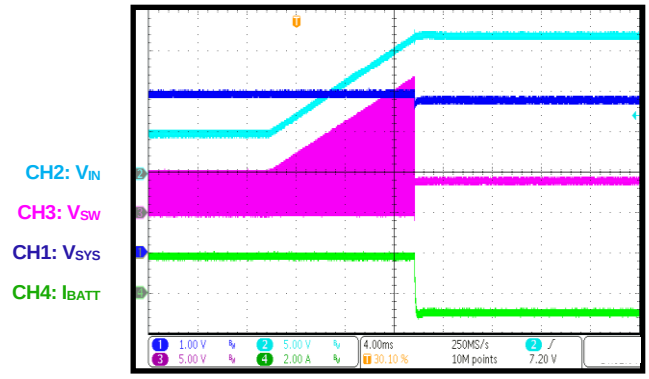

### SYS Load Transient

$V_{IN}$ = 5V, $V_{BATT}$ = 3.3V, charge disable, $I_{SYS}$ = 1A to 3A




### VIN OVP Test

$V_{IN}$ = 5V to 17V, $V_{BATT}$ = 3.8V, $I_{SYS}$ = 1A

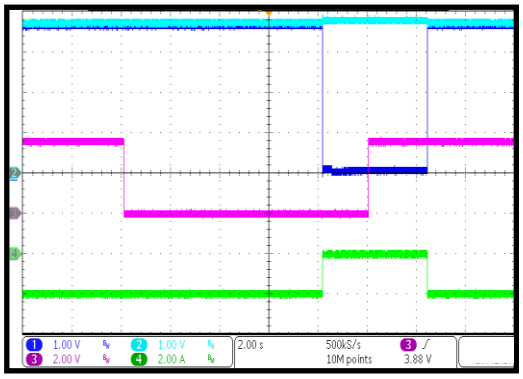


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = full range, I²C-controlled, $I_{CHG}$ = 1.84A, $I_{IN\_LIM}$ = 3.0A, $V_{IN\_MIN}$ = 4.3V, L = 1.0µH (DCR = 14.9mΩ), $T_A$ = 25°C, unless otherwise noted.**

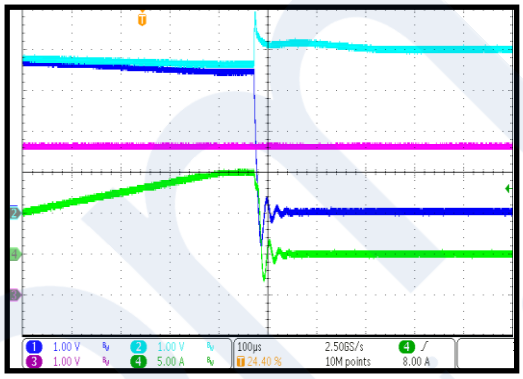
### System Reset Mode

$V_{IN}$ = float, $V_{BATT}$ = 3.8V, $I_{SYS}$ = 2A



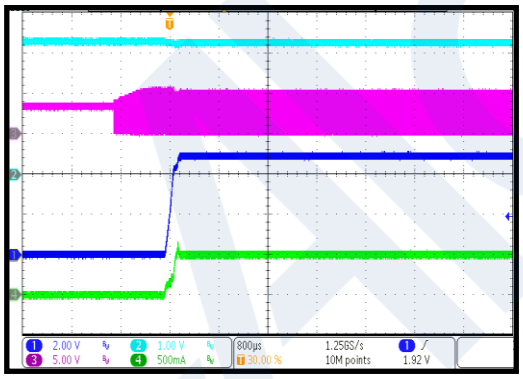

### Battery Discharge Current

$V_{IN}$ = float, $V_{BATT}$ = 4.0V, $I_{SYS}$ = 10A maximum



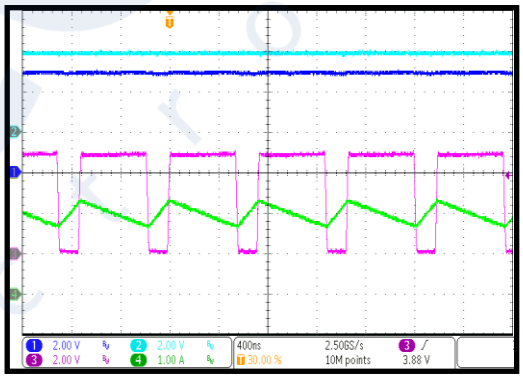

### OTG Mode On

$V_{IN}$ = float, OTG mode, $V_{BATT}$ = 3.3V, $I_{IN\_DSCHG}$ = 0.5A, $I_{OTG}$ = 0.5A



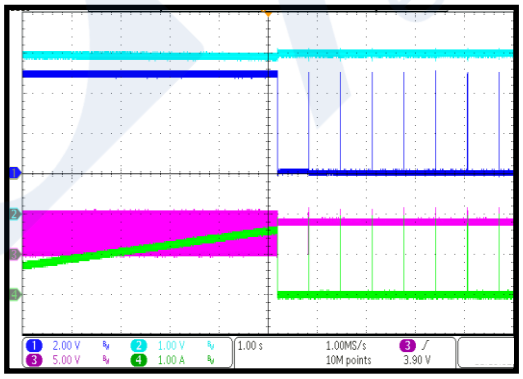

### OTG Steady State Operation

$V_{IN}$ = float, OTG mode, $V_{BATT}$ = 4.0V, $I_{IN\_DSCHG}$ = 3.0A, $I_{OTG}$ = 1.5A



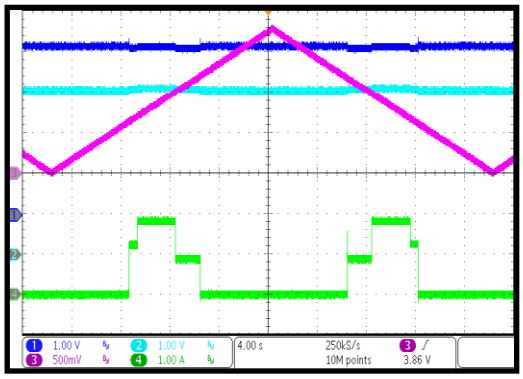

### OTG Voltage Regulation

$V_{IN}$ = float, OTG mode, $V_{BATT}$ = 4.0V, $I_{IN\_DSCHG}$ = 1.5A, $I_{OTG}$ = 0A to 1.5A




### NTC JEITA Operation

$V_{IN}$ = 5V, $V_{BATT}$ = 4.07V, $I_{SYS}$ = 0A , JEITA_ISET = 50%, JEITA_VSET = -100mV



## FUNCTIONAL BLOCK DIAGRAM

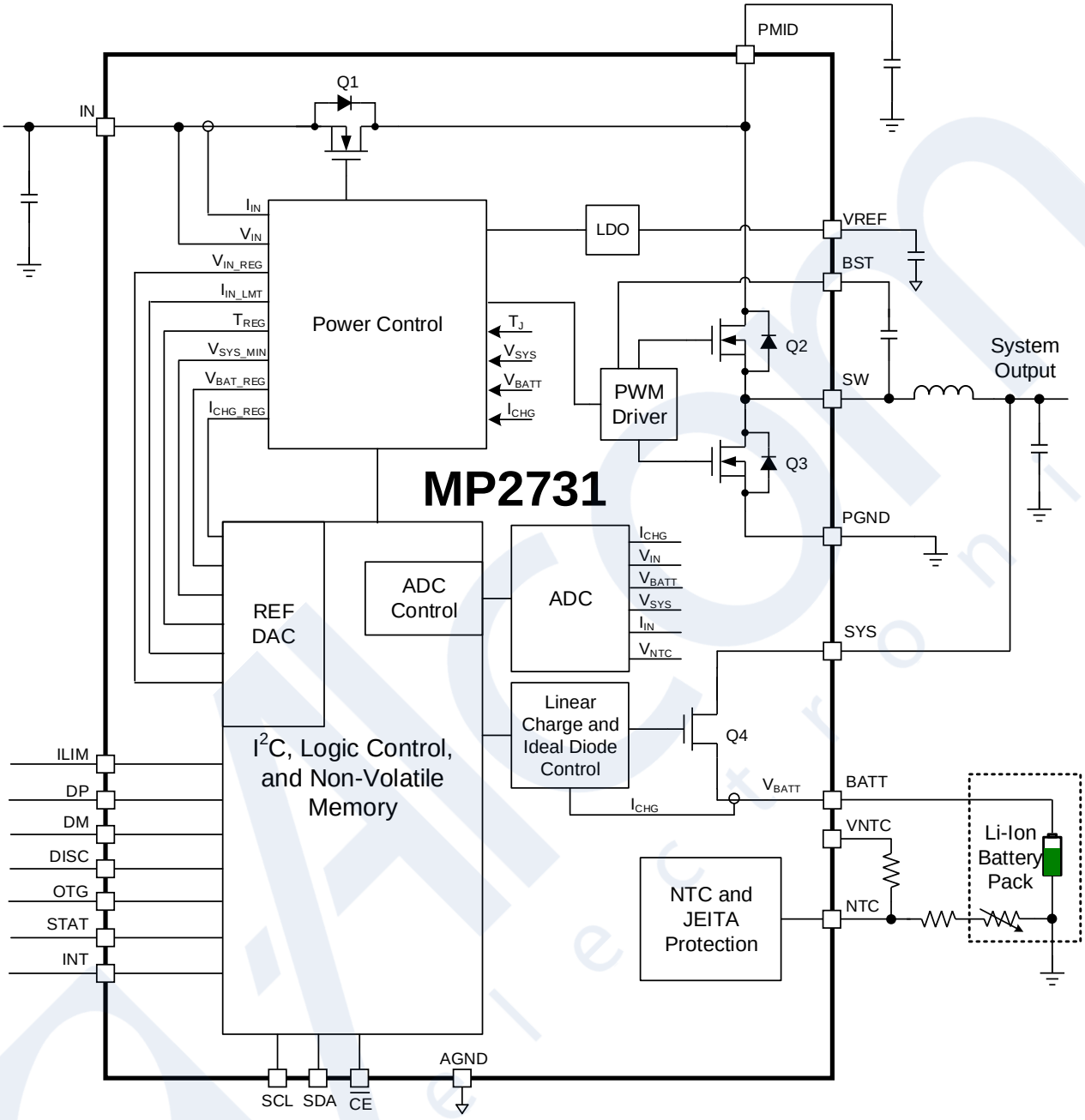



**Figure 1: Functional Block Diagram**

## OPERATION

The MP2731 is a highly integrated, 4.5A, switch-mode battery charger IC with NVDC power path management for single-cell Li-ion or Li-polymer battery applications. The device integrates a reverse blocking FET (Q1), high-side switching FET (Q2), low-side switching FET (Q3), and battery FET (Q4) between the SYS and BATT pins.

### Power Supply

The VREF pin's voltage supplies the internal bias circuits as well as the high-side and low-side MOSFET gate drive. The pull-up rail of STAT can also be connected to VREF. The VREF pin has an internal LDO, which has two inputs. One input is from IN, and the other is from a battery. IN and the battery voltage are connected to the input of the LDO via a PMOS.

Figure 2 shows the VREF power supply circuit.

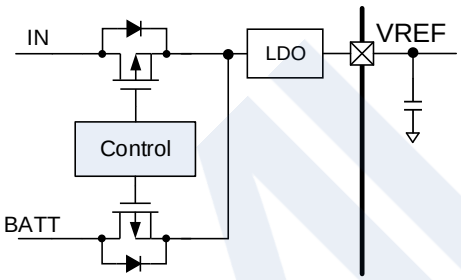



**Figure 2: VREF Power Supply Circuit**

### Device Power-Up from Input Source

When an input source is plugged in, the MP2731 qualifies the input source before start-up. The input source must meet both of the following requirements:

1. $V_{IN} > V_{BATT} + V_{HDRM}$
2. $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$

If the input power source meets the conditions above, a good input is detected and the device asserts an INT signal to the host. Then the device detects the input source type via the DP/DM pins. When DP/DM detection completes, the status register bit (VIN_STAT) changes, and an INT pulse is sent to the host. Then the device starts up the step-down converter.

### NVDC Power Path Management

The MP2731 employs a narrow-voltage DC (NVDC) power structure with the battery FET, decoupling the system from the battery and thus allowing separate controls between the system and the battery. The system is a priority during start-up, even if the battery is deeply discharged or missing. If the input power is available with a depleted battery, the system voltage is regulated at the minimum system voltage ($V_{SYS\_REG\_MIN}$).

Figure 3 shows the NVDC power structure, which is composed of a front-end, step-down DC/DC converter, and a battery FET placed the between SYS and BATT pins.

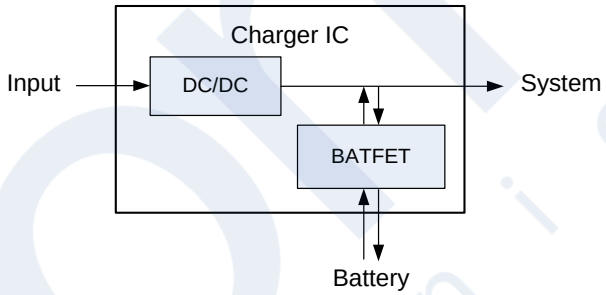



**Figure 3: NVDC Power Path Management Structure**

The DC/DC converter is a 1.35MHz step-down switching regulator, which directly drives the system load and charges the battery through the battery FET.

The system regulates the voltage in the following ways:

1. If the battery voltage drops below $V_{SYS\_MIN}$, the system voltage is regulated at a minimum system voltage ($V_{SYS\_REG\_MIN}$), which exceeds $V_{SYS\_MIN}$ by $V_{TRACK}$. The battery FET works linearly to charge the battery via trickle charge, pre-charge, or fast charge current, depending on the battery voltage. $V_{SYS\_MIN}$ can be set via register REG04h, bits[3:1], and $V_{TRACK}$ can be set via REG04h, bit[0].
2. When the battery voltage exceeds $V_{SYS\_MIN}$ + $V_{BATT\_GD}$ (60mV), the battery FET fully turns on, and the voltage difference between the system and the battery is the $V_{DS}$ of the BATFET. The charge current loop is implemented by the PWM control of the DC/DC converter.
3. If charging is suspended or completed (the battery FET is off), the system voltage is always regulated at its maximum value, ($V_{SYS\_MIN}$, $V_{BATT}$) + $V_{TRACK}$.

Figure 4 illustrates charging voltage regulation.

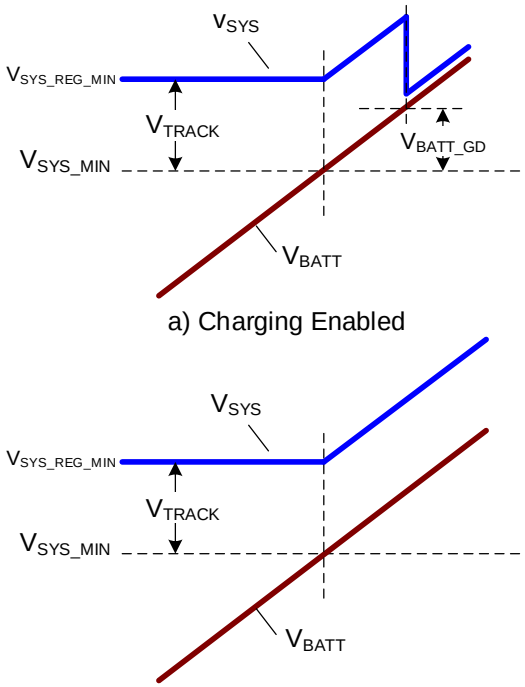



**Figure 4: $V_{SYS}$ Variation with $V_{BATT}$**

### Dynamic Power Management

To meet the maximum current limit in USB specifications and avoid overloading the adapter, the MP2731 features dynamic power management (DPM), and continuously monitors the input current and input voltage. The total input current limit is configurable to prevent the input source from being overloaded. If the input current increases and reaches the input current limit, the charge current is reduced to prioritize the system power.

If the preset input current limit exceeds the adapter's rating, the additional minimum input voltage regulation loop activates to prevent the input power source from being overloaded. When the input voltage falls below the input voltage regulation threshold due to a heavy load, the charge current is reduced to prevent the input voltage from dropping further.

Power path management can operate in two ways:

1. If $V_{BATT} < V_{SYS\_MIN} + V_{BATT\_GD}$, the system voltage is regulated at $V_{SYS\_REG\_MIN}$. If the input current or voltage regulation threshold is reached, the input current loop or input voltage loop controls the DC/DC converter, the system voltage drops, and the battery FET driver is pulled down to decrease the charge current. This prioritizes the system power requirement.
2. This case occurs if the battery is directly connected to the system, and $V_{BATT} > V_{SYS\_MIN} + V_{BATT\_GD}$. Due to the free transition between each control loop, the charge decreases automatically when the input current limit or voltage regulation threshold is reached.

### Battery Supplement Mode

If the device reaches the input current limit or input voltage threshold, the charge current decreases. If the input source is still overloaded when the charge current decreases to zero, the system voltage starts to collapse. If the system voltage drops below the battery voltage, the MP2731 enters battery supplement mode, in which the battery simultaneously powers the system and the DC/DC converter.

The MP2731 can operate in ideal diode mode to optimize the control transition between the battery FET and DC/DC converter. The battery FET enters ideal diode under either of the following conditions:

1. $V_{IN}$ starts up from the battery supply system.
2. $V_{BATT} < V_{SYS\_MIN}$, and the system voltage drops below the battery voltage.

During ideal diode mode, the battery FET operates as an ideal diode, and regulates the gate drive of battery FET. The $V_{DS}$ of the battery FET remains at about 20mV. As the discharge current increases, the battery FET's gate drive increases and its $R_{DS}$ decreases until the battery FET is fully on.

### Battery Charge Profile

If $V_{IN}$ powers on, CHG_CONFIG bit = 01, and the $\overline{CE}$ pin is low, then the device automatically completes a charging cycle without host involvement. However, the host can set different charging parameters to optimize the charge profile by writing to the corresponding registers via the I²C.

A new charge cycle starts when all of the following conditions are valid:

1. Good input power is inserted
2. Battery charging is enabled by the I²C, and $\overline{CE}$ is forced to a low logic
3. No thermistor fault on the NTC pin
4. No safety timer fault
5. BATFET is not forced to turn off

The MP2731 provides four main charging phases: trickle charge, pre-charge, constant current charge, and constant voltage charge, described below:

Phase 1 (trickle charge): When the input power qualifies as a good power supply, the MP2731 checks the battery voltage to determine whether trickle charge is required. If the battery voltage is below $V_{BATT\_TC}$ (2.0V), a trickle-charge current is applied on the battery, which helps reset the protection circuit in the battery pack. The trickle-charge current can be set via REG06h, bit[4]. If REG06h, bit[4] is set to 1, the trickle-charge current is 185mA. If REG06h, bit[4] is set to 0, the trickle-charge current is 145mA.

Phase 2 (pre-charge): If the battery voltage exceeds $V_{BATT\_TC}$, the MP2731 starts to safely pre-charge the depleted battery until the battery voltage reaches the pre-charge to fast charge threshold ($V_{BATT\_PRE}$). If $V_{BATT\_PRE}$ is not reached before the pre-charge timer (1hr) expires, the charge cycle ends and a corresponding timeout fault signal is asserted. The pre-charge current can be configured via I²C register REG06h, bits[7:4], and can be set between 150mA and 750mA.

Phase 3 (constant current charge): If the battery voltage exceeds $V_{BATT\_PRE}$ (set via REG05h, bit[7]), the MP2731 enters a constant current charge (fast-charge) phase. The fast-charge current can be configured to as high as to 4.5A via REG05h, bits[5:0].

There are two stages of fast charge. First, the battery FET works linearly to charge the battery with fast charge current. Once the battery voltage exceeds $V_{SYS\_MIN}$ + $V_{BATT\_GD}$, the battery FET fully turns on. The charge current loop is implemented by the PWM control of the buck converter.

Phase 4 (constant voltage charge): When the battery voltage rises to the configurable float voltage ($V_{BATT\_REG}$) set via REG07h, bits[7:1], the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the battery termination threshold ($I_{TERM}$) set via REG06h, bits[3:0] after a 200ms termination deglitch time, assuming the termination function is enabled if REG08h, bit[7] is set to 1. If $I_{TERM}$ is not reached before the safety charge timer expires (see the Safety Timer section on page 24), the charge cycle ends and a corresponding timeout fault signal is asserted.

Figure 5 shows the charge profile.

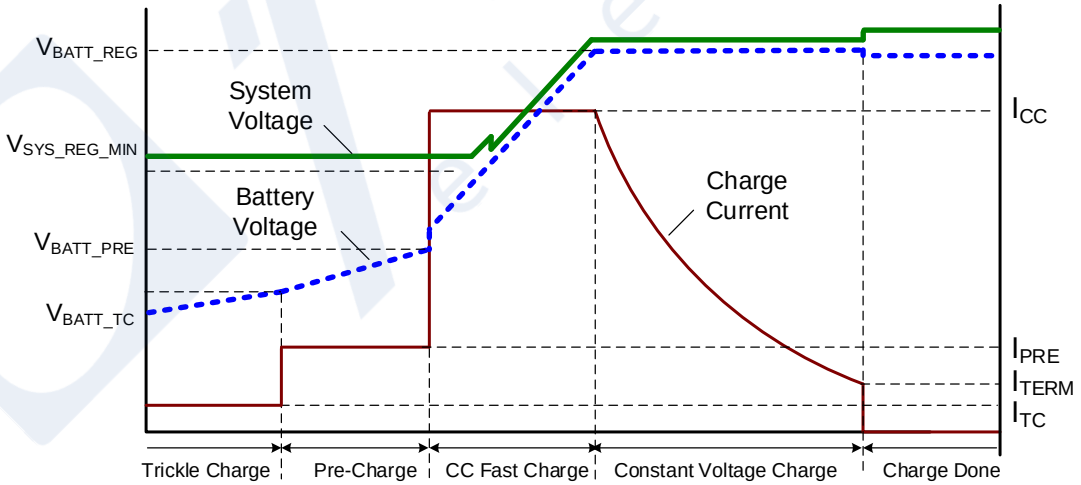



**Figure 5: Battery Charge Profile**

During the charging process, the actual charge current may be less than the register setting due to other loop regulations, like dynamic power management (DPM) regulation (input current limit or input voltage regulation loop) or thermal regulation. The thermal regulation reduces the charge current so that the IC junction temperature does not exceed the preset limit. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirements of different applications. The junction temperature regulation threshold can be set via REG02h, bits[3:2].

### Auto-Recharge

When the battery is done charging, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold after a 200ms auto-recharge deglitch time, the MP2731 automatically starts another charging cycle.

### CE Control

$\overline{CE}$ is a logic input pin that enables or disables battery charging, or restarts a new charging cycle. Battery charging is enabled when CHG_CONFIG (REG04h, bits[5:4]) is set to 01 and the $\overline{CE}$ pin is pulled to logic low.

### Battery Over-Voltage Protection (OVP)

The MP2731 is designed with built-in battery over-voltage protection (OVP). If the battery voltage exceeds 103.5% of $V_{BATT\_REG}$, the MP2731 immediately suspends the charging and asserts a fault. If battery OVP occurs, charging is disabled but the DC/DC converter continues operating.

### System Over-Voltage Protection

The MP2731 monitors the voltage at the SYS pin. If an over-voltage condition ($V_{SYS}$ > $V_{BATT\_REG}$ + 0.4V) is detected, the DC/DC converter turns off and the system is powered by the battery via the battery FET.

### Automatic Input Current Optimizer (AICO)

The device provides an optimized input current limit without overloading the input source. This function can be enabled or disabled by configuring the AICO_EN bit, which is disabled by default. If AICO is enabled, $I_{IN\_LIM}$ is set to a larger current, and the input voltage drops to $V_{IN\_MIN}$, the AICO function is triggered. This function decreases $I_{IN\_LIM}$ step by step until the input voltage exits $V_{IN\_MIN}$ control. The input current limit remains optimized and does not automatically run the AICO function unless another $V_{IN\_MIN}$ event occurs.

The actual input current limit is reported in the $I_{IN\_DPM}$ register when the AICO function is enabled (AICO_EN = 1). If the AICO function is disabled (AICO_EN = 0), the input current limit is set by the $I_{IN\_LIM}$ register. Any write to $I_{IN\_LIM}$ can reset $I_{IN\_DPM}$ to the same $I_{IN\_LIM}$ value when the AICO function is enabled.

### Input Source Type Detection

The MP2731 features input source detection compatible with USB Battery Charging Specification 1.2 (BC1.2) and nonstandard adapters. The user can force DP/DM detection in the host mode by writing 1 to the USB_DET_EN bit (REG0Bh, bit[5]).

When the input voltage is first applied and a good input source is detected, BC1.2 detection first begins with data content detection (DCD). If DCD is effective, the standard downstream port (SDP), charging downstream port (CDP), and dedicated charging port (DCP) can be distinguished. If the 500ms DCD timer expires, then the MP2731 proceeds with nonstandard adapter detection.

DCD uses a current source to detect when the data pins have made contact during an attach event. The protocol for DCD is as follows:

1. The portable device (PD) detects $V_{IN}$ assertion.
2. The PD turns on DP $I_{DP\_SRC}$ and the DM pull-down resistor.
3. The PD waits for the DP line to be low.
4. If the DP line is detected low for 10ms, the PD starts primary detection.
5. If data contact is not detected, the DCD timer (500ms) expires.

After the DCD timer expires, the PD turns off $I_{DP\_SRC}$ and the DM pull-down resistor. Then the 50ms timer starts, and the PD can detect a special adapter. If a special adapter is detected, an INT is sent to the host. Otherwise, the PD starts primary detection after the 50ms timer expires.

Primary detection is used to distinguish between USB hosts (or the SDP) and different types of charging ports. During primary detection, the IC turns on $V_{DP\_SRC}$ on DP, and $I_{DM\_SINK}$ on DM. If the portable device is attached to a USB host, the DM pin pulls low. The SDP is detected, and an INT signal is sent to the host.

If the DM pin is high, the IC goes into secondary detection, which distinguishes between a CDP and a DCP.

During secondary detection, the IC turns on $V_{DM\_SRC}$ on DM, and $I_{DP\_SINK}$ on DP. If the input source is a CDP port and DP is low, then the CDP is detected and an INT signal is sent to the host.

If DP is high, the DCP source is detected, and an INT is sent to host. In this case, after turning off $V_{DM\_SRC}$ and $I_{DP\_SINK}$, $V_{DP\_SRC}$ is applied to DP, and the IC goes to fast-charge detection.

Fast-charge detection identifies whether the input source has fast-charge capability.

If DM is always high during fast-charge detection, the input source has no fast-charge capability. If DM is low for 40ms, and the input source has fast-charge capability, the MP2731 sends an INT signal to the host. The MP2731 features an I²C-configurable DP/DM output for host-controlled communication, with various fast-charge protocols.

Table 1 lists input current limits that are compatible with USB specifications and BC1.2.

**Table 1: Input Current Limit vs. USB Type**

| DP/DM Detection | $I_{IN\_LIM}$ (A) | $V_{IN\_OVP}$ (V) | $V_{IN\_MIN}$ (V) |
|---|---|---|---|
| Nonstandard adapter (1A) | 1 | 6 | 3.7 to 5.2 |
| Nonstandard adapter (2.1A) | 2.1 | 6 | 3.7 to 5.2 |
| Nonstandard adapter (2.4A) | 2.4 | 6 | 3.7 to 5.2 |
| SDP | 0.5 | 6 | 3.7 to 5.2 |
| CDP | 1.5 | 6 | 3.7 to 5.2 |
| DCP | 1.8 | 6 | 3.7 to 5.2 |

USB detection is independent of the charge enable status. After DP/DM detection completes, the MP2731 indicates the USB port type in status register VIN_STAT (REG0Ch, bits[7:5]), and asserts an INT signal to the host. The host can revise the input current limit according to VIN_STAT.

### Input Current Limit Setting via ILIM

For safe operation, the MP2731 has an additional hardware pin (ILIM) to adjust the maximum input current limit. The limit can be set by connecting a resistor from ILIM to GND. The actual input current limit is the lower value between what is set by the ILIM pin and the value set by the I²C.

The current limit set by the ILIM pin can be calculated with Equation (1):

$$I_{IN\_LIM} = \frac{120}{R_{ILIM}(k\Omega)}(A) \quad (1)$$

### Battery Temperature Monitor in Charge Mode

The MP2731 continuously monitors the battery's temperature by measuring the voltage at the NTC pin. This value is typically determined by a negative temperature coefficient (NTC) thermistor and external voltage dividers. For the NTC thermistor, a hotter ambient temperature corresponds with a lower resistance and voltage ratio, and vice versa.

Figure 6 shows an NTC protection circuit. The external resistor dividers and the internal reference resistor series are pulled up to the VNTC pin. The voltage ratios between the internal and external dividers are compared to determine if an NTC protection has been triggered. The VNTC voltage (1.7V) is regulated by an LDO that is powered from VREF. The VNTC pin is available in both charge mode and OTG mode.

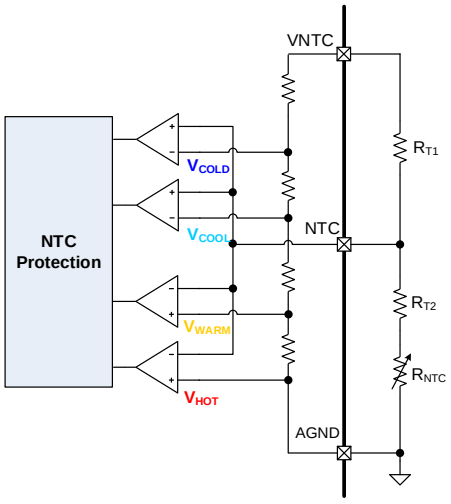



**Figure 6: NTC Protection Circuit**

The MP2731 provides standard and JEITA battery temperature monitoring, which can be selected by the NTC_TYPE bit. If the standard type is selected, and the external voltage ratio transitions from the high temperature threshold ($V_{HOT}$) to the low temperature threshold ($V_{COLD}$), this means that the battery temperature is out of the cold-to-hot range. The IC suspends charging and reports the NTC fault. Charging resumes automatically once the battery temperature is within the cold-to-hot temperature range again.

If the JEITA type is selected, the MP2731 monitors four temperature thresholds: the cold temperature threshold ($T_{NTC}$ < 0°C, default), the cool temperature threshold (0°C < $T_{NTC}$ < 15°C, default), the warm temperature threshold (45°C < $T_{NTC}$ < 55°C, default), and the hot temperature threshold ($T_{NTC}$ > 55°C, default).

For a given NTC thermistor, these temperatures correspond to the values for $V_{COLD}$, $V_{COOL}$, $V_{WARM}$, and $V_{HOT}$. These voltage thresholds can be configured via REG16h, bits[5:0] to set different temperature ranges.

If $V_{NTC}$ < $V_{HOT}$ or $V_{NTC}$ > $V_{COLD}$, the charging and timers are suspended. If $V_{HOT}$ < $V_{NTC}$ < $V_{WARM}$, the battery regulation voltage ($V_{BATT\_REG}$) is reduced by 200mV, which can be configured via REG16h, bit[7]. If $V_{COOL}$ < $V_{NTC}$ < $V_{COLD}$, the charging current is reduced to 16.7%, which can be configured via REG16h, bit[6]. Figure 7 shows JEITA control.

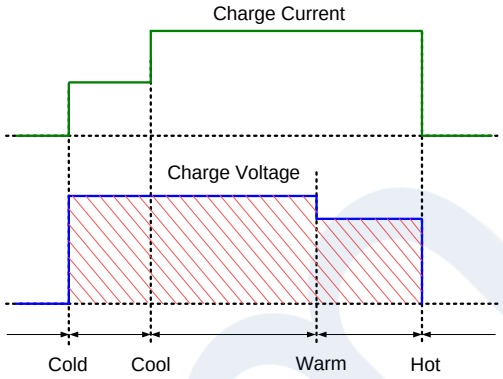



**Figure 7: NTC Window under JEITA Control**

The MP2731 provides PCB over-temperature monitoring. The PCB over-temperature response is selected by the NTC OPT bit (REG02h, bit[1]). If this bit is set to 1, PCB over-temperature protection is enabled. If this bit is set to 0 (the default setting), the battery temperature monitoring and corresponding protection features mentioned above are utilized instead.

While monitoring over-temperature conditions in the PCB, the IC continuously monitors the PCB temperature at the NTC pin. If the NTC pin voltage is below the threshold that reuses $V_{HOT}$, the DC/DC converter and battery FET turn off. Operation resumes once the NTC pin voltage returns to the normal value.

If the NTC thermistor is removed, NTC is pulled up to VNTC (see Figure 6). If the NTC voltage exceeds 95% of VNTC, then the NTC thermistor float is detected. The MP2731 sends an INT signal to the host, and the RNTC FLOAT_STAT bit is set to 1.

### Battery Temperature Monitor in OTG Boost Mode

In boost mode, the device monitors the battery temperature to be within the $V_{COLD}$ and $V_{HOT}$ thresholds unless boost mode temperature monitoring is disabled by setting EN_OTG NTC (REG02h, bit[5]) to 0. If the temperature is outside of the temperature thresholds, boost mode is suspended. Once the temperature is within the thresholds again, boost mode resumes.

### Charging STAT Indication

The MP2731 indicates the charging state on the open-drain STAT pin. Table 2 shows the STAT status. The STAT pin function can be disabled by setting the STAT_EN bit to 0.

**Table 2: Operation Indications**

| Charging State | STAT |
|---|---|
| Charging | Low |
| Charging complete, charge disabled, input OVP, battery discharge mode | High |
| Charging suspended (battery OVP, system OVP, timer fault, NTC fault, NTC float) | Blinking at 1Hz |

### Interrupt to Host (INT)

The MP2731 also has an alert mechanism that can output an interrupt signal via the INT pin to notify the system of the operation by outputting a 256μs, low-state INT pulse. The events that can trigger an INT output are listed below:

- Good input source detected
- DP/DM USB detection completed
- Input removed
- Charge completed
- NTC float is detected
- VINPPM or IINPPM is reached
- Any fault in REG0Dh (watchdog timer fault, OTG fault, thermal shutdown, safety timer fault, battery OVP fault, NTC fault)

If a fault occurs, the charger device sends out INT signal. The fault is not latched, and always reports the current conditions.

### Safety Timer

The MP2731 provides both a pre-charge and complete charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is 1 hour when the battery voltage is below $V_{BATT\_PRE}$. The complete charge safety timer starts when the battery enters constant current charge. The user can configure the constant current charge safety timer via the CHG_TMR bit (REG08h, bits[2:1]) through the I²C. If the safety timer function is not used, it can be disabled by EN_TIMER (REG08h, bit[0]) via the I²C during initializing charger configuration.

The safety timer is reset at the beginning of a new charging cycle. Before the safety timer expires, any of the actions listed below can reset the safety timer:

- A new charge cycle begins by either input insertion or automatic recharge
- Toggling the $\overline{CE}$ pin low to high to low (charge enabled)
- Writing CHG_CONFIG (REG04h, bits[5:4]) from 00 to 01 (charge enabled)
- Writing EN_TIMER (REG08h, bit[0]) from 0 to 1 (safety timer enabled)

When safety timer expires, the safety timer fault bit (REG17h, bit[7]) is set to 1 and an INT is asserted to the host. Writing the BG_EN bit (REG09h, bit[3]) from 1 to 0 or re-inserting the input re-enables the input detection, clears the safety timer fault and restarts the safety timer.

The MP2731 automatically adjusts or suspends the timer if any fault occurs. The timer is suspended if any of the following conditions are met:

- Battery enters supplement mode and $V_{BATT} < V_{SYS\_MIN}$
- Battery over-voltage protection (OVP) occurs
- NTC hot or cold fault occurs
- NTC floats
- Writing EN_TIMER (REG08h, bit[0]) from 1 to 0

The MP2731 provides a way to double the remaining time left on the timer, which is enabled by the TMR2X_EN bit. If the input current limit, input voltage regulation, or thermal regulation threshold is reached, the remaining time on the timer is doubled when TMR2X_EN is enabled. Once the device is cleared of the above conditions, the remaining time returns to the original setting.

The safety timer does not operate in USB OTG mode.

### Watchdog Timer

The MP2731 is a host-controlled device, but it can operate in a default mode without host control. In default mode, all registers are in the default settings, and the WATCHDOG_FAULT command is set to 1.

In host-controlled mode, all the parameters can be configured by the host. To keep the device in host mode, the host has to periodically reset the watchdog timer by setting the WATCHDOG

TIMER RESET bit (REG08h, bit[3]) to 1 before the watchdog timer expires. If the watchdog timer expires, some of the registers will reset their values to default. See the I²C Register Map on page 29 to check which register is reset after the watchdog timer expires.

The following actions reset the watchdog timer and make the IC recover from a watchdog timer fault.

- Writing 1 to the WATCHDOG TIMER RESET bit (REG08h, bit[3])
- Toggling the WATCHDOG TIMER ENABLE bit (disable first, then enable)

### Thermal Regulation and Thermal Shutdown

The MP2731 continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. If the internal junction temperature reaches the thermal regulation threshold (set by the $T_{J\_REG}$ bit), the MP2731 starts to reduce the charge current to prevent higher power dissipation. During thermal regulation, the THERM_STAT bit is set to 1.

If the junction temperature reaches thermal shutdown threshold $T_{J\_SHDN}$ (150°C), the MP2731 turns off the PWM step-down converter and BATFET. The THERMAL SHUTDOWN bit in the fault register is set to 1, and an INT signal is asserted to host. The step-down converter and BATFET resume normal operation when the junction temperature drops below the $T_{J\_SHDN}$ hysteresis threshold.

### Battery Discharge Mode

If only the battery is connected, and $V_{BATT}$ exceeds the $V_{BATT\_UVLO}$ threshold, then the battery FET turns on and connects the battery to the system. The 14mΩ battery FET minimizes the conduction loss during discharge. The MP2731's quiescent current goes as low as 40μA. The low on resistance and low quiescent current help extend battery runtime.

There is an over-current limit designed in the MP2731 to avoid system over-current conditions while the battery discharges. If the discharge current exceeds this limit ($I_{DSCHG\_LMT}$) after a 50μs blanking time, the discharge FET turns off and enters hiccup mode. After a 600ms recovery time, the discharge FET turns on again. If the discharge current goes high to reach the internal fast-off current limit (14A), the battery FET turns off immediately and enters hiccup mode.

### Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode, or to allow the reset of system power during operation. The MP2731 provides both shipping mode and system reset mode for different applications.

The MP2731 can enter and exit shipping mode through I²C control of the BATFET_DIS bit (REG0Ah, bit[5]). Writing 1 to BATFET_DIS turns off the battery FET after a 10s delay. In battery discharge mode, the delay time is configured by the $t_{SM\_DLY}$ bit. Writing 0 to BATFET_DIS turns the battery FET on again.

In an application that requires a system power reset, the MP2731 uses a dedicated DISC pin to cut off the path from the battery to the system.

System reset function has two options, which can be selected via SYSRST_SEL bit (REG0Ah, bit[4]). If SYSRST_SEL is set to 1, once the logic at DISC is pulled low for more than 8s — programmable by the $t_{DISC\_L}$ bit (REG0Ah, bits[1:0]) — then the system is disconnected from the battery by turning off the battery FET. After a 4s low period, which can be programmed by $t_{DISC\_H}$ bit (REG0Ah, bits[3:2]), the battery FET automatically turn on (see Figure 8).

If the SYSRST_SEL bit (REG0Ah, bit[4]) is set to 0, and the logic at DISC is pulled low longer than the time programmed by the $t_{DISC\_L}$ bit, the battery FET turns off. Once the logic at DISC is pulled low again for time set by the $t_{DISC\_H}$ bit, the battery FET turns on (see Figure 9).

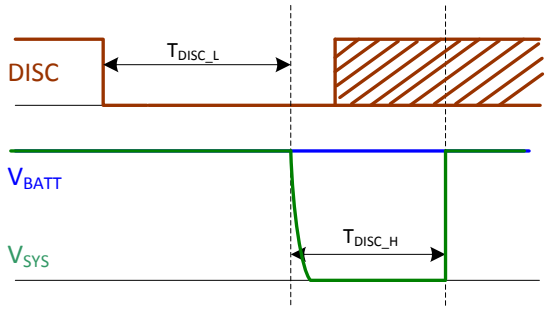



**Figure 8: System Software Reset (SYSRST_SEL = 1)**

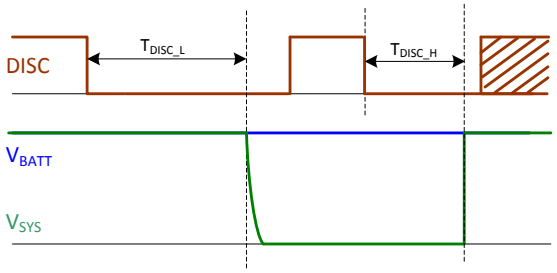



**Figure 9: System Hardware Reset (SYSRST_SEL = 0)**

### OTG Boost Function

The MP2731 can supply a regulated 5V output at the IN pin to power the peripherals. This output is compliant with USB On-The-Go (OTG) specifications. The MP2731 does not enter OTG mode if the battery is below the battery under-voltage lockout (UVLO) threshold, to ensure that the battery is not drained. To enable OTG mode, the input voltage at the IN pin must be below 1.0V.

Boost operation can be enabled when the CHG_CONFIG bit = 11 (REG04h, bits[5:4] = 11) and the OTG pin is high. The OTG output current limit can be configured by the $I_{IN\_DSCHG}$ bit (REG03h, bits[1:0]) via the I²C. During boost mode, status register VIN_STAT (REG0Ch, bits[7:5]) changes to 111.

The following conditions must be met to enable boost operation:

- $V_{BATT} > V_{BATT\_UVLO\_OTG}$ (rising 3V)
- $V_{IN} < 1V$
- OTG pin is high and CHG_CONFIG (REG04h, bits[5:4]) is set to 11
- Boost mode is enabled after a 200ms delay

Once OTG is enabled, the MP2731 boosts the PMID to 5.0V. Then the block FET (Q1) is linearly regulated with a 3A output current limit. If $V_{IN}$ is charged above 4.4V within 6ms, the block FET fully turns on. Otherwise, the block FET turns off, and the part goes into hiccup mode. After a 600ms off period, PMID tries to charge $V_{IN}$ again.

The MP2731 provides OTG output short protection. If $V_{IN}$ falls below 4.0V, the block FET and boost turn off, and the part enters hiccup mode. After a 600ms recovery time, OTG starts up again. When the OTG output is short, the fault register's OTG_FAULT bit (REG0Dh, bit[6]) is set to 1, and an INT signal is sent to the host. The device also provides OTG output voltage protection. Once $V_{IN}$ exceeds $V_{INOVP\_DSCHG}$, the MP2731 stops switching, the fault register OTG_FAULT bit (REG0Dh, bit[6]) is set to 1, and an INT signal is sent to the host.

In boost mode, the MP2731 employs a fixed, 1.35MHz, PWM step-up switching regulator. It switches from PWM operation to pulse-skip operation at light-load.

### ADC

The MP2731 integrates an 8-bit ADC, which is available in charge mode and OTG mode. In charge mode, the ADC monitors input voltage, input current, system voltage, battery voltage, charge current and NTC voltage alternatively. In OTG mode, the ADC monitors battery voltage, system voltage, NTC voltage and input voltage. When ADC functionality is available, the ADC can be controlled by the ADC_START bit.

ADC operation has two modes, which can be selected by ADC_RATE. If ADC_RATE is set to 0, the ADC acts once an I²C command is issued. If ADC_RATE is set to 1, ADC always acts in a round-robin manner.

### Series Interface

The IC uses an I²C-compatible interface to set the charging parameters and instantaneously report the device status. The I²C is a two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and serial clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device and receives control inputs from the master device, such as a microcontroller. The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbits/s) and fast mode (up to 400kbits/s).

All transactions begin with a start (S) condition and are terminated by a stop (P) condition. Start and stop conditions are always generated by the master. A start condition is defined as a high-to-low transition on the SDA line while SCL is high. A stop condition is defined as a low-to-high transition on the SDA line while the SCL is high (see Figure 10).

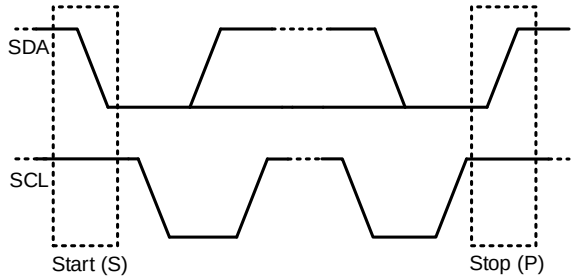



**Figure 10: Start and Stop Conditions**

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 11). Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is first transferred with the most significant bit (MSB).

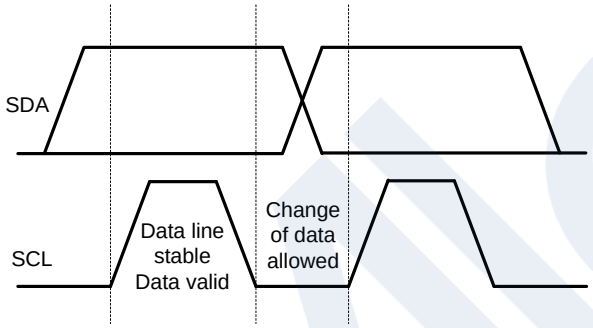



**Figure 11: Bit Transfer on the I²C Bus**

Each byte has to be followed by an acknowledge (ACK) bit, which is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal occurs when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low. The SDA line stays low during the high period of the ninth clock.

If the SDA line is high during the ninth clock, this is defined as a not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer or a repeated start (Sr) condition to start a new transfer.

After the start condition, a slave address is sent. This address is 7 bits long, followed by the 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 12 shows the address bit arrangement.

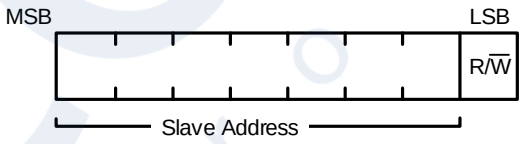



**Figure 12: 7-Bit Addressing**

See Figure 13, Figure 14, Figure 15, Figure 16, and Figure 17 on page 27 for detailed sequences.

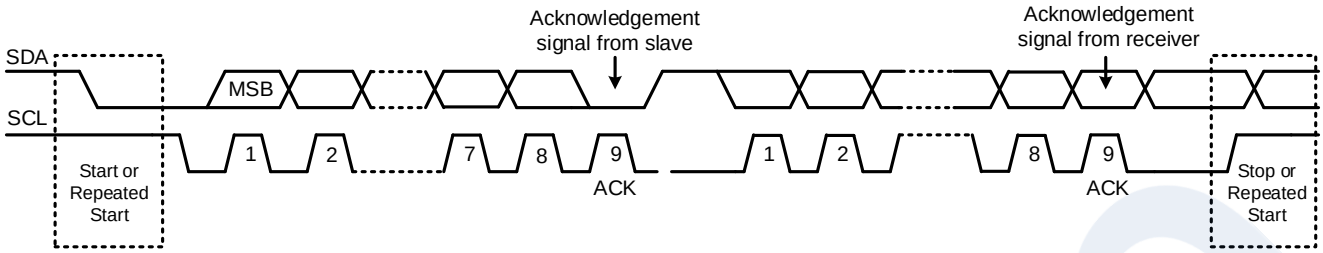



**Figure 13: Data Transfer on the I²C Bus**

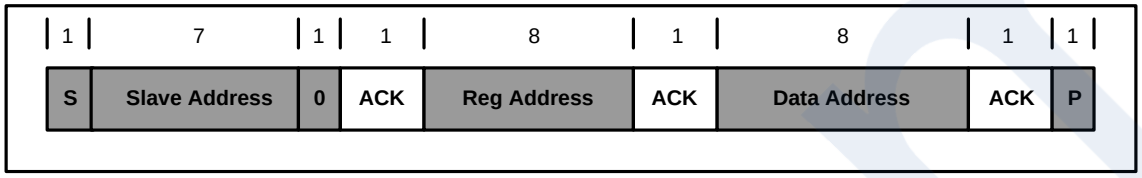



**Figure 14: Single Write**


**Figure 15: Single Read**

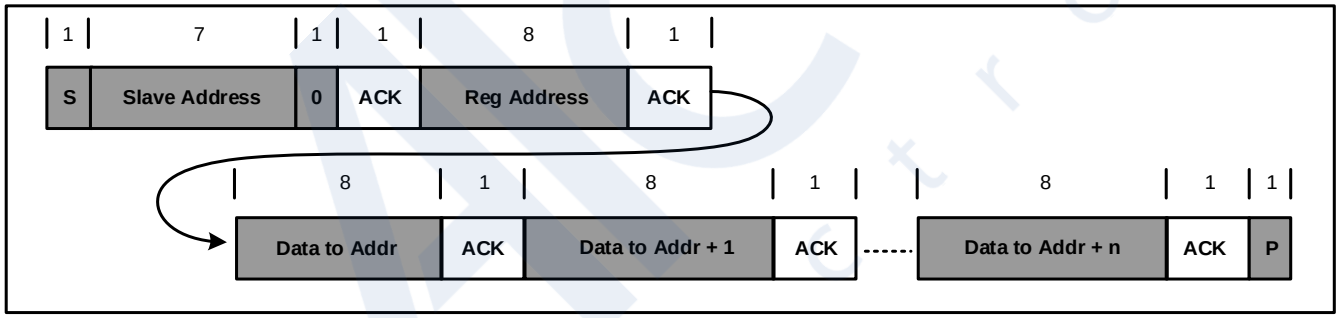



**Figure 16: Multi Write**

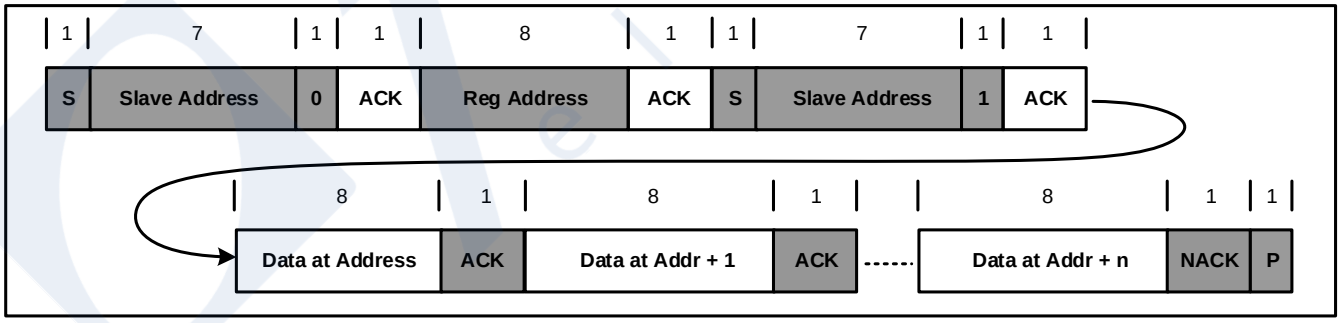



**Figure 17: Multi Read**

## I²C REGISTER MAP

| IC Address 4Bh Register Name | Address | R/W | Description |
|---|---|---|---|
| REG00h | 0x00 | R/W | Input current limit. |
| REG01h | 0x01 | R/W | Input voltage regulation. |
| REG02h | 0x02 | R/W | NTC configuration and thermal regulation. |
| REG03h | 0x03 | R/W | ADC control and OTG configuration. |
| REG04h | 0x04 | R/W | Charge control and VSYS configuration. |
| REG05h | 0x05 | R/W | Charge current configuration. |
| REG06h | 0x06 | R/W | Pre-charge and termination current. |
| REG07h | 0x07 | R/W | Charge voltage regulation. |
| REG08h | 0x08 | R/W | Timer configuration. |
| REG09h | 0x09 | R/W | Bandgap. |
| REG0Ah | 0x0A | R/W | BATFET configuration. |
| REG0Bh | 0x0B | R/W | INT MASK and USB detection |
| REG0Ch | 0x0C | R | Status. |
| REG0Dh | 0x0D | R | Fault. |
| REG0Eh | 0x0E | R | ADC of battery voltage. |
| REG0Fh | 0x0F | R | ADC of system voltage. |
| REG10h | 0x10 | R | ADC of NTC voltage. |
| REG11h | 0x11 | R | ADC of input voltage. |
| REG12h | 0x12 | R | ADC of charge current. |
| REG13h | 0x13 | R | ADC of input current. |
| REG14h | 0x14 | R | Power management status. |
| REG15h | 0x15 | R/W | DPM mask. |
| REG16h | 0x16 | R/W | JEITA configuration. |
| REG17h | 0x17 | R | Safety timer status and part number. |

### REG00h: Input Current Limit

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | EN_HIZ | 0 | Y | Y | R/W | 0: Disable<br>1: Enable | Hi-Z mode enable bit. Set to 0 by default. This bit only turns off the DC/DC converter. |
| 6 | EN_LIM | 1 | Y | Y | R/W | 0: Disable<br>1: Enable | Enable bit for the ILIM pin. This bit is set to 1 by default. The charger input current limit is the lower value between the IIN_LIM register setting and ILIM pin setting. |
| 5 | $I_{IN\_LIM}$[5] | 0 | Y | N | R/W | 1600mA | This bit sets the input current limit threshold. It has a 100mA offset, a 500mA default, and a 100mA to 3.25A range via the one-time programmable (OTP) memory. $V_{IN}$ POR can reset $I_{IN\_LIM}$ to the default via the OTP. |
| 4 | $I_{IN\_LIM}$[4] | 0 | Y | N | R/W | 800mA | |
| 3 | $I_{IN\_LIM}$[3] | 1 | Y | N | R/W | 400mA | |
| 2 | $I_{IN\_LIM}$[2] | 0 | Y | N | R/W | 200mA | |
| 1 | $I_{IN\_LIM}$[1] | 0 | Y | N | R/W | 100mA | |
| 0 | $I_{IN\_LIM}$[0] | 0 | Y | N | R/W | 50mA | |

### REG01h: Input Voltage Regulation

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | REGISTER RESET | 0 | Y | N | R/W | 0: Keep current setting<br>1: Reset | This bit is set to 0 by default. |
| 6 | $V_{IN\_MIN}$ [6] | 0 | Y | N | R/W | 6400mV | This bit sets the input voltage limit threshold. It has a 3.7V offset, 3.7V to 15.2V range, and is set to 0000110 (4.3V) by default via the OTP. $V_{IN}$ POR can reset $V_{IN\_MIN}$ to its default value via the OTP. |
| 5 | $V_{IN\_MIN}$ [5] | 0 | Y | N | R/W | 3200mV | |
| 4 | $V_{IN\_MIN}$ [4] | 0 | Y | N | R/W | 1600mV | |
| 3 | $V_{IN\_MIN}$ [3] | 0 | Y | N | R/W | 800mV | |
| 2 | $V_{IN\_MIN}$ [2] | 1 | Y | N | R/W | 400mV | |
| 1 | $V_{IN\_MIN}$ [1] | 1 | Y | N | R/W | 200mV | |
| 0 | $V_{IN\_MIN}$ [0] | 0 | Y | N | R/W | 100mV | |

## REG02h: NTC Configuration and Thermal Regulation

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | $t_{SM\_DLY}$ | 1 | Y | Y | R/W | 0: No delay<br>1: 10s delay | This bit sets the shipping mode entry delay time. It is set to 1 by default. |
| 6 | NTC_TYPE | 1 | Y | Y | R/W | 0: Standard<br>1: JEITA | This bit is set to 1 by default. |
| 5 | EN_OTG NTC | 0 | Y | Y | R/W | 0: Disabled<br>1: Enabled | OTG NTC enable bit. This bit is set to 0 by default. |
| 4 | EN_CHG NTC | 1 | Y | Y | R/W | 0: Disabled<br>1: Enabled | Charge NTC enable bit. This bit is set to 1 by default. |
| 3 | $T_{J\_REG}$ [1] | 1 | Y | Y | R/W | 00: 60°C<br>01: 80°C<br>10: 100°C<br>11: 120°C | Thermal regulation threshold. This bit is set to 11 by default. |
| 2 | $T_{J\_REG}$ [0] | 1 | Y | Y | R/W | | |
| 1 | NTC OPT | 0 | Y | Y | R/W | 0: Battery OTP<br>1: PCB OTP | NTC option selection bit. This bit is set to 0 by default. |
| 0 | AICO_EN | 0 | Y | N | R/W | 0: Disable AICO<br>1: Enable AICO | Automatic input current optimization enable bit. This bit is set to 0 by default. |

## REG03h: ADC Control and OTG Configuration

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | ADC_START | 0 | Y | Y | R/W | 0: Disable ADC<br>1: Enable ADC | ADC enable bit. Set to 0 by default. This bit is read-only when ADC_RATE = 1. This bit stays high during ADC conversion. |
| 6 | ADC_RATE | 0 | Y | Y | R/W | 0: One-shot conversion<br>1: Start continuous conversion | This bit sets the ADC conversion rate. This bit is set to 0 by default. |
| 5 | $V_{IN\_DSCHG}$ [2] | 0 | Y | Y | R/W | 400mV | This bit sets the On-the-Go (OTG) voltage. The offset is 4.8V, the default is 5.0V (010), and the range is 4.8V to 5.5V. |
| 4 | $V_{IN\_DSCHG}$ [1] | 1 | Y | Y | R/W | 200mV | |
| 3 | $V_{IN\_DSCHG}$ [0] | 0 | Y | Y | R/W | 100mV | |
| 2 | $I_{IN\_DSCHG}$[2] | 0 | Y | Y | R/W | 000: 0.5A<br>001: 0.8A<br>010: 1.1A<br>011: 1.5A<br>100: 1.8A<br>101: 2.1A<br>110: 2.4A<br>111: 3.0A | This bit sets the On-the-Go (OTG) current limit. Set to 000 by default. |
| 1 | $I_{IN\_DSCHG}$[1] | 0 | Y | Y | R/W | | |
| 0 | $I_{IN\_DSCHG}$[0] | 0 | Y | Y | R/W | | |

### REG04h: Charge Control and VSYS Configuration

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | BAT_LOADEN | 0 | Y | Y | R/W | 0: Disable $I_{BATLOAD}$<br>1: Enable $I_{BATLOAD}$ | Battery load enable bit. Set to 0 by default. |
| 6 | STAT_EN | 1 | Y | Y | R/W | 0: Disabled<br>1: Enabled | STAT pin enable bit. Set to 1 by default. |
| 5 | CHG CONFIG [1] | 0 | Y | Y | R/W | 00: Charge disabled<br>01: Charge enabled<br>10: Reserved<br>11: On-the-Go (OTG) | Charge configuration bit. Set to 01 by default. |
| 4 | CHG CONFIG [0] | 1 | Y | Y | R/W | | |
| 3 | $V_{SYS\_MIN}$ [2] | 1 | Y | N | R/W | 000: 3V<br>001: 3.15<br>010: 3.3V<br>011: 3.45V<br>100: 3.525V<br>101: 3.6V<br>110: 3.675V<br>111: 3.75V | This bit sets the minimum system voltage. It has 3V to 3.75V range, and is set to 101 by default. |
| 2 | $V_{SYS\_MIN}$ [1] | 0 | Y | N | R/W | | |
| 1 | $V_{SYS\_MIN}$ [0] | 1 | Y | N | R/W | | |
| 0 | $V_{TRACK}$ [0] | 1 | Y | N | R/W | 0: 100mV<br>1: 150mV | Battery track voltage bit. Set to 1 by default. |

### REG05h: Charge Current Configuration

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | $V_{BATT\_PRE}$ | 1 | Y | Y | R/W | 0: 2.8V<br>1: 3.0V | This bit sets the pre-charge to fast charge threshold. It is set to 1 by default. |
| 6 | $I_{CC}$ [6] | 0 | Y | Y | R/W | 2560mA | This bit sets the fast charge current. It has a 320mA offset, 320mA to 4520mA range, and is set to 0100110 (1840mA) by default. |
| 5 | $I_{CC}$ [5] | 1 | Y | Y | R/W | 1280mA | |
| 4 | $I_{CC}$ [4] | 0 | Y | Y | R/W | 640mA | |
| 3 | $I_{CC}$ [3] | 0 | Y | Y | R/W | 320mA | |
| 2 | $I_{CC}$ [2] | 1 | Y | Y | R/W | 160mA | |
| 1 | $I_{CC}$ [1] | 1 | Y | Y | R/W | 80mA | |
| 0 | $I_{CC}$ [0] | 0 | Y | Y | R/W | 40mA | |

### REG06h: Pre-Charge and Termination Current

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | $I_{PRE}$ [3] | 0 | Y | Y | R/W | 320mA | This bit sets the pre-charge current. It has a 150mA offset, 150mA to 750mA range, and is set to 0010 (230mA) by default. |
| 6 | $I_{PRE}$ [2] | 0 | Y | Y | R/W | 160mA | |
| 5 | $I_{PRE}$ [1] | 1 | Y | Y | R/W | 80mA | |
| 4 | $I_{PRE}$ [0] | 0 | Y | Y | R/W | 40mA | |
| 3 | $I_{TERM}$ [3] | 0 | Y | Y | R/W | 320mA | This bit sets the termination current. It has a 120mA offset, 120mA to 720mA range, and is set to 0010 (200mA) by default. |
| 2 | $I_{TERM}$ [2] | 0 | Y | Y | R/W | 160mA | |
| 1 | $I_{TERM}$ [1] | 1 | Y | Y | R/W | 80mA | |
| 0 | $I_{TERM}$ [0] | 0 | Y | Y | R/W | 40mA | |

### REG07h: Charge Voltage Regulation

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | $V_{BATT\_REG}$ [5] | 1 | Y | Y | R/W | 640mV | This bit sets the battery regulation voltage. It has a 3.4V offset, 3.4V to 4.67V range, and is set to 1010000 (4.2V) by default. |
| 6 | $V_{BATT\_REG}$ [5] | 0 | Y | Y | R/W | 320mV | |
| 5 | $V_{BATT\_REG}$ [4] | 1 | Y | Y | R/W | 160mV | |
| 4 | $V_{BATT\_REG}$ [3] | 0 | Y | Y | R/W | 80mV | |
| 3 | $V_{BATT\_REG}$ [2] | 0 | Y | Y | R/W | 40mV | |
| 2 | $V_{BATT\_REG}$ [1] | 0 | Y | Y | R/W | 20mV | |
| 1 | $V_{BATT\_REG}$ [0] | 0 | Y | Y | R/W | 10mV | |
| 0 | $V_{RECH}$ | 0 | Y | Y | R/W | 0: 100mV<br>1: 200mV | This bit sets the battery recharge threshold (below $V_{BATT\_REG}$). Set to 0 by default. |

### REG08h: Timer Configuration

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | EN_TERM | 1 | Y | Y | R/W | 0: Disabled<br>1: Enabled | Termination enable bit. Set to 1 by default. |
| 6 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 5 | WATCHDOG [1] | 0 | Y | N | R/W | 00: Disable timer<br>01: 40s<br>10: 80s<br>11: 160s | This bit sets the I²C watchdog timer limit. Set to 01 by default. The watchdog function is not available when only a battery is present. |
| 4 | WATCHDOG [0] | 1 | Y | N | R/W | | |
| 3 | WATCHDOG TIMER RESET | 0 | Y | Y | R/W | 0: Normal<br>1: Reset | This bit is set to 0 by default, and returns to 0 after the timer resets. |
| 2 | CHG_TMR [1] | 1 | Y | Y | R/W | 00: 5hrs<br>01: 8hrs<br>10: 12hrs<br>11: 20hrs | Constant current charge timer. This bit is set to 10 by default via the OTP. |
| 1 | CHG_TMR [2] | 0 | Y | Y | R/W | | |
| 0 | EN_TIMER | 1 | Y | Y | R/W | 0: Disabled<br>1: Enabled | Safety timer enable bit. Set to 1 by default. |

### REG09h: Bandgap

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 6 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 5 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 4 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 3 | BG_EN | 0 | Y | Y | R/W | 0: Enabled<br>1: Disabled | This bit is set to 0 by default. Setting this bit from 1 to 0 will reset the input plug-in detection and safety timer. |
| 2 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 1 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 0 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |

### REG0Ah: BATFET Configuration

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | SW FREQ | 0 | Y | Y | R/W | 0: 1.35MHz<br>1: 1MHz | This bit sets the switching frequency. Set to 0 by default. |
| 6 | TMR2X_EN | 1 | Y | Y | R/W | 0: Disable 2x extended safety timer<br>1: Enable 2x extended safety timer | 2x timer enable bit. Set to 1 by default. |
| 5 | BATFET_DIS | 0 | N | N | R/W | 0: Allow BATFET to turn on<br>1: Force BATFET off | This bit is set to 0 by default. |
| 4 | SYSRST_SEL | 1 | Y | N | R/W | 0: Hardware reset<br>1: Software reset | System reset selection bit.<br>If hardware is selected, pull DISC low for time in Bit[1:0] to turn off BATFET, pull DISC low for time in Bit[3:2] to turn on BATFET.<br>If software reset is selected, the off time is set by bits[3:2].<br>Set this bit to 1 by default. |
| 3 | $t_{DISC\_H}$[1] | 1 | Y | Y | R/W | 00: 0.5s<br>01: 2s<br>10: 4s<br>11: 8s | DISC pin pull low time or BATFET off time to reset BATFET. This bit is set to 10 by default. |
| 2 | $t_{DISC\_H}$[0] | 0 | Y | Y | R/W | | |
| 1 | $t_{DISC\_L}$[1] | 0 | Y | Y | R/W | 00: 8s<br>01: 10s<br>10: 12s<br>11: 16s | DISC pin pull low lasting time to turn off BATFET. This bit is set to 00 by default. |
| 0 | $t_{DISC\_L}$[0] | 0 | Y | Y | R/W | | |

### REG0Bh: INT MASK and USB Detection

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | INT_MASK [1] | 1 | Y | Y | R/W | 0: No INT during safety timer fault<br>1: INT during safety timer fault | This bit is set to 1 by default. |
| 6 | INT_MASK [0] | 1 | Y | Y | R/W | 0: No INT during BAT_FAULT<br>1: INT in BAT_FAULT | This bit is set to 1 by default. |
| 5 | USB_DET_EN | 0 | Y | Y | R/W | 0: Not in DP/DM detection<br>1: Force DP/DM detection | USB DP/DM detection enable bit. Set to 0 by default. |
| 4 | DM | 0 | Y | N | R/W | 0: 3.3V<br>1: 0.6V | This bit is set to 0 by default, and is valid when REG0Bh, bits[2:1] = 11. It resets to 0 after 1 is written. |
| 3 | DP | 0 | Y | N | R/W | 0: 0.6V<br>1: 3.3V | This bit is set to 0 by default, and is valid when REG0Bh, bits[2:1] = 11. It resets to 0 after 1 is written. |
| 2 | USB FAST CHG [1] | 0 | Y | N | R/W | 00: DP = 0.6V, DM = Hi-Z<br>01: DP = 3.3V, DM = 0.6V<br>10: DP = 0.6V, DM = 0.6V<br>11: DP = 0.6V, DM = 3.3V | This bit sets the fast charge value. Set to 00 by default. After $V_{IN}$ POR, these bits go back to 00. |
| 1 | USB FAST CHG [0] | 0 | Y | N | R/W | | |
| 0 | USB FAST CHG_RESET | 0 | Y | N | R/W | 0: D+ recovers to $V_{DP\_SRC}$<br>1: D+ is pulled down to zero | This bit resets USB fast charge by forcing the DP pin to 0V. Set to 0 by default. This bit is valid in fast charge mode. |

### REG0Ch: STATUS

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | VIN_STAT[2] | 0 | N | N | R | D+/D- version<br>000: No input<br>001: Nonstandard adapter (1A/2.1A/2.4A)<br>010: SDP<br>011: CDP<br>100: DCP<br>101: Fast-charge adapter<br>111: OTG | This bit selects the input source. Set to 000 by default. $V_{IN}$ POR resets VIN_STAT. |
| 6 | VIN_STAT[1] | 0 | N | N | R | | |
| 5 | VIN_STAT[0] | 0 | N | N | R | | |
| 4 | CHG_STAT [1] | 0 | N | N | R | 00: Not charging<br>01: Trickle charge<br>10: Constant current charge<br>11: Charge done | This bit is set to 00 by default. |
| 3 | CHG_STAT [0] | 0 | N | N | R | | |
| 2 | NTC FLOAT_ STAT | 0 | N | N | R | 0: No NTC float<br>1: NTC float | This bit is set to 0 by default. |
| 1 | THERM_STAT | 0 | N | N | R | 0: Normal<br>1: Thermal regulation | This bit is set to 0 by default. |
| 0 | VSYS_STAT | 1 | N | N | R | 0: In $V_{SYSMIN}$ regulation (BAT < $V_{SYSMIN}$)<br>1: Not in $V_{SYSMIN}$ regulation (BAT > $V_{SYSMIN}$) | This bit is set to 1 by default. |

### REG0Dh: FAULT

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | WATCHDOG_ FAULT | 0 | N | N | R | 0: Normal<br>1: Watchdog timer expiration | This bit is set to 0 by default. |
| 6 | OTG_FAULT | 0 | N | N | R | 0: Normal<br>1: $V_{IN}$ overload, or $V_{IN}$ over-voltage protection (OVP), or the battery has an under-voltage condition | This bit is set to 0 by default. |
| 5 | INPUT_FAULT | 0 | N | N | R | 0: Normal<br>1: Input over-voltage protection (OVP) or no input | This bit is set to 0 by default. |
| 4 | THERMAL SHUTDOWN | 0 | N | N | R | 0: Normal<br>1: Thermal shutdown | This bit is set to 0 by default. |
| 3 | BAT_FAULT | 0 | N | N | R | 0: Normal<br>1: Battery over-voltage protection (OVP) | This bit is set to 0 by default. |
| 2 | NTC_FAULT [2] | 0 | N | N | R | Buck mode<br>000: Normal<br>010: NTC warm<br>011: NTC cool<br>101: NTC cold<br>110: NTC hot<br>Boost mode<br>000: Normal<br>101: NTC cold<br>110: NTC hot | This bit is set to 000 by default. |
| 1 | NTC_FAULT [1] | 0 | N | N | R | | |
| 0 | NTC_FAULT [0] | 0 | N | N | R | | |

### REG0Eh: ADC of Battery Voltage

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | VBATT[7] | 0 | N | N | R | 2560mV | This bit sets the ADC conversion of the battery cell voltage. It has a 0V offset and a 0V to 5.1V range. |
| 6 | VBATT[6] | 0 | N | N | R | 1280mV | |
| 5 | VBATT[5] | 0 | N | N | R | 640mV | |
| 4 | VBATT[4] | 0 | N | N | R | 320mV | |
| 3 | VBATT[3] | 0 | N | N | R | 160mV | |
| 2 | VBATT[2] | 0 | N | N | R | 80mV | |
| 1 | VBATT[1] | 0 | N | N | R | 40mV | |
| 0 | VBATT[0] | 0 | N | N | R | 20mV | |

### REG0Fh: ADC of System Voltage

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | VSYS[7] | 0 | N | N | R | 2560mV | This bit sets the ADC conversion of the system voltage. It has a 0V offset and 0V to 5.1V range. |
| 6 | VSYS[6] | 0 | N | N | R | 1280mV | |
| 5 | VSYS[5] | 0 | N | N | R | 640mV | |
| 4 | VSYS[4] | 0 | N | N | R | 320mV | |
| 3 | VSYS[3] | 0 | N | N | R | 160mV | |
| 2 | VSYS[2] | 0 | N | N | R | 80mV | |
| 1 | VSYS[1] | 0 | N | N | R | 40mV | |
| 0 | VSYS[0] | 0 | N | N | R | 20mV | |

### REG10h: ADC of NTC Voltage

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | NTC[7] | 0 | N | N | R | 50.176% | This bit sets the ADC conversion of the NTC voltage. It has a 0% offset and 0% to 100% range. |
| 6 | NTC[6] | 0 | N | N | R | 25.088% | |
| 5 | NTC[5] | 0 | N | N | R | 12.544% | |
| 4 | NTC[4] | 0 | N | N | R | 6.272% | |
| 3 | NTC[3] | 0 | N | N | R | 3.136% | |
| 2 | NTC[2] | 0 | N | N | R | 1.568% | |
| 1 | NTC[1] | 0 | N | N | R | 0.784% | |
| 0 | NTC[0] | 0 | N | N | R | 0.392% | |

### REG11h: ADC of Input Voltage

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | VIN[7] | 0 | N | N | R | 7680mV | The bit sets the ADC conversion of the input voltage. It has a 0V offset and a 3.6V to 15.3V range. |
| 6 | VIN[6] | 0 | N | N | R | 3840mV | |
| 5 | VIN[5] | 0 | N | N | R | 1920mV | |
| 4 | VIN[4] | 0 | N | N | R | 960mV | |
| 3 | VIN[3] | 0 | N | N | R | 480mV | |
| 2 | VIN[2] | 0 | N | N | R | 240mV | |
| 1 | VIN[1] | 0 | N | N | R | 120mV | |
| 0 | VIN[0] | 0 | N | N | R | 60mV | |

### REG12h: ADC of Charge Current

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | $I_{CHG}$[7] | 0 | N | N | R | 2240mA | The bit sets the ADC conversion of the charge current. It has a 0A offset and a 0A to 5.66A range. |
| 6 | $I_{CHG}$[6] | 0 | N | N | R | 1120mA | |
| 5 | $I_{CHG}$[5] | 0 | N | N | R | 560mA | |
| 4 | $I_{CHG}$[4] | 0 | N | N | R | 280mA | |
| 3 | $I_{CHG}$[3] | 0 | N | N | R | 140mA | |
| 2 | $I_{CHG}$[2] | 0 | N | N | R | 70mA | |
| 1 | $I_{CHG}$[1] | 0 | N | N | R | 35mA | |
| 0 | $I_{CHG}$[0] | 0 | N | N | R | 17.5mA | |

### REG13h: ADC of Input Current

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | $I_{IN}$[7] | 0 | N | N | R | 1702.4mA | This bit sets the ADC conversion of the input current. It has a 0A offset and a 0A to 3.39A range. |
| 6 | $I_{IN}$[6] | 0 | N | N | R | 851.2mA | |
| 5 | $I_{IN}$[5] | 0 | N | N | R | 425.6mA | |
| 4 | $I_{IN}$[4] | 0 | N | N | R | 212.8mA | |
| 3 | $I_{IN}$[3] | 0 | N | N | R | 106.4mA | |
| 2 | $I_{IN}$[2] | 0 | N | N | R | 53.2mA | |
| 1 | $I_{IN}$[1] | 0 | N | N | R | 26.6mA | |
| 0 | $I_{IN}$[0] | 0 | N | N | R | 13.3mA | |

### REG14h: Power Management Status

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | VINPPM_STAT | 0 | N | N | R | 0: No PPM<br>1: VINPPM | This bit is set to 0 by default. |
| 6 | IINPPM_STAT | 0 | N | N | R | 0: No PPM<br>1: IINPPM | This bit is set to 0 by default. |
| 5 | $I_{IN\_DPM}$[5] | 0 | N | N | R | 1600mA | The bit has a 100mA offset, a 100mA to 3.25A range, and is 001000 by default. |
| 4 | $I_{IN\_DPM}$[4] | 0 | N | N | R | 800mA | |
| 3 | $I_{IN\_DPM}$[3] | 1 | N | N | R | 400mA | |
| 2 | $I_{IN\_DPM}$[2] | 0 | N | N | R | 200mA | |
| 1 | $I_{IN\_DPM}$[1] | 0 | N | N | R | 100mA | |
| 0 | $I_{IN\_DPM}$[0] | 0 | N | N | R | 50mA | |

### REG15h: DPM Mask

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | AICO_STAT | 0 | N | N | R | 0: No operation<br>1: AICO action | This bit is set to 0 by default. |
| 6 | VINPPM_INT_MASK[1] | 1 | Y | Y | R/W | 0: No INT during VINPPM<br>1: INT during VINPPM | This bit is set to 1 by default. |
| 5 | IINPPM_INT_MASK[1] | 1 | Y | Y | R/W | 0: No INT during IINPPM<br>1: INT during IINPPM | This bit is set to 1 by default. |
| 4 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 3 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 2 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 1 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 0 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |

### REG16h: JEITA Configuration

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | JEITA_VSET | 1 | Y | Y | R/W | 0: $V_{BATT\_REG}$ minus 100mV<br>1: $V_{BATT\_REG}$ minus 200mV | This bit is set to 1 by default. |
| 6 | JEITA_ISET | 1 | Y | Y | R/W | 0: 50% of $I_{CHG}$<br>1: 16.7% of $I_{CHG}$ | This bit is set to 1 by default. |
| 5 | $V_{TH\_HOT}$ | 1 | Y | Y | R/W | 0: 34.0% (60°C)<br>1: 36.0% (55°C) | This bit sets the hot threshold. Set to 1 by default. The thermistor is 103AT. |
| 4 | $V_{TH\_WARM}$[1] | 0 | Y | Y | R/W | 00: 43.0% (40°C)<br>01: 40.0% (45°C)<br>10: 38.0% (50°C)<br>11: 36.0% (55°C) | This bit sets the warm threshold. Set to 01 by default. The thermistor is 103AT. |
| 3 | $V_{TH\_WARM}$[0] | 1 | Y | Y | R/W | | |
| 2 | $V_{TH\_COOL}$[1] | 1 | Y | Y | R/W | 00: 72.0% (0°C)<br>01: 68.0% (5°C)<br>10: 64.0% (10°C)<br>11: 60.0% (15°C) | This bit sets the cool threshold. Set to 11 by default. The thermistor is 103AT. |
| 1 | $V_{TH\_COOL}$[0] | 1 | Y | Y | R/W | | |
| 0 | $V_{TH\_COLD}$ | 0 | Y | Y | R/W | 0: 72.0% (0°C)<br>1: 68% (5°C) | This bit sets the cold threshold. Set to 0 by default. The thermistor is 103AT. |

### REG17h: Safety Timer Status and Part Number

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | SAFETY TIMER | 0 | N | N | R | 0: Normal<br>1: Safety timer expiration | This bit is set to 0 by default. |
| 6 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 5 | PN[2] | 0 | N | N | R | 000: MP2731 | This bit is set to 000 by default. |
| 4 | PN[1] | 0 | N | N | R | | |
| 3 | PN[0] | 0 | N | N | R | | |
| 2 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 1 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 0 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |

### REG18h (7)

| Bit | Name | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment |
|---|---|---|---|---|---|---|---|
| 7 | IINLIM/VINMIN RESET_EN | 0 | N | N | N | 0: IIN_LIM and VIN_MIN do not reset when VIN POR<br>1: IIN_LIM and VIN_MIN reset when VIN POR | This bit is set to 0 by default. |
| 6 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 5 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 4 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |
| 3 | VINOVP_CS | 0 | N/A | N/A | N/A | 0: 16.8V<br>1: As per USB FAST CHG[1:0] setting | This bit is set to 0 by default. |
| 2 | ADDRESS | 0 | N/A | N/A | N/A | 0: 4BH<br>1: 21H | This bit is set to 0 by default. |
| 1 | PFM_EN | 0 | N/A | N/A | N/A | 0: Enable<br>1: Disable | This bit is used to enable or disable PFM when charging is disabled. Set to 0 by default. |
| 0 | RESERVED | N/A | N/A | N/A | N/A | Reserved. | |

**Note:**

7) This register is for the one-time programmable (OTP) memory. It is not accessible.

## OTP MAP

| # | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| 00 | N/A | | $I_{IN\_LIM}$: 100mA to 3250mA/50mA step | | | | | |
| 01 | N/A | $V_{IN\_MIN}$: 3.7V to 15.2V/100mV step | | | | | | |
| 05 | N/A | $I_{CC}$: 320mA to 4520mA/40mA step | | | | | | |
| 07 | $V_{BATT\_REG}$: 3.4V to 4.67V/10mV step | | | | | | | N/A |
| 08 | N/A | | | | | CHG_TMR | | N/A |
| 18 | IINLIM/VINMIN RESET_EN | N/A | N/A | N/A | VINOVP_CS | ADDRESS | PFM_EN | N/A |

## OTP DEFAULT

| OTP Items | Default |
|---|---|
| $I_{IN\_LIM}$ | 500mA |
| $V_{IN\_MIN}$ | 4.3V |
| $I_{CC}$ | 1.84A |
| $V_{BATT\_REG}$ | 4.2V |
| CHG_TMR | 12hrs |
| INLIM/VINMIN RESET_EN | IIN_LIM and VIN_MIN not reset when VIN POR |
| VINOVP_CS | 16.8V |
| ADDRESS | 4BH |
| PFM_EN | Enable |

# APPLICATION INFORMATION

### Setting the Input Current Limit

The input current limit is set according to the input power source. The input current limit can be set through the I²C using the MP2731's GUI. If a user wants to set a current limit that cannot be set by the I²C, it can be set using the ILIM pin. Connect a resistor from the ILIM pin to AGND to program the input current limit. The MP2731 selects the lower limit between the I²C setting and the resistor setting. The ILIM pin resistor can be determined with Equation (1) on page 22.

See Table 1 on page 22 to determine how to set the input current limit for USB inputs.

### Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A smaller-value inductor is physically small, but results in higher ripple current, magnetic hysteretic loss, and output capacitance. A larger-value inductance provides lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss.

For the best results, the inductor ripple current should not exceed 30% of the maximum load current under the worst-case conditions. For the MP2731 to operate with a typical 5V input voltage, the maximum inductor current ripple occurs at the corner point between pre-charge and constant current charge. The inductance (L) can be estimated with Equation (2):

$$L=\frac{V_{IN}-V_{SYS}}{\Delta I_{L\_MAX}}\frac{V_{SYS}}{V_{IN}\times f_{SW}(MHz)}(\mu H) \quad (2)$$

Where $V_{IN}$ is the input voltage, $V_{SYS}$ is the system voltage, $f_{SW}$ is the switching frequency, and $\Delta I_{L\_MAX}$ is the maximum inductor ripple current, which is usually 30% of the CC charge current.

$I_{PEAK}$ can be calculated with Equation (3):

$$I_{PEAK}=I_{LOAD(MAX)}\times\left(1+\frac{\%ripple}{2}\right)(A) \quad (3)$$

The maximum charge current can be set to 4.5A, but the real charge current cannot reach this value due to the input current limit. To cover most typical applications, and to give enough margin to avoid reaching the peak current limit of the high-side switch, the maximum inductor current ripple is set to 0.5A with $5V_{IN}$, and the inductance is 1.5µH. Select 1.0µH for low-profile operation. To optimize efficiency, choose an inductor with a low DC resistance.

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors are sufficient. Choose ceramic capacitors with X5R or X7R dielectrics.

Since the input capacitor ($C_{IN}$) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{CIN}=I_{LOAD}\times\sqrt{\frac{V_{SYS}}{V_{IN}}\times\left(1-\frac{V_{SYS}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs when $V_{IN}$ = $2V_{SYS}$, and $I_{CIN}$ = $I_{SYS}$ / 2. For simplification, choose the input capacitor with an RMS current rating that exceeds half of the maximum load current.

For the MP2731, the RMS current in the input capacitor is from PMID to GND. This means a small, high-quality ceramic capacitor (e.g. 10µF) should be placed from VPMID to PGND, as close to the IC as possible. The remaining capacitor should be placed from VIN to GND.

When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge that prevents excessive voltage ripple at the input.

### Selecting the Output Capacitor

In the typical application circuit, the output capacitor ($C_{SYS}$) is in parallel with the SYS load. $C_{SYS}$ absorbs the high-frequency switching ripple current and smooths the output voltage. Its impedance must be below that of the system load to ensure that it properly absorbs the ripple current.

It is recommended to use a ceramic capacitor because its lower ESR and smaller size allow the ESR of the output capacitor to be ignored.

The output voltage ripple can be calculated with Equation (5):

$$\Delta R = \frac{\Delta V_{SYS}}{V_{SYS}} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times C_{SYS} \times f_{SW}^{2} \times L}\% \quad (5)$$

To guarantee the ±0.5% system voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g. 0.1%). The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage.

The output capacitor can be calculated with Equation (6):

$$C_{SYS} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times f_{SW}^{2} \times L \times \Delta R} \quad (6)$$

For example, if $V_{IN}$ = 5V, $V_{SYS}$ = 3.7V, L = 1µH, $f_{SW}$ = 1.35MHz, and ΔR = 0.1%, choose a 22µF ceramic capacitor.

### Selecting the NTC Resistor

Figure 6 on page 23 shows an external resistor divider reference circuit to limit the low-temperature threshold ($V_{COLD}$) and high-temperature threshold ($V_{HOT}$). For a given NTC thermistor, select the appropriate $R_{T2}$ and $R_{T1}$ values to set the NTC window, calculated with Equation (7) and Equation (8), respectively:

$$R_{T2} = \frac{R_{NTC\_HOT} \times V_{COLD} \times (1\text{-}V_{HOT}) - R_{NTC\_COLD} \times V_{HOT} \times (1 - V_{COLD})}{V_{HOT} - V_{COLD}} \quad (7)$$

$$R_{T1} = \frac{(1\text{-}V_{COLD}) \times (R_{NTC\_COLD} + R_{T2})}{V_{COLD}} \quad (8)$$

$R_{NTC\_HOT}$ is the value of the NTC resistor at the high temperature of the required temperature operation range, and $R_{NTC\_COLD}$ is the value of the NTC resistor at the low temperature.

$R_{T1}$ and $R_{T2}$ allow the high-temperature limit and low-temperature limit to be configured independently. With this feature, the MP2731 can operate within most NTC resistor and temperature operation range requirements.

The $R_{T1}$ and $R_{T2}$ values depend on the type of the NTC resistor. For example, a 103AT thermistor must have the following electrical characteristics:

- At 0°C, $R_{NTC\_COLD}$ = 27.28kΩ
- At 60°C, $R_{NTC\_HOT}$ = 3.02kΩ

$V_{HOT}$ is selected at 34% and $V_{COLD}$ is selected at 72% via the REG16h register. Using Equation (7) and Equation (8), $R_{T1}$ = 11.8kΩ and $R_{T2}$ = 3.06kΩ.

### PCB Layout Guidelines

Careful PCB layout is critical to meet specified noise rejection requirements and high efficiency. For the best results, follow the guidelines below:

1. Route the power stages adjacent to their grounds. Minimize the high-side switching node (SW and inductor), the trace lengths in the high-current paths, and the current-sense resistor trace.
2. Keep the switching node short and route it away from all small control signals, especially the feedback network.
3. Place the input capacitor as close as possible to the PMID and PGND pins.
4. Place the output inductor close to the IC, and connect the output capacitor between the inductor and PGND of the IC.
5. For high-current applications, the pins for the power pads (IN, SW, SYS, BATT, and PGND) should be connected to as much copper on the board as possible. This improves thermal performance by conducting heat away from the IC.
6. Connect a ground plane directly to the return of all components through via holes. It is also recommended to put via holes inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With a small layout and a single ground plane, there is no ground-bounce issue, and having the components separated minimizes coupling between signals and stability requirements.
7. Pull the connection wire from the MCU (I²C) far from the SW mode and copper regions. SCL and SDA should be placed in close parallel.

## TYPICAL APPLICATION CIRCUIT

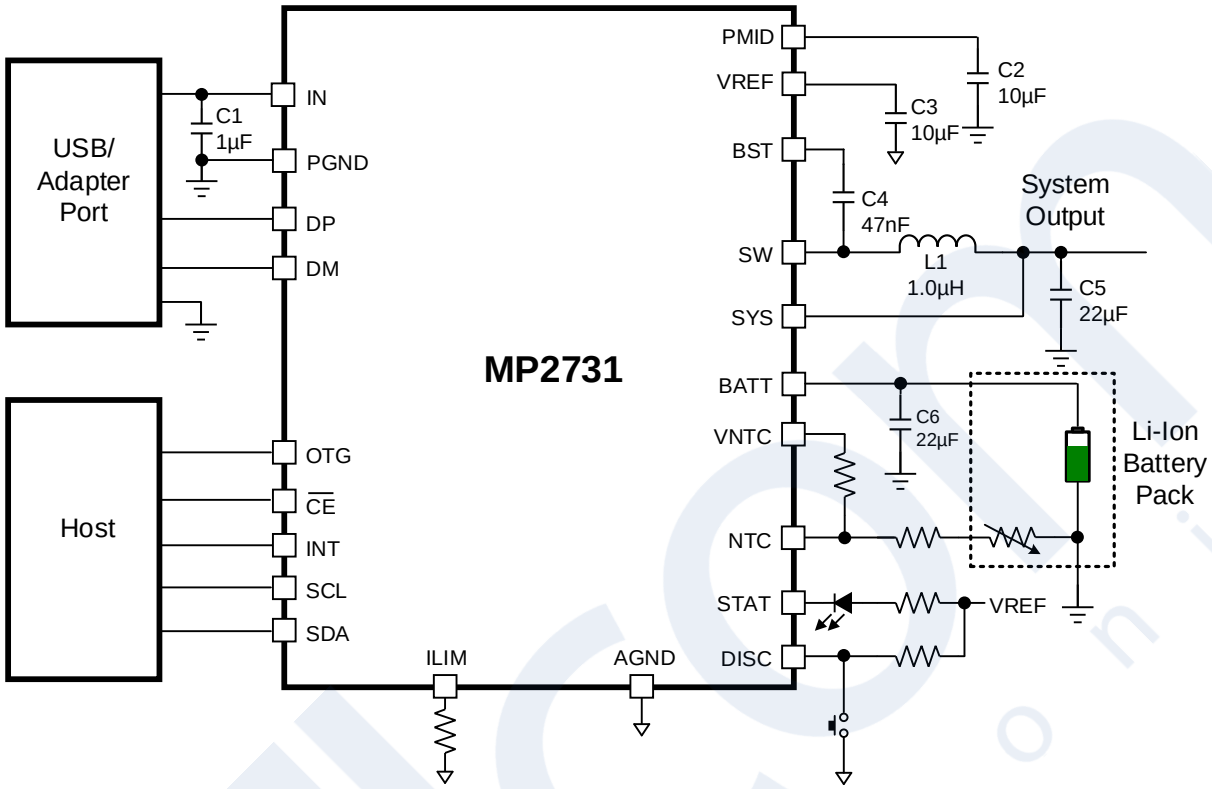


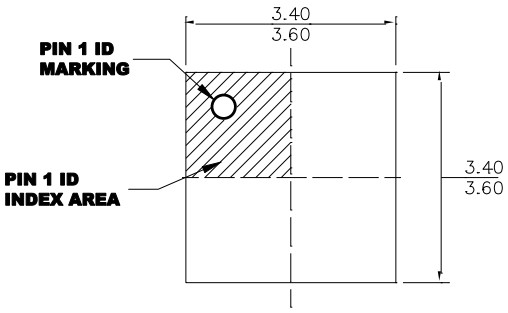

**Figure 18: Typical Application Circuit**

**Table 3: Key BOM of Figure 18**

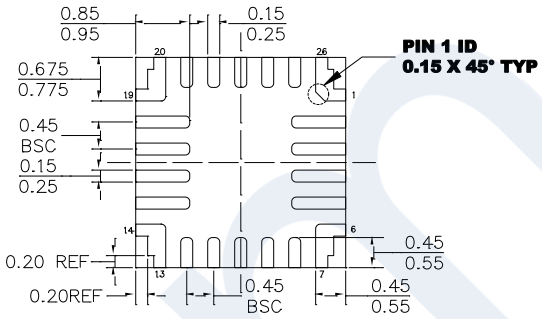
| Qty | Ref | Value | Description | Package | Manufacturer |
|---|---|---|---|---|---|
| 1 | C1 | 1µF | Ceramic capacitor, 50V, X5R or X7R | 0603 | Any |
| 1 | C2 | 10µF | Ceramic capacitor, 50V, X5R or X7R | 0603 | Any |
| 1 | C3 | 10µF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |
| 1 | C4 | 47nF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |
| 1 | C5 | 22µF | Ceramic capacitor, 16V, X5R or X7R | 0805 | Any |
| 1 | C6 | 22µF | Ceramic capacitor, 16V, X5R or X7R | 0805 | Any |
| 1 | L1 | 1.0µH | >9.6A | N/A | Any |

# PACKAGE INFORMATION

## QFN-26 (3.5mmx3.5mm)

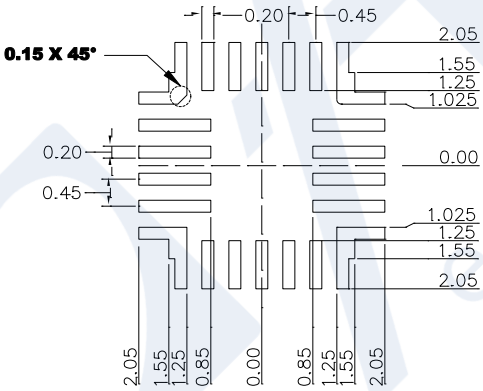



**TOP VIEW**




**BOTTOM VIEW**


**SIDE VIEW**

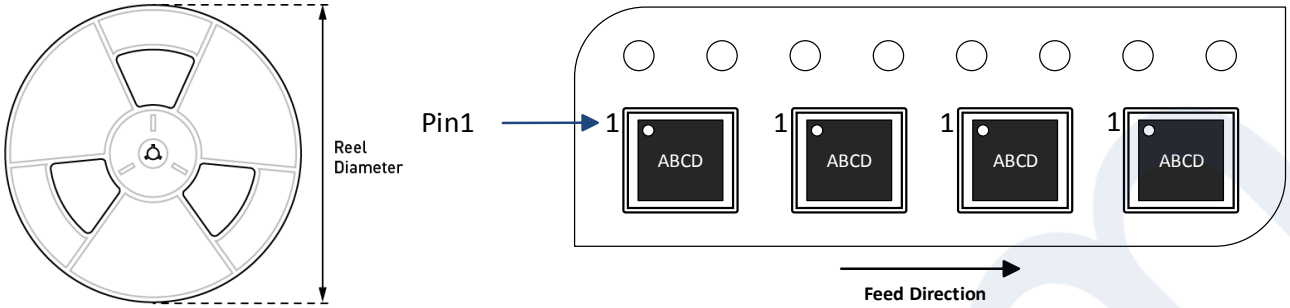



**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch | Trailer Leader/ Reel |
|---|---|---|---|---|---|---|---|---|
| MP2731GQC-xxxx-Z | QFN-26 (3.5mmx3.5mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm | 125&125 |

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 5/29/2020 | Initial Release | - |
| 1.1 | 08/24/2020 | Update safety timer expiration reset actions | Page 24 |
| | | Add function description for BG_EN bit | Page 34 |
| | | Update ADC description | Page 1, Page 26 |
| 1.2 | 09/22/2021 | Update the factory default code to 0001 | Page 3 |
| | 09/22/2021 | Update the feature description | Page 1 |
| | | Update the description (3A to 4.5A) | Page 21 |
| | | Update the I²C description | Page 27, 28, and 29 |