MP2710

500mA 1-Cell Li-ion Battery Charger with PPM 1mA Termination and <1uA Battery Leakage

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP2710 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power path management for space-limited portable applications. The MP2710 takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The charger function features pre-charge (PRE.C), fast current (CC) and constant voltage (CV) regulation, charge termination, and auto-recharge.

The power path management function ensures continuous power to the system by automatically selecting the input, battery, or both to power the system. This function features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2710 provides a system short-circuit protection (SCP) function by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged due to an excessively high current. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below a programmable battery UVLO threshold. This prevents the Li-ion battery from being over-discharged. An integrated I²C control interface allows the MP2710 to program the charging parameters, such as input current limit, input minimum voltage regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2710 is available in a 9-pin WLCSP (1.85mmx1.85mm) package.

FEATURES

- 4.35V to 5.5V Operating Input Voltage
- Up to 21V Input Sustainable Voltage
- Programmable Charging Current from 8mA to 456mA in 2mA step
- 1mA Termination Current
- ±0.5% Charge Voltage Accuracy
- 700µA Input Quiescent Current
- Low Power Mode to Reduce Battery Consumption
- Programmable JEITA for Battery Temperature Protection
- No NTC Divided Resistor Needed to Save Battery Current
- Dedicated pin to Control Shipping Mode and System Reset
- Enter Shipping Mode via I²C or Analog Pin
- Exit Shipping Mode by VIN Plug In or Analog Pin
- <350nA Battery Leakage Current in Shipping Mode
- I²C Interface for Setting Charging Parameters and Status Reporting
- Built-In Robust Charging Protection
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Watchdog Monitoring I²C Operation
- Available in a WLCSP-9 (1.85mmx1.85mm) Package

APPLICATIONS

- TWS Earbud
- Fitness Accessories
- IOT
- Smart Watches

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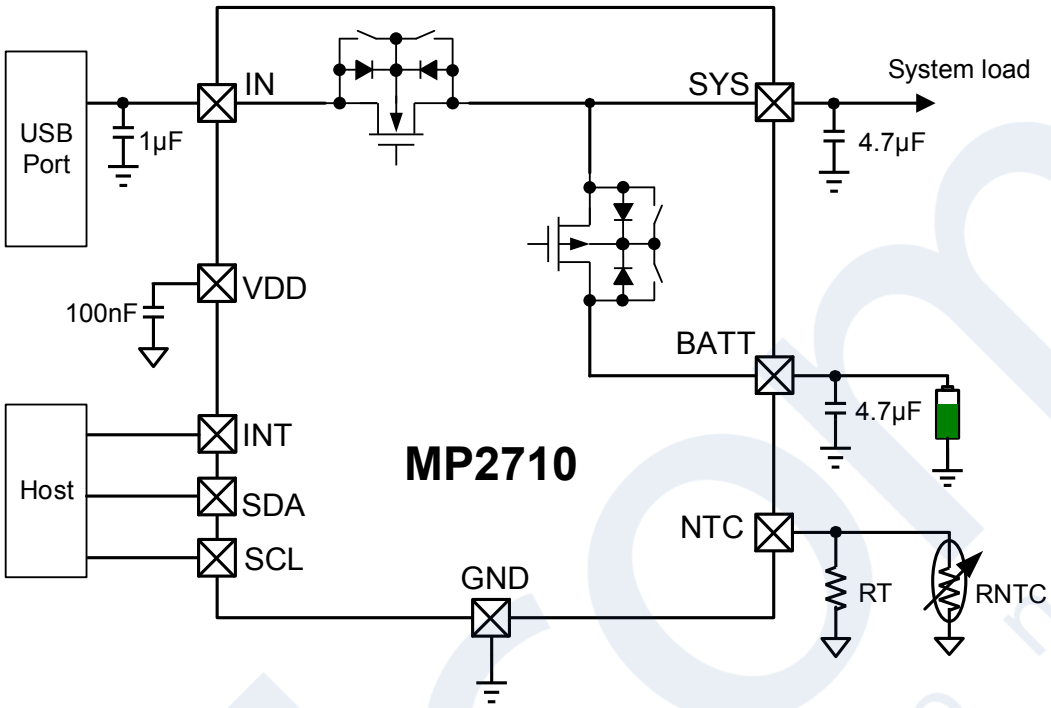
TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2710GC-xxxx	WLCSP (1.85mmx1.85mm)	*See Below*	1
EVKT-MP2710	Evaluation kit	-	

* For Tape & Reel, add suffix –Z (e.g. MP2710GC-xxxx-Z).
**"xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Please contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

MAY
LLL

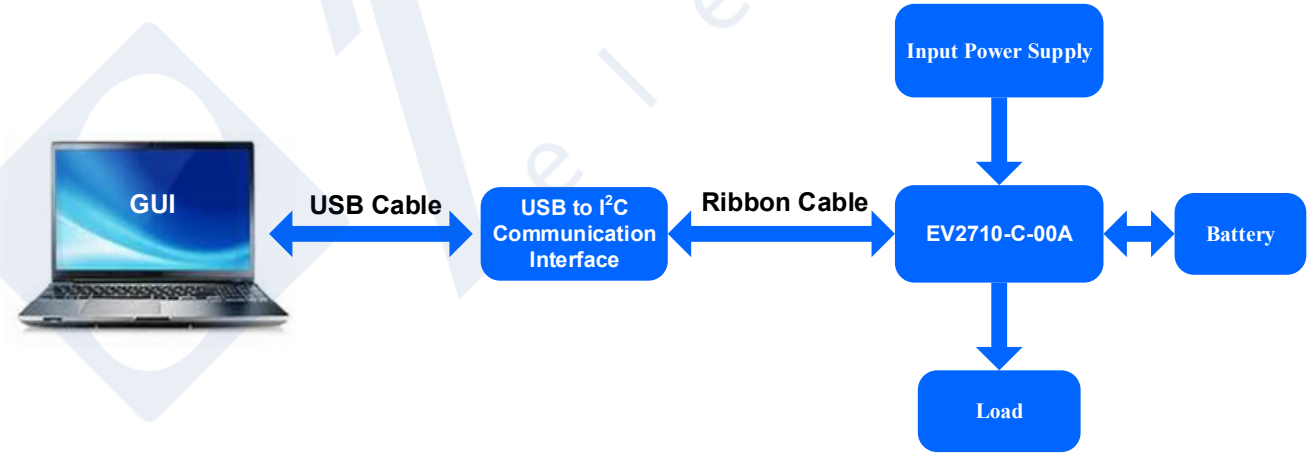
MA: Product code of MP2710GC
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP2710

EVKT-MP2710 kit contents: (Items below can be ordered separately)

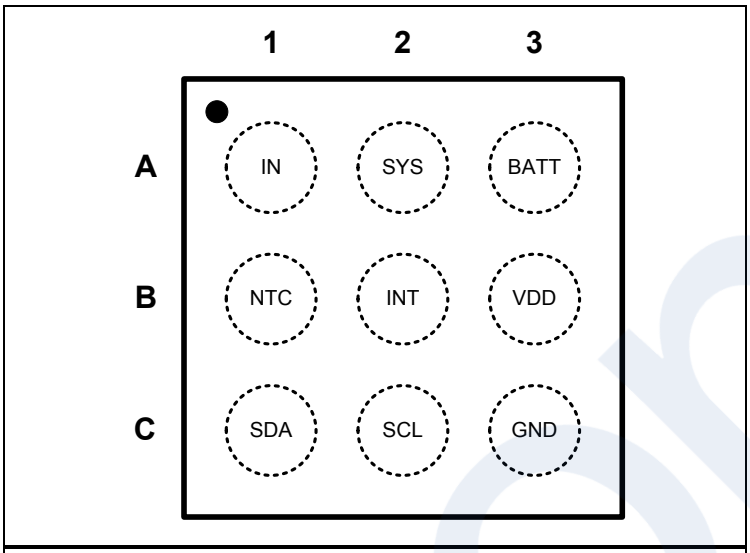
#	Part Number	Item	Quantity
1	EV2710-C-00A	MP2710 evaluation board	1
2	EVKT-USBI2C-02-bag	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order direct from MonolithicPower.com or our distributors.



EVKT-MP2710 Evaluation Kit Set-Up

PACKAGE REFERENCE



WLCSP (1.85mmx1.85mm)

PIN FUNCTIONS

Package Pin #	Name	Description
A1	IN	**Input power pin.** Place a ceramic capacitor from IN to GND as close to the IC as possible.
A2	SYS	**System power supply.** Place a ceramic capacitor from SYS to GND as close to the IC as possible.
A3	BATT	**Battery pin.** Place a ceramic capacitor from BATT to GND as close to the IC as possible.
B1	NTC	**Temperature sense input.** Connect a negative temperature coefficient thermistor to NTC. Put a resistor 91kohm in parallel with thermistor to make sure NTC voltage in operation range if NTC function is used, otherwise, remove this resistor.
B2	INT	**Interrupt output.** INT can send a charging status and fault interrupt signal to the host. INT is also used to disconnect the system from the battery.
B3	VDD	**Internal control power supply pin.** Connect a 100nF ceramic capacitor from VDD to GND. No external load is allowed.
C1	SDA	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
C2	SCL	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
C3	GND	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

IN ..... -0.3V to 21V
SYS ..... -0.3V to 5.3V (5.5V for 500µs)
All other pins ..... -0.3V to 6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = 25°C) (2) 0.88W
Storage temperature ..... -65°C to +150°C

ESD Rating

Human-body model (HBM) 2000V
Charged-device model (CDM) 750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.35V to 5.5V
I_{IN} ..... up to 500mA
I_{DISCHG} ..... up to 3.2A
I_{CHG} ..... up to 456mA
V_{BATT} ..... up to 4.545V
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

WLCSP (1.85mmx1.85mm)	114	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT}=3.8V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input Under-voltage Lock-out Threshold	V_{IN_UVLO}	Input falling	3.15	3.25	3.35	V
Input Under-voltage Lock-out Threshold Hysteresis		Input rising		150		mV
Input Over-voltage Protection Threshold	V_{IN_OVLO}	Input rising threshold	5.85	6	6.15	V
Input Over-voltage Protection Threshold Hysteresis				350		mV
Input vs. Battery Voltage Headroom Threshold	V_{HDRM}	Input rising vs. battery	80	130	170	mV
Input vs. Battery Voltage Headroom Threshold Hysteresis				90		mV
BATT Input Voltage(5)	V_{BATT}				4.5	V
Battery Under-voltage Lockout Threshold	V_{BATT_UVLO}	BATT voltage falling, REG01H[2:0]=000	2.28	2.4	2.48	V
		BATT voltage falling, REG01H[2:0]=100	2.66	2.76	2.86	
		BATT voltage falling, REG01H[2:0]=111	2.93	3.03	3.13	
BATT Under Voltage Threshold Hysteresis		V_{BATT_UVLO}=2.76V		190		mV
Battery Over-voltage Protection Threshold	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		130		mV
Battery Over-voltage Protection Hysteresis				60		
Power Path Management						
Regulated System Output Voltage Accuracy	$V_{SYS\_REG\_ACC}$	V_{IN} =5.5V, R_{SYS}=100Ω, I_{CHG}=0A, REG07H[3:0]=0000, V_{SYS_REG}=4.2V	4.1	4.2	4.3	V
		V_{IN} =5.5V, R_{SYS}=100Ω, I_{CHG}=0A, REG07H[3:0]=1001, V_{SYS_REG}=4.65V	4.55	4.65	4.75	
		V_{IN} =5.5V, R_{SYS}=100Ω, I_{CHG}=0A, REG07H[3:0]=1111, V_{SYS_REG}=4.95V	4.85	4.95	5.05	
Input Current Limit	I_{IN_LIM}	REG00H[3:0]=0000,I_{IN_LMT}=50mA	30	40	50	mA
		REG00H[3:0]=0011,I_{IN_LMT}=140mA	112	126	140	
		REG00H[3:0]=1001,I_{IN_LMT}=320mA	275	300	320	
		REG00H[3:0]=1111,I_{IN_LMT}=500mA	440	470	500	
Input Minimum Voltage Regulation	V_{IN_MIN}	REG00H[7:4]=0000, V_{IN_REG} =3.88V	3.68	3.88	4.18	V
		REG00H[7:4]=0110, V_{IN_REG} =4.36V	4.10	4.36	4.62	
		REG00H[7:4]=1001, V_{IN_REG} =4.20V	4.40	4.60	4.75	
		REG00H[7:4]=1111, V_{IN_REG} =5.08V	4.88	5.08	5.35	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT}=3.8V, T_A = +25°C, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN to SYS Switch On Resistance	R_{ON_Q1}	V_{IN}=5V, I_{SYS}=100mA		290		mΩ
Input Quiescent Current	I_{IN_Q}	V_{IN} = 5V, EN_HIZ = 0, CE = L, charge enable, I_{CHG} = 0A, I_{SYS} = 0A		700	780	μA
		V_{IN} = 5V, EN_HIZ = 0, CE = H, charge disabled		450	520	
		V_{IN} = 5V, EN_HIZ = 1		150	200	
Battery Quiescent Current	I_{BATT_Q}	V_{IN} = 5V, CE = L, I_{SYS} = 0A, charge done, V_{BATT} = 4.35V		15	20	μA
		V_{IN} = GND, CE = H, I_{SYS} = 0A, V_{BATT} = 4.35V, low power mode 1. NTC is disabled, 2. BATTOCP is disabled 3. INT interrupt is disabled 4. watchdog is disabled		1.5	3	
		V_{IN} = GND, CE = H, I_{SYS} = 0A, V_{BATT} = 4.35V, active mode, NTC is disabled, watchdog is disabled		7.2	8	
		V_{IN} = GND, CE = H, I_{SYS} = 0A, V_{BATT} = 4.35V, active mode, NTC is disabled, watchdog is enabled		15		
		V_{BATT}=4.5V, V_{IN}=V_{SYS}=GND, in shipping mode			350	nA
B-FET on resistance	R_{ON_Q2}	V_{IN} < 2V, V_{BATT} = 3.5V, I_{SYS} = 100mA		100		mΩ
B-FET discharge current limit	I_{DSCHG}	REG03H[7:4] = 0001, I_{DSCHG} = 400mA	370	490	585	mA
		REG03H[7:4] = 1001, I_{DSCHG} = 2000mA		2400(5)		
SYS reverse to BATT switch leakage		V_{SYS} = 4.65V, V_{IN} = 5V, V_{BATT} = GND, EN_HIZ = 1, CE = H, charge disabled			100	nA
Ideal diode forward voltage in supplement mode	V_{FWD}	50mA discharge current		30		mV
Shipping Mode						
Enter shipping mode deglitch time	t_{ESM_DGL}	REG06H[5] is set from 0 to 1, REG0AH[5:4]=00		1		s
Exit shipping mode deglitch time	t_{EXSM_DGL}	Exit shipping mode by VIN plug in, REG0AH[2]=0		80		ms
		Exit shipping mode by pulling INT low		2		s
Auto-Reset Mode						
Reset deglitch by INT	t_{RST_DGL}	REG01H[7:6] = 00		8		s
		REG01H[7:6] = 10		16		
B-FET off duration	t_{RST_DUR}	REG01H[5] = 0		2		s
		REG01H[5] = 1		4		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT}=3.8V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery Charger						
Battery Charge Voltage Regulation	V_{BATT_REG}	REG04H[7:2] = 000000, V_{BATT_REG} = 3.6V, T_A=0°C-85°C	3.578	3.6	3.622	V
		REG04H[7:2] = 101000, V_{BATT_REG} = 4.2V	4.179	4.2	4.221	
		REG04H[7:2] = 101000, V_{BATT_REG} = 4.2V, T_A=0°C-85°C	4.175	4.2	4.225	
		REG04H[7:2] = 110010, V_{BATT_REG} = 4.38V, T_A=0°C-85°C	4.354	4.38	4.404	
		REG04H[7:2] = 111110, V_{BATT_REG} = 4.53V, T_A=0°C-85°C	4.506	4.53	4.556	
Fast Charge Current	I_{CC}	REG02H[7:0] = 00000000, I_{CC}=8mA	7.6	8	8.6	mA
		REG02H[7:0] = 00011100， I_{CC}=58mA	53	58	63	
		REG02H[7:0] = 00110000, I_{CC} = 98mA	91	98	105	
		REG02H[7:0] =10000011, I_{CC} = 264mA	246	264	280	
		REG02H[7:0] = 11100011, I_{CC} = 456mA	420	456	484	
Pre-charge Current	I_{PRE}	I_{PRE} = I_{TERM}	1		31	mA
Charge Termination Current Threshold	I_{TERM}	REG03H[3:0]=0000, I_{TERM}=1mA	0.82	1.08	1.37	mA
		REG03H[3:0]=0001, I_{TERM}=3mA	2.55	3	3.45	
		REG03H[3:0]=0101, I_{TERM}=11mA	9.8	11	12.2	
		REG03H[3:0]=0101, I_{TERM}=31mA	28	31	34	
Termination deglitch time	t_{TERM_DGL}			3.2		s
Pre-charge to Fast Charge Threshold	V_{BATT_PRE}	V_{BATT} Rising, REG04H[1]=1, V_{BATT_PRE}=3.0V	2.9	3.0	3.1	V
Pre-charge to Fast Charge Threshold Hysteresis				90		mV
Battery Auto-recharge Voltage Threshold	V_{RECH}	Below V_{BATT_REG}, REG04H[0] = 0	60	100	140	mV
		Below V_{BATT_REG}, REG04H[0] = 1	160	200	240	
Battery Auto-recharge Delay Time	t_{RECH_DGL}			200		ms
Thermal Protection						
Junction Temperature Regulation(5)	T_{J_REG}	Thermal_Limit=120ºC		120		ºC
Thermal Shutdown Threshold(5)	T_{J_SHDN}			150		ºC
Thermal Shutdown Hysteresis(5)				20		ºC
NTC bias current	I_{NTC}		49	50	51	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
NTC Cold Temp Rising Threshold	V_{COLD}		1040	1050	1060	mV
NTC Cold Temp Rising Threshold Hysteresis				25		mV
NTC Cooler Temp Rising Threshold	V_{COOLER}		744	751	759	mV
NTC Cooler Temp Rising Threshold Hysteresis				25		mV
NTC Cool Temp Rising Threshold	V_{COOL}		626	632	638	mV
NTC Cool Temp Rising Threshold Hysteresis				25		mV
NTC Warm Temp Falling Threshold	V_{WARM}		229	233	237	mV
NTC Warm Temp Falling Threshold Hysteresis				25		mV
NTC Hot Temp Falling Threshold	V_{HOT}		194	199	204	mV
NTC Hot Temp Falling Threshold Hysteresis				25		mV
Logic IO Pin Characteristics						
Low Logic Voltage Threshold	V_L				0.4	V
High Logic Voltage Threshold	V_H		1.3			V
I²C Interface(SDA, SCL)						
Input High Threshold Level	V_{IH}		1.3			V
Input Low Threshold Level	V_{IL}				0.4	V
Output Low Threshold Level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C Clock Frequency	F_{SCL}				400	kHz
Clock Frequency and Watchdog Timer						
Clock Frequency	F_{CLK}			131		kHz
Watchdog Timer	t_{WDT}	REG05H[5:4] = 11		160		s

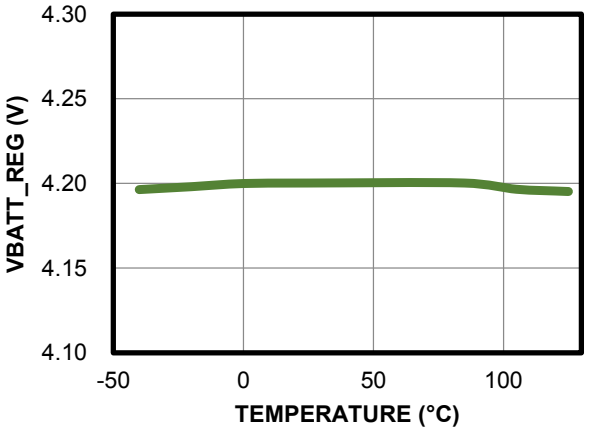
Note:
5) Guaranteed by design

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, I_{IN_LIM} = 500mA, I_{CC}=128mA, T_A = 25°C, unless otherwise noted.

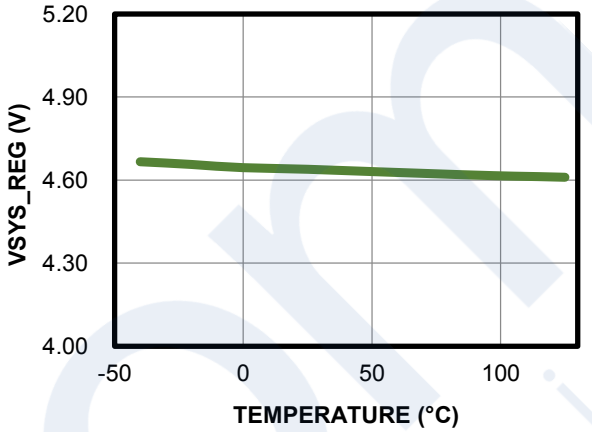
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 4.2V

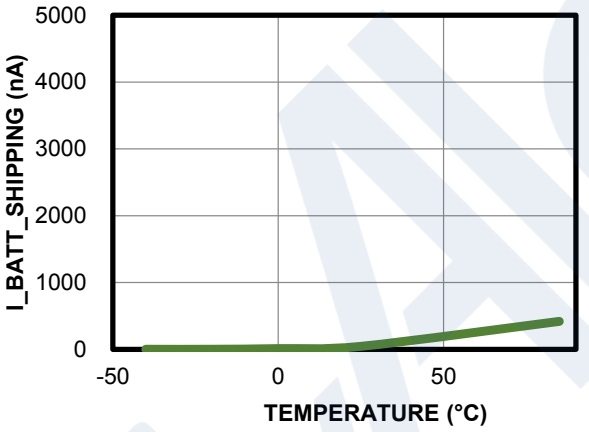


System regulation voltage vs. Temperature

V_{SYS_REG} = 4.65V

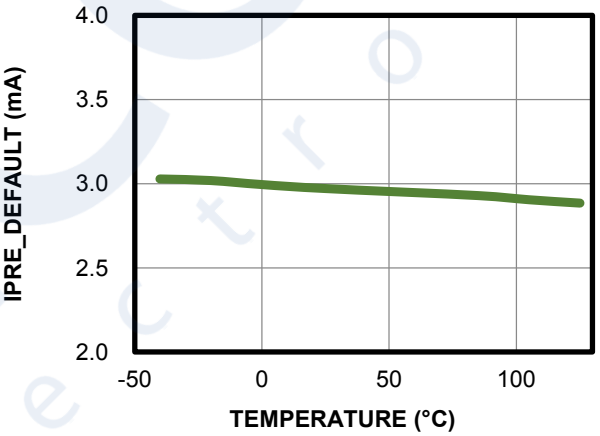


Battery Current Under Shipping Mode vs. Temperature



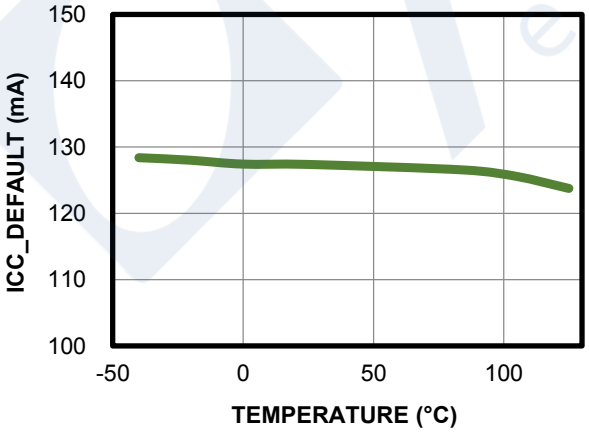
Pre-Charge Current vs. Temperature

Ipre = 3mA



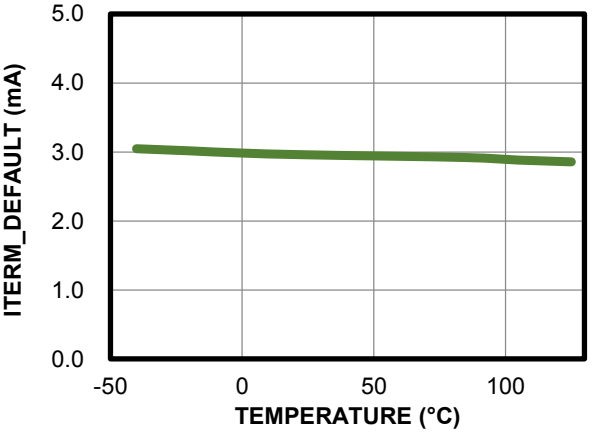
Fast Charge Current vs. Temperature

I_{CC} = 128mA



Battery termination Current vs. Temperature

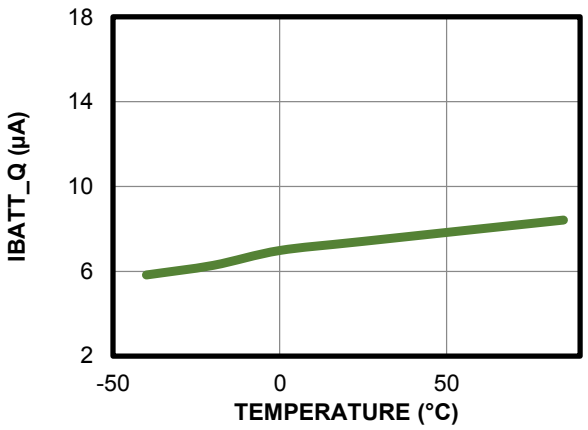
I_{TERM} = 3mA



TYPICAL PERFORMANCE CHARACTERISTICS

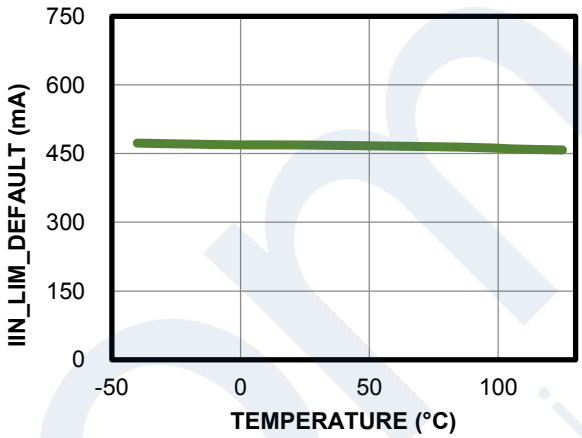
V_{IN} = 5V, I_{IN_LIM} = 500mA, I_{CC}=128mA, T_A = 25°C, unless otherwise noted.

Battery Quiescent Current



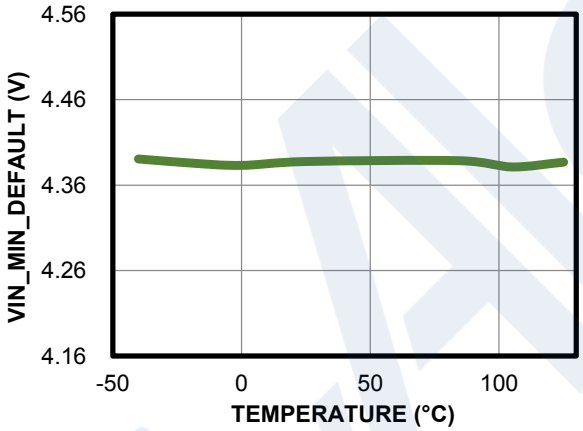
Input Current limit vs. Temperature

I_{IN_LIM} = 500mA



Input minimum Voltage vs. Temperature

V_{IN_MIN} = 4.36V

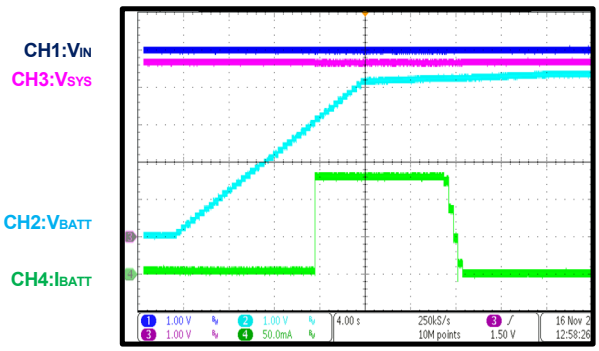


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, I_{IN_LIM} = 500mA, I_{CC}=128mA, T_A = 25°C, unless otherwise noted.

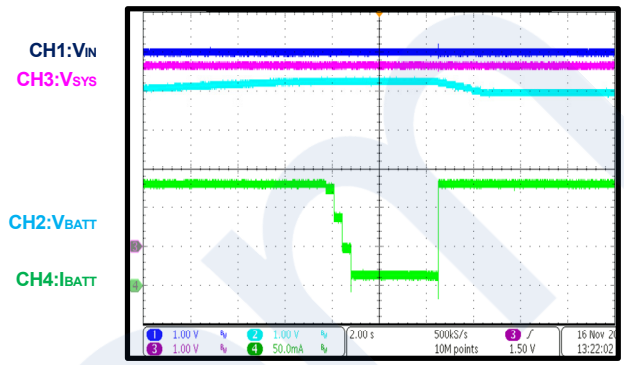
Battery Charge Curve

I_{SYS} = 0A



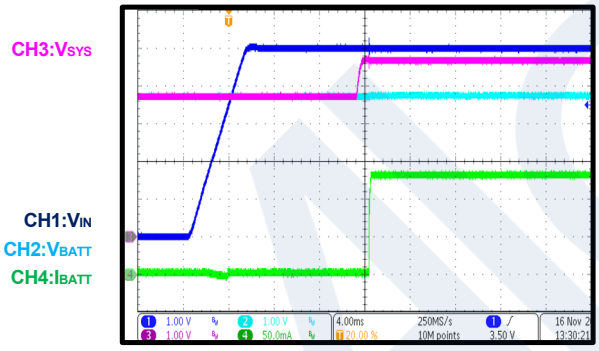
Auto-Recharge

I_{SYS} = 0A



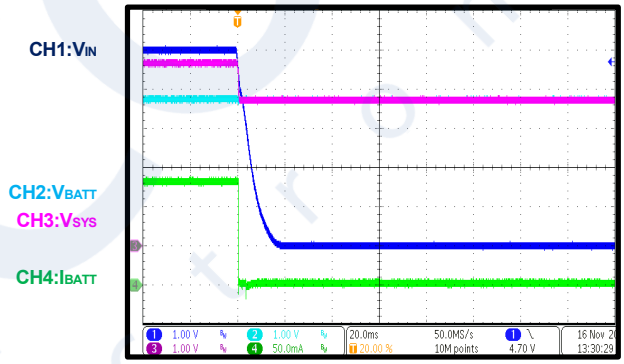
Power On

V_{BATT} = 3.7V, I_{SYS} = 0A



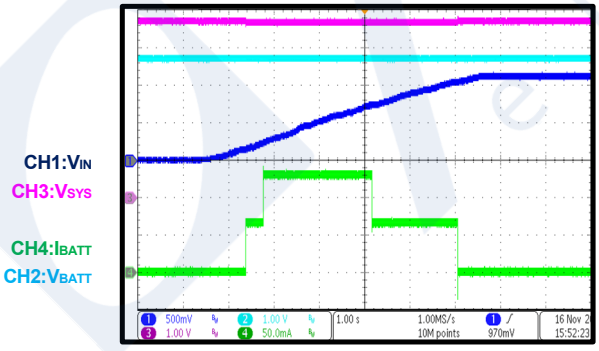
Power Off

V_{BATT} = 3.7V, I_{SYS} = 0A



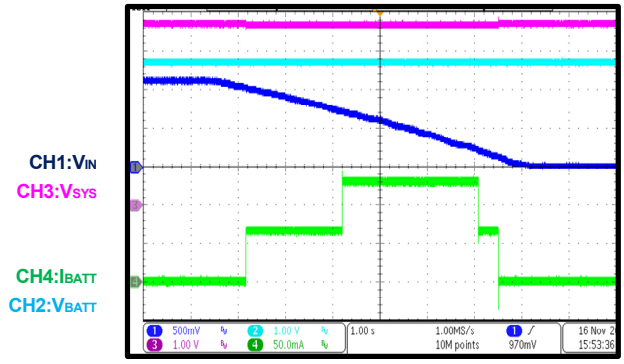
NTC Rising

V_{BATT} = 3.7V, I_{SYS} = 0A



NTC Falling

V_{BATT} = 3.7V, I_{SYS} = 0A

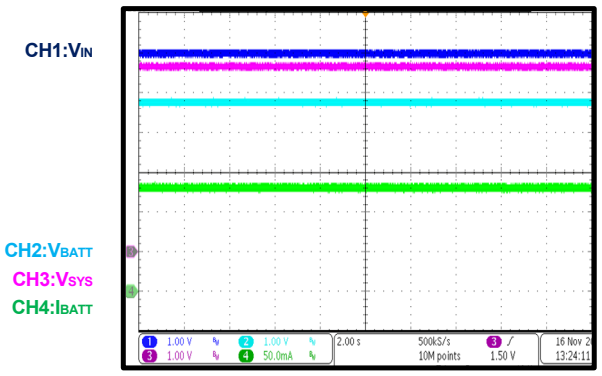


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, I_{IN_LIM} = 500mA, I_{CC}=128mA, T_A = 25°C, unless otherwise noted.

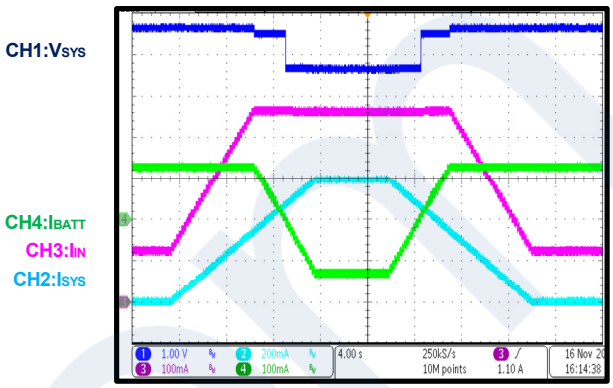
CC Charge Steady State

V_{BATT} = 3.7V, I_{SYS} = 0A



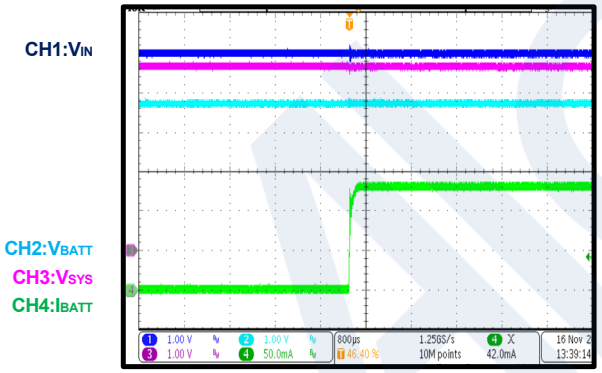
Input Current Limit-Based PPM

V_{BATT} = 3.7V



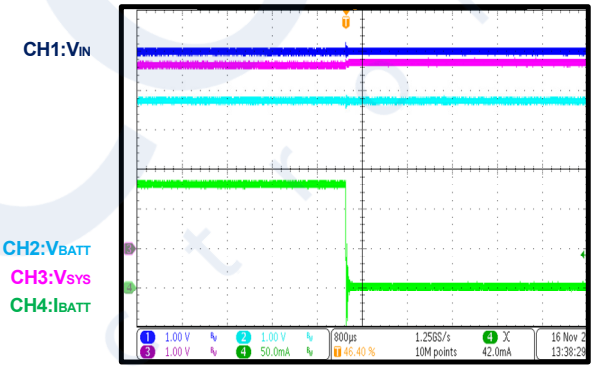
Charge Enable

V_{BATT} = 3.7V, I_{SYS} = 0A



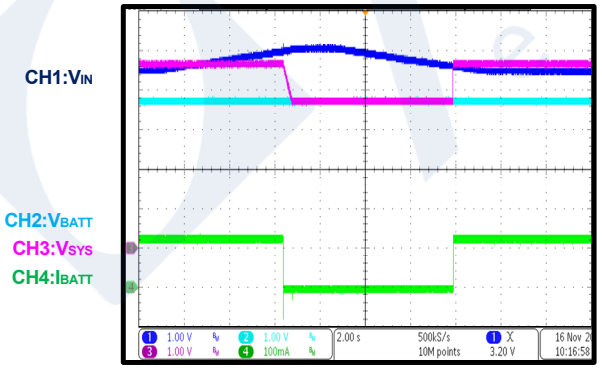
Charge Disable

V_{BATT} = 3.7V, I_{SYS} = 0A



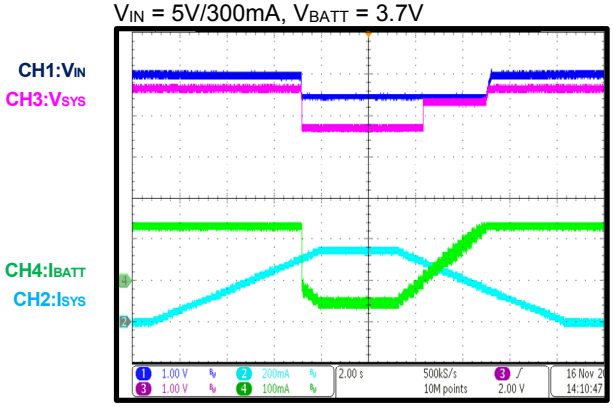
VIN OVP Operation

V_{BATT} = 3.7V, I_{SYS} = 0A



Input Voltage Regulation-Based PPM

V_{IN} = 5V/300mA, V_{BATT} = 3.7V

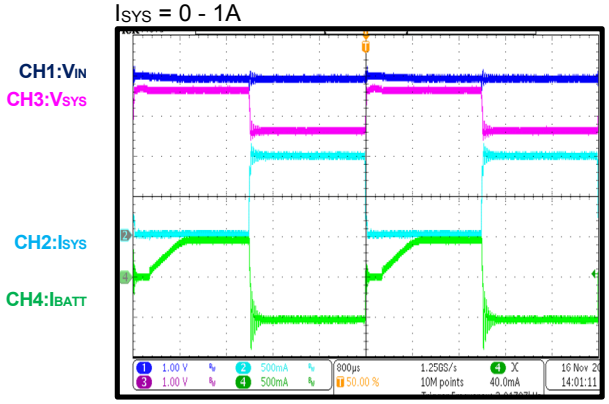


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, I_{IN_LIM} = 500mA, I_{CC}=128mA, T_A = 25°C, unless otherwise noted.

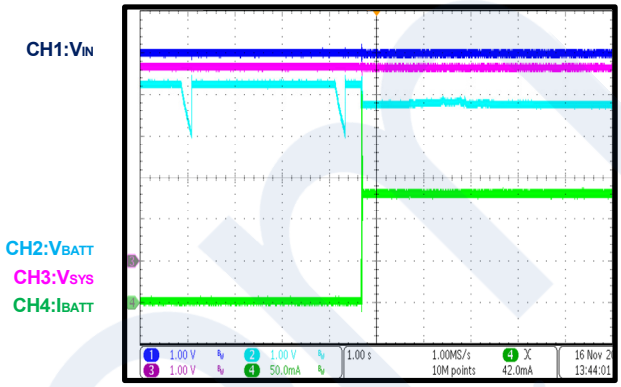
SYS Load Transient

V_{IN} = 5V, V_{BATT} = 3.7V, I_{CC} = 456mA,
I_{SYS} = 0 - 1A



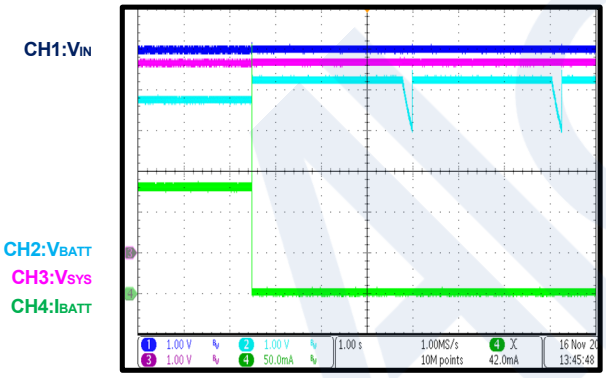
BATT Insertion

V_{BATT} = 3.7V, I_{SYS} = 0A



BATT Removal

V_{BATT} = 3.7V, I_{SYS} = 0A



FUNCTIONAL BLOCK DIAGRAM

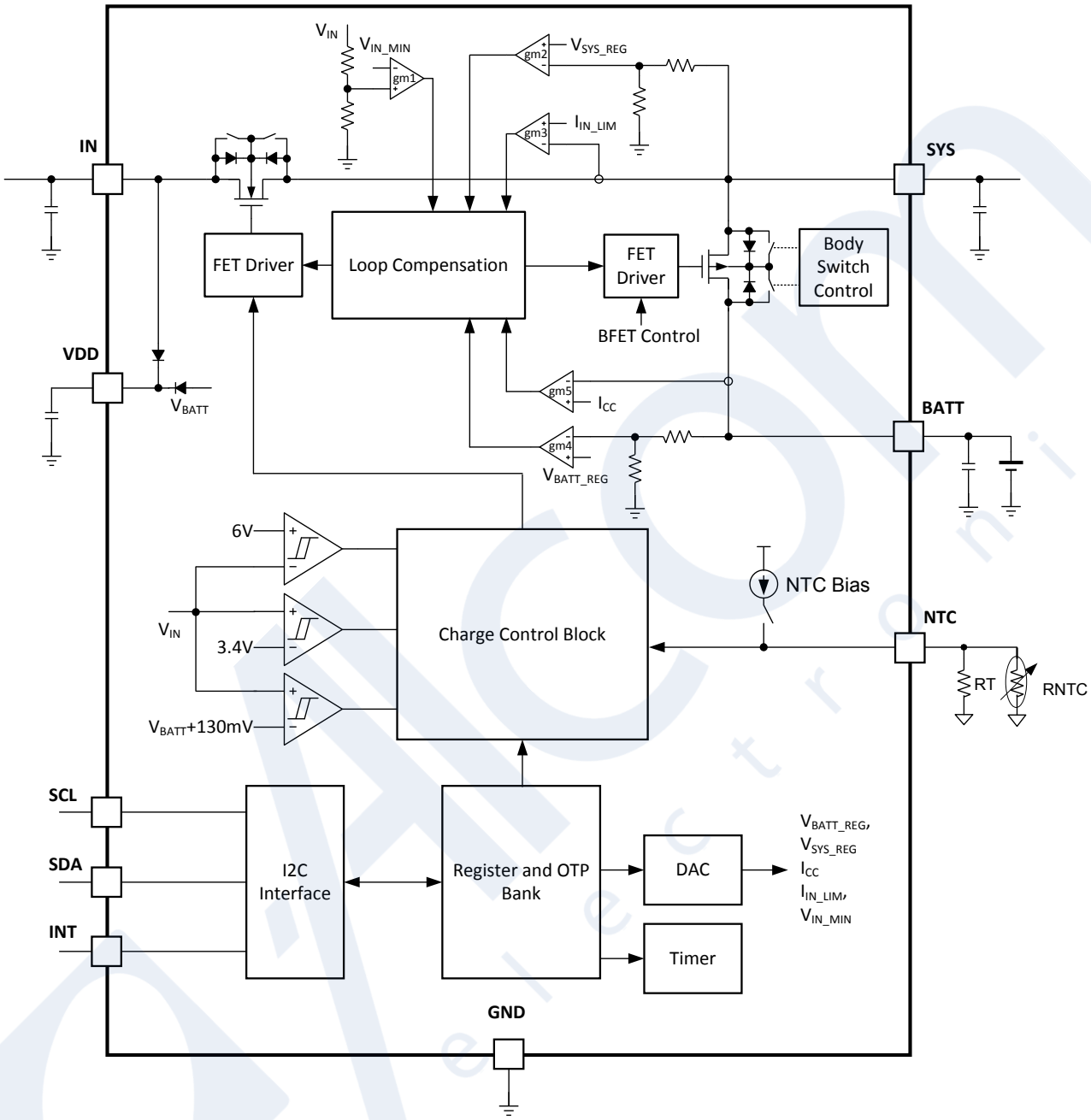


Figure 1: Functional Block Diagram

OPERATION

The MP2710 is an I²C-controlled, single-cell, Li-ion or Li-polymer battery charger with a complete power path management. The full-charge function includes constant-current pre-charge, constant-current fast charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. The system load requirement always has priority to the charge current. When the input power is limited due to an input current limit or input voltage limit, the IC reduces the charge current automatically until the battery supplements the system load.

The IC integrates a 290mΩ LDO FET between IN and SYS and a 100mΩ battery FET between SYS and BATT.

In charging mode, the on-chip 100mΩ battery FET works as a fully featured linear charger with pre-charge, fast charge, constant voltage charge, charge termination, auto-recharge, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmable via the I²C interface. The IC adjusts the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

In supplement mode, the 100mΩ battery FET turns on to connect the battery to the system load when the input power is not sufficient to power the system load. When the input is removed, the 100mΩ battery FET is also fully turned on to allow the battery to power up the system.

The system load is satisfied in priority, and the remaining current is used to charge the smart power path management battery. The MP2710 reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

If the battery is connected and the input source is missing, the IC works in battery discharge mode, the low 100mΩ battery FET and low power mode help to reduce battery current consumption.

Figure 2 shows the power path management for the MP2710.

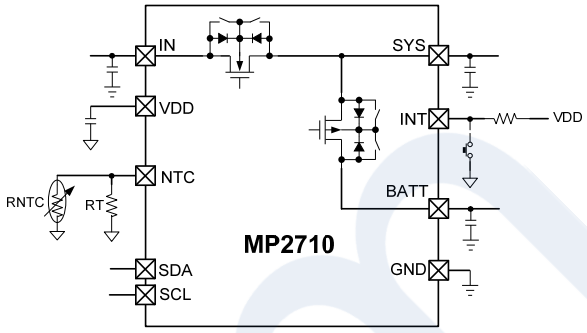


Figure 2: Power Path Management Structure

Table 1 summarizes the functions that are active for each operation mode. Each mode is discussed detail in the following sections.

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of either IN or BATT. When IN or BATT rises above its respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and battery FET driver are all active. The I²C interface is ready for communication, and all registers are reset to the default value. The host can access all of the registers.

Input OVP and UVLO

The MP2710 has an input over-voltage protection (OVP) threshold and input UVLO threshold. Once the input voltage is out of its normal range, the LDO FET (Q1) is turned off immediately.

When the input voltage is identified as a good source, a 10ms glitch filter becomes active. If the input power is normal until the 10ms expires, the system starts up. Otherwise, Q1 remains off (see Figure 3).

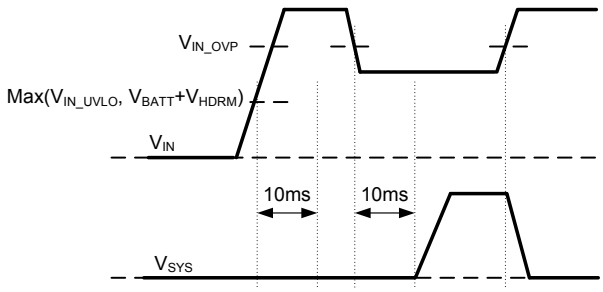


Figure 3: Input Power Detection Operation Profile

Table 1: Function Availability in Different Operation Mode

Function	CHARGE MODE	BATTERY DISCHARGE MODE	LOW POWER MODE	SHIPPING MODE
VINOVP	Yes	No	No	No
VINUVLO	Yes	No	No	No
BATTOCP	Yes	Yes	No	No
BATTUVLO	Yes	Yes	Yes	No
VINDPM	If enabled	No	No	No
IINDPM	Yes	No	No	No
BATFET	Yes	Yes	Yes	No
NTC	If enabled	No	No	No
Charging	If enabled	No	No	No
INT Input	Yes	Yes	Yes	Yes
INT Output	Yes	Yes	No	No
I²C	Yes	Yes	Yes	No
WATCHDOG	If enabled	If enabled	No	No

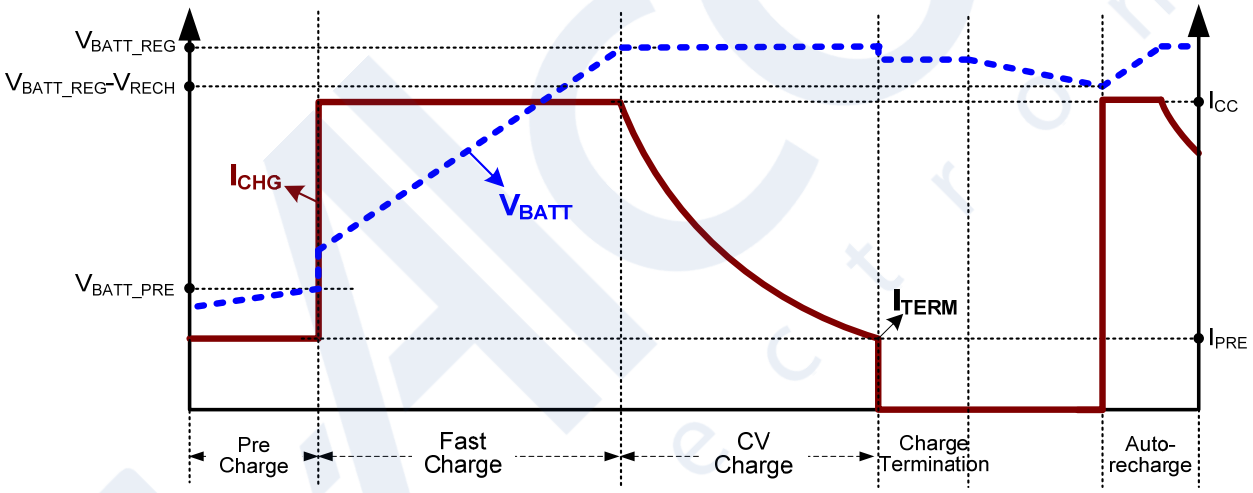


Figure 4: Battery Charge Profile

Power Path Management

The MP2710 employs a power path structure consisting of a front-end LDO FET (Q1) between IN and SYS and a battery FET (Q2) between SYS and BATT. The battery FET decouples the system from the battery, which allows for separate control between the system and the battery. The system has the priority to start up, even with a deeply discharged or missing battery. When input power is available, the system voltage is regulated to V_{SYS_REG} which can be programmable through REG07H Bit[3:0]. The LDO FET and battery FET can be controlled additionally by the I²C as table 2.

Table 2: FET Control via I²C

FET On/Off	Hi-Z Mode and Charge Control	
	Set EN_HIZ to 1	Set CEB to 1
LDO FET	OFF	/
Battery FET (charging)	/	OFF
Battery FET (discharging)	/	/

NOTE: / = not affected.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDO FET is fully on with the input current limit.

Battery Charge Profile

The MP2710 provides three main charging phases: pre-charge, fast-current charge, and constant-voltage charge (see Figure 4).

1. Phase 1 (pre-charge): The MP2710 can safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast-charge threshold (V_{BATT_PRE}). The pre-charge current is also programmed through REG03H bit[3:0]. If V_{BATT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle stops, and a corresponding timeout fault signal is asserted.
2. Phase 2 (fast charge): When the battery voltage exceeds V_{BATT_PRE}, the MP2710 enters a fast-charge phase. The fast-charge current can be programmed via REG02H bit[7:0].
3. Phase 3 (constant-voltage charge): When the battery voltage rises to the battery-full voltage (V_{BATT_REG}) set via REG04H bit[7:2], the charge mode changes from CC mode to CV mode, and the charge current starts decreasing. Note system voltage should be at least 140mV higher than V_{BATT} when fast charger current is lower than 200mA.

The charge cycle completes when the charge current reaches the termination current threshold after a 3.2s termination deglitch time. The termination charge current threshold can be programmed via REG03H bit[3:0].

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation.

A new charge cycle starts when any of the following conditions are valid:

- The input power is recycled.
- Battery charging is enabled via the I²C.
- Auto-recharge kicks in.

Under the following conditions:

- No thermistor fault at NTC.
- No safety timer fault.
- No battery over-voltage event.
- BATT FET is not forced off.

Automatic Recharge

When charge cycle completes, the battery may be discharged due to system consumption or self-discharge. When the battery voltage discharges below the recharge threshold and valid input is still present, the MP2710 begins another new charging cycle automatically.

Battery OVP

The MP2710 is designed with a built-in battery over-voltage limit (about 130mV higher than V_{BATT_REG}). When a battery over-voltage event occurs, the MP2710 suspends charging immediately and asserts a fault.

Input Current- and Input Voltage-Based Power Management

To meet the input source's (typically USB) maximum current limit specification, the MP2710 uses an input current-based power management by monitoring the input current continuously. The total input current limit can be programmable via the I²C to prevent the input source from being over-loaded.

If the preset input current limit is higher than the rating of the input source, the back-up input voltage-based power management also works to prevent the input source from being over-loaded. Either the input current limit or the input voltage limit is reached, the Q1 FET between IN and SYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to a minimum value of V_{SYS_REG} - 100mV and V_{IN} - 145mV, the charge current is reduced to prevent the system voltage from dropping further.

The voltage-based DPM regulates the input voltage to V_{IN_MIN} when the load is over the input power capacity. The input voltage limit function can be disabled by REG07H bit[6].

Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is reduced to zero and the input source is still overloaded due to a heavy system load, the system voltage begins decreasing. Once the system voltage drops to 30mV below the battery voltage, the MP2710 enters battery supplement mode, and the ideal diode mode is enabled. The battery FET is regulated to keep V_{BATT} - V_{SYS} at 22.5mV when I_{DSCHG} (supplement current) * R_{ON_BATT} is lower than 22.5mV. In the case that I_{DSCHG} * R_{ON_BATT} is higher than 22.5mV, the battery FET is fully turned on to maintain the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than V_{BATT} + 20mV, the ideal diode mode is disabled. Figure 5 shows the dynamic power management and battery supplement mode operation profile.

When V_{IN} is not available, the MP2710 operates in discharge mode, and the battery FET is always fully on to reduce loss.

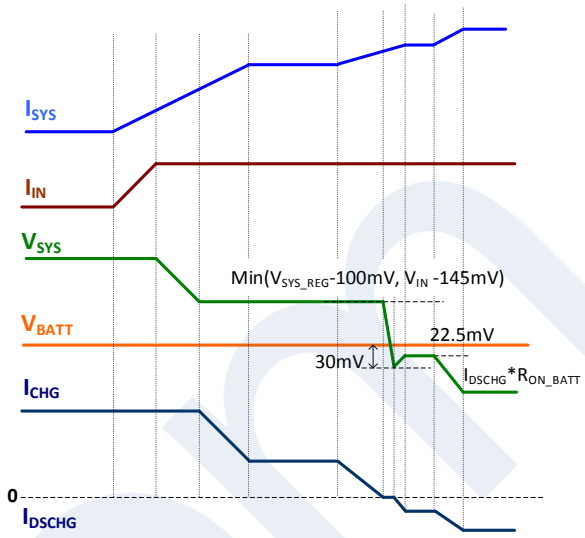


Figure 5: Dynamic Power Management and Battery Supplement Operation Profile

Thermal Regulation and Thermal Shutdown

The MP2710 monitors the internal junction temperature continuously to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset limit of T_{J_REG} (120°C default), the IC starts to reduce the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60 - 120°C help the system design meet the thermal requirements in different applications. The junction temperature regulation threshold can be set via REG07H bit[5:4].

When the junction temperature reaches 150°C, both Q1 and Q2 turn off.

Negative Temperature Coefficient (NTC) Temperature Sensor

The MP2710 continuously monitors battery's temperature by measuring the NTC pin voltage, which is created by an internal precise NTC bias current flowing out NTC pin to thermistor. The MP2710 compares this voltage to internal threshold to determine which fault happens and take different actions accordingly. This current is only active when V_{IN} is present and can be disabled by writing 0 to EN_NTC bit.

The MP2710 monitors five battery temperatures: the hot battery temperature, the warm battery temperature, the cool battery temperature, the cooler battery temperature, and the cold battery temperature. These temperatures correspond

to the V_{HOT}, V_{WARM}, V_{COOL}, V_{COOLER}, and V_{COLD} threshold in Electrical Characteristics table, these thresholds can be adjusted by REG0BH register.

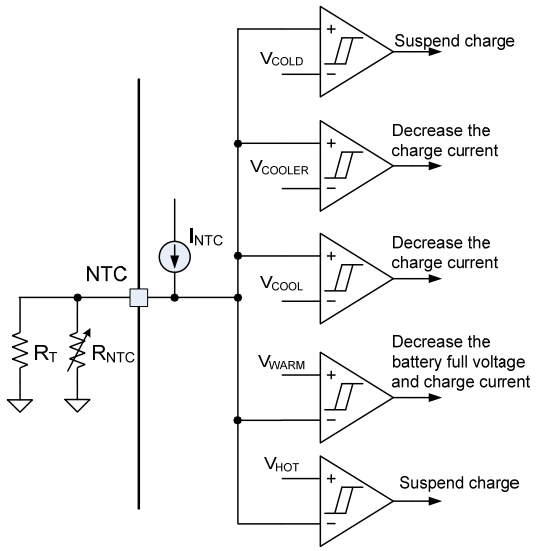


Figure 6: NTC Protection Circuit

The NTC protection circuit is shown in Figure 6, the NTC pin operation voltage is up to 1.2V. The MP2710 supports the following thresholds by default for 10kΩ NTC. For accurate temperature thresholds, a 10kΩ NTC with a 3435 B-constant should be used with a parallel 91kΩ resistor.

Table 3: NTC Threshold for 10kΩ Thermistor

VNTC (V)	Temperature (°C)
0.146	60
0.233	45
0.751	10
1.049	0

Charging and safety timer are suspended when $V_{NTC}<V_{HOT}$ or $V_{NTC}>V_{COLD}$, when $V_{HOT}<V_{NTC}<V_{WARM}$, the battery regulation voltage is reduced to the value programmed by the Hot_warm_VSET bit, the charging current is reduced to the value programmed by the Hot_warm_ISET[1:0] bits. When $V_{COOL}<V_{NTC}<V_{COOLER}$, the charging current is reduced to the value programmed by the Cool_cooler_ISET[1:0] bits. When $V_{COOLER}<V_{NTC}<V_{COLD}$, the charging current is reduced to the value programmed by the Cooler_cold_ISET[1:0] bits. NTC protection action is shown in Figure 7.

When a NTC fault occurs, an INT is asserted, and the fault bits are updated.

The five adjustable temperature threshold and programmed charging current reduced value allow the user to easily meet the JEITA standard or a simpler HOT/COLD function only.

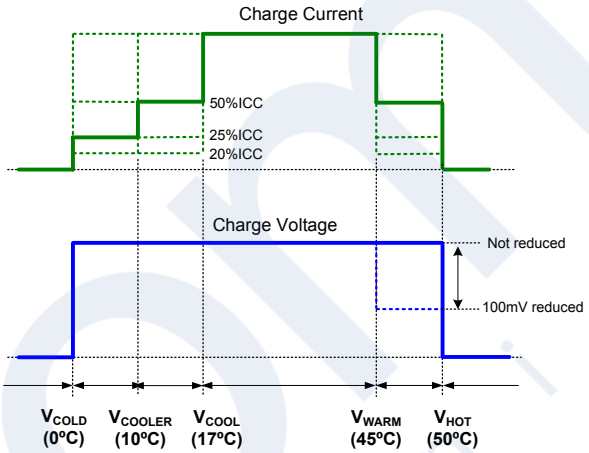


Figure 7: NTC Protection Action

Safety Timer

The MP2710 provides both a pre-charge and fast-charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer is 1hr when the battery voltage is lower than V_{BATT_PRE}. The fast-charge safety timer starts when the battery enters fast-charge mode. The fast-charge safety timer can be programmable through the I²C. The safety timer can be disabled via the I²C.

The following actions can restart the safety timer:

- A new charge cycle is kicked in.
- Write REG01H bit[3] from 1 to 0 (charge enable).
- Write REG01H bit[4] from 1 to 0 (HIZ disable).

Watchdog Timer Function

The watchdog timer works in both charge and discharge mode. When the watchdog timer runs out, most registers return to the default value (refer to the I²C Register Map section). When the watchdog timer is out in both charge and discharge mode, both the LDO FET and battery FET are turned off. They turn on again automatically after 4s.

To save quiescent current during discharge mode, the watchdog timer can be turned off during by setting REG05H bit[7] to 0.

If the watchdog timer (REG05H bit[6:5]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to REG06H bit[7] before the watchdog timer expires. The watchdog timer can also be programmable or disabled by the host control.

When the REG05H bit[6:5] is set to 00, then the watchdog timer is disabled under both charge mode and discharge mode regardless of the status of REG05H bit[7].

Battery Discharge Mode

If the battery is connected and the input source is missing, the battery FET is fully on when V_{BATT} is above the V_{BATT_UVLO} threshold. The 100mΩ battery FET minimizes conduction loss during battery discharging, the battery quiescent current is as low as 8μA in this mode. MP2710 has a low power mode which is enabled by setting REG07H Bit[7] to 1, in this mode, the battery quiescent current can be as low as 1.5μA. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The MP2710 has an over-discharge current protection in discharge mode and supplement mode. Once I_{BATT} exceeds the programmable discharge current limit (2A default), the battery FET turns off after a 60μs delay. The MP2710 enters hiccup mode as part of the over-current protection (OCP). The discharge current can be programmed high to 3.2A through the I²C. If the discharge current goes high and reaches the internal fixed current limit (about 3.7A), the battery FET turns off and begins hiccup mode immediately.

Similarly, when the battery voltage falls below the programmable V_{BATT_UVLO} threshold (2.76V default), the battery FET turns off to prevent an over-discharge.

System Short-Circuit Protection (SCP)

The MP2710 features SYS node short-circuit protection (SCP) for both the IN to SYS path and the BATT to SYS path.

The system voltage is monitored continuously. If V_{SYS} is lower than 1.5V, system SCP for both the IN to SYS path and the BATT to SYS path is active. I_{DSCHG} decreases to half of the original value.

For the IN to SYS path, once I_{IN} is over the protection threshold, both the LDO FET and battery FET are turned off immediately, and the MP2710 enters hiccup mode. When the setting input current limit is reached, I_{IN} is regulated at I_{IN_LIM}. Hiccup mode also starts after a 60μs delay. The hiccup mode interval is 800μs.

For the BATT to SYS path, once I_{BATT} is over the 3.7A protection threshold, both the LDO FET and battery FET are turned off immediately, and the MP2710 enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The hiccup mode interval is 800μs.

Particularly, if a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths works. The faster one of the two dominates the hiccup operation.

Interrupt to Host (INT)

The MP2710 also has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of the below events can trigger an INT output:

- Good input source detected (PG_STAT)
- Charge completed
- Charging status change
- Any fault in REG09H (watchdog timer fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the MP2710 sends out an INT pulse and latches the fault state in REG09H. After the MP2710 exits the fault state, the fault bit is reset to 0 after the host reads REG09H. The NTC fault is not latched and always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set in REG06H bit[4:0]. When an INT condition is masked, this means that the INT pin signal (and register bit) will not trigger when the corresponding

condition occurs. Masking INTs is useful when writing software code to avoid unnecessary interruptions due to these events.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system to reset system power during application or to enter shipping mode. The MP2710 provides both system reset mode and shipping mode (shown in Table 4) for different applications.

The MP2710 uses pulling INT pin low to reset the system. Once the logic at INT is set low for longer than t_{RST_DGL} which is programmable by REG01H Bit[7:6], the battery is disconnected from the system by turning off the battery FET, the LDO FET is also turned off if Vin is present. The off state lasts for t_{RST_DUR}, which is programmable by REG01H Bit[5], then the battery FET turns on automatically, the LDO FET turns on too if Vin is present, and the system is powered on again. As system reset with battery only in Figure 8.

MP2710 has two ways to enter shipping mode which is selected by SHIP_METH OTP bit.

If SHIP_METH=0, entering shipping mode by software is selected. The IC enters shipping mode when setting FET_DIS bit to 1, the delay time of entering shipping mode is programmable in REG0AH Bit[5:4]. The FET_DIS bit refreshes to 0 after entering shipping mode. There are two ways to exit shipping mode, plug in Vin for 80ms which can be programmable by REG0AH Bit[2], as in Figure 9, or pull the INT pin low for 2s.

If SHIP_METH=1, entering shipping mode by hardware is selected. Pull INT pin low for 16s which is programmable by REG01H Bit[7:6], the IC enters shipping mode. To exit shipping mode, plug in Vin for 80ms or pull the INT pin low again for 2s, as in Figure 10. Note, system reset mode is not available if SHIP_METH=1.

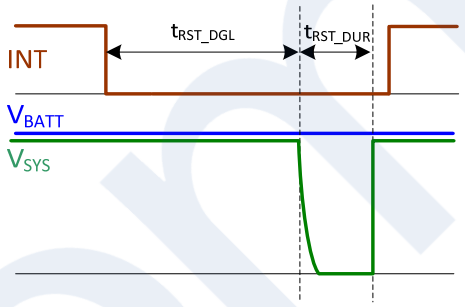


Figure 8: System Reset Mode Operation

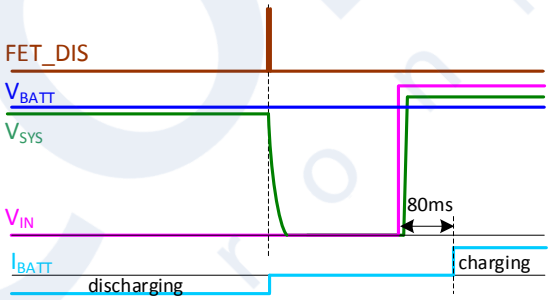


Figure 9: Enter Shipping Mode by I²C

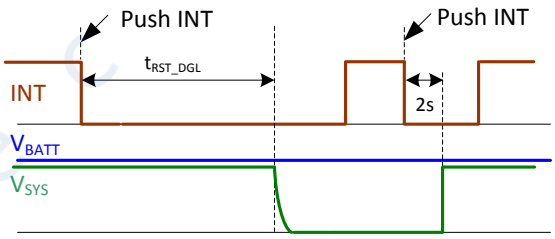


Figure 10: Enter Shipping Mode by Hardware

Table 4: Shipping Mode Control

Items	Enter Shipping Mode	Exit Shipping Mode	
	Set FET_DIS to 1 (or pull INT low if SHIP_METH=1)	INT H to L for 2s	V_{IN} Plug-In
LDO FET	/	/	on (10ms later)
Battery FET	off	on	on (80ms later)

NOTE: / = not affected

SERIES INTERFACE

The IC uses an I²C compatible interface for flexible charging parameters setting and instantaneous device status reporting. I²C™ is a bidirectional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). The device can be considered a master or a slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit the transfer. At that time, any device addressed is considered as a slave.

MP2710 operates as a slave device with the address 07H, receiving control inputs from the master device, like a micro controller or a digital signal processor. MP2710 is made to ignore general call address.

The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). Both SDA and SCL are bi-direction lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

The Data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred (see Figure 11).

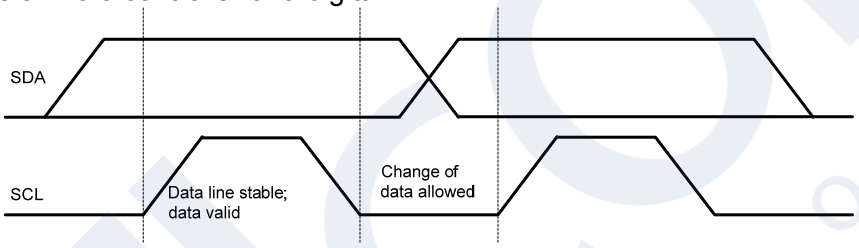


Figure 11: Bit Transfer on the I2C Bus

All the transactions begin with a START(S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition (see Figure 12).

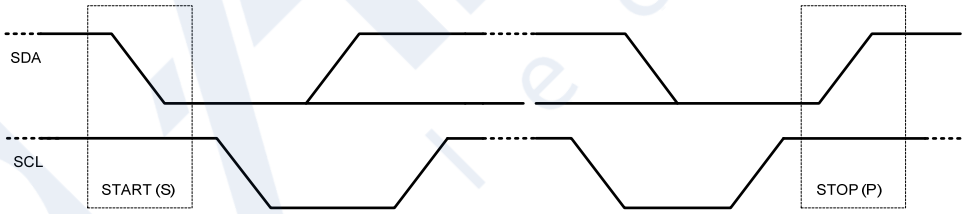


Figure 12: START and STOP Conditions

Every byte on the SDA line must be 8 bits long. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL (see Figure 13).

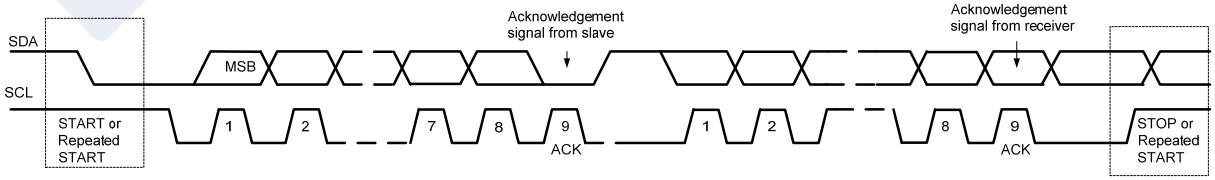


Figure 13: Data transfer on the I2C BUS

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line LOW. The SDA line remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

After the START, a slave address is sent. This address is 7 bits long followed by the 8th a data direction bit (bit R/W), A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The complete data transfer is shown in Figure 14.

If the register address is not defined, MP2710 sends back NACK and go back to the idle state.

MP2710 supports single-write and single-read, shown in Figure 15 and Figure 16.

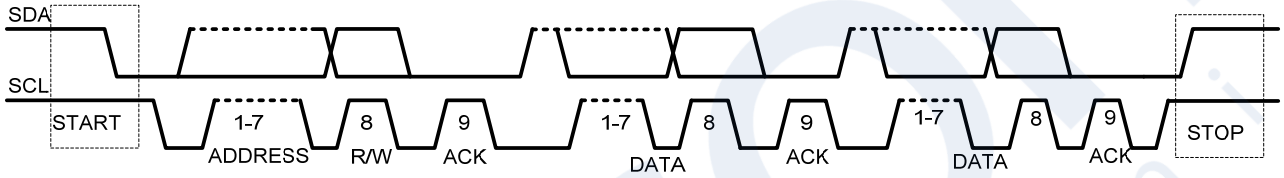


Figure 14: Complete Data Transfer

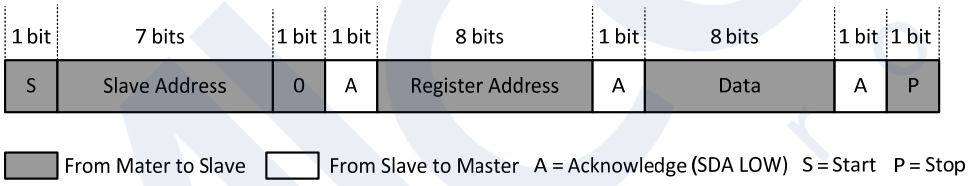


Figure 15: Single Write

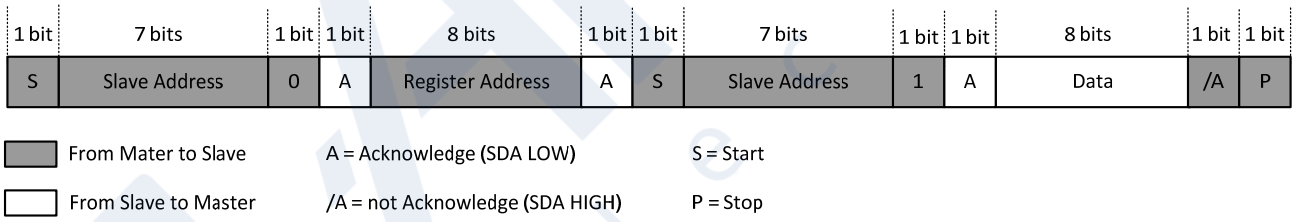


Figure 16: Single Read

APPLICATION INFORMATION

RESISTOR SELECTION FOR NTC SENSOR

The MP2710 supports 10kΩ NTC thermistor with 3435 B-constant. Every internal threshold is divided from 1.2V reference voltage based on precise 50μA current flowing through 10kΩ NTC thermistor in parallel with 91kΩ resistor as shown in Figure 17. User needs to put a 91kΩ resistor in parallel with 10kΩ NTC to get accurate temperature protection threshold. User can adjust threshold by configuring REG0BH register.

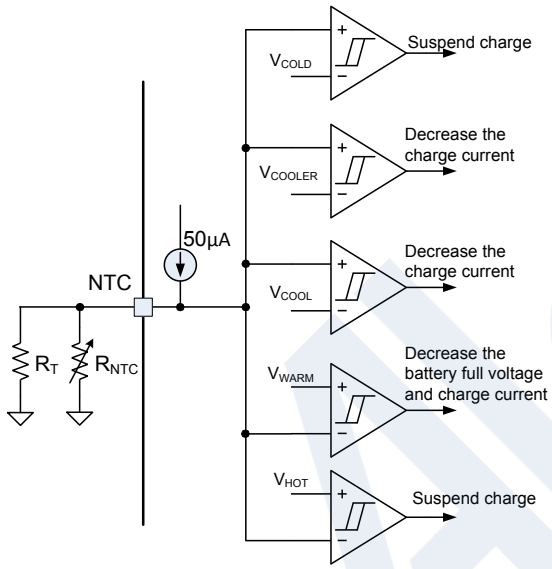


Figure 17: NTC Function Block

EXTERNAL CAPACITOR SELECTION

Like most low-dropout regulators, the MP2710 requires external capacitors for regulator stability and voltage spike immunity. The device is designed for portable applications requiring minimum board space and smallest components, these capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitor is required for stability, at least, a 1uF capacitor has to be connected between IN to GND for stable operation over full load current range. Basically, it is OK to have more output capacitance than input, as long as the input is at least 1uF.

Output Capacitor

The IC is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor (dielectric types X5R or X7R) at least 4.7uF is suitable in the MP2710 application circuit. For this device, the output capacitor should be connected between SYS pin and GND pin with thick trace and small loop area.

BATT to GND Capacitor

The capacitor from BATT pin to GND is also necessary for MP2710. A ceramic capacitor (dielectric types X5R or X7R) at least 4.7uF is suitable for the MP2710 application circuit.

VDD to GND Capacitor

The capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB LAYOUT GUIDE

1) Put the external capacitors as close to the IC as possible to make sure the smallest input inductance and the ground impedance.

2) The PCB trace to connect the capacitor between VDD and GND is very important, and it should be put very close to the IC.

3) The GND for the I²C wire should be clean, and it should not be very close to the GND.

4) I²C wire should be put in parallel.

TYPICAL APPLICATION CIRCUITS

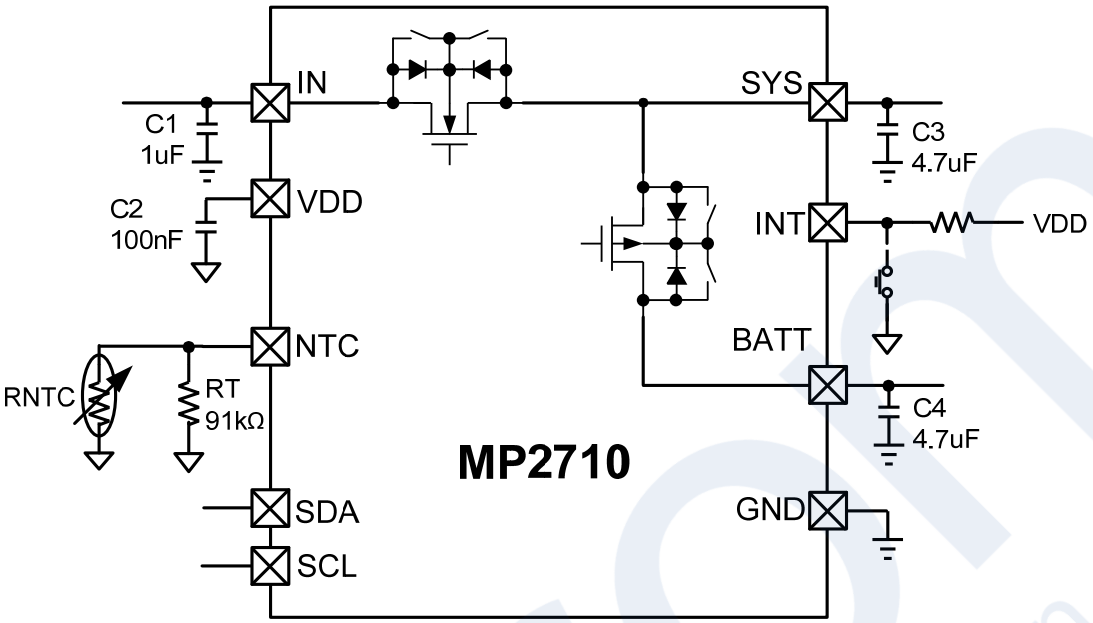


Figure 18: Application Circuit Name

Table 5: Key BOM of Figure 18

Qty	Ref	Value	Description	Package	Manufacture
1	C1	1μF	Ceramic Capacitor;25V; X5R or X7R	0603	Any
1	C2	100nF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
1	C3	4.7μF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	C4	4.7μF	Ceramic Capacitor;16V; X5R or X7R	0603	Any

I²C REGISTER MAP

IC Address: 08H (Reserved some trim options)

Register Name	Address	R/W	Description
REG00H	0x00	R/W	Input Source control register
REG01H	0x01	R/W	Power on configuration register
REG02H	0x02	R/W	Charge Current Control Register
REG03H	0x03	R/W	Termination Current
REG04H	0x04	R/W	Charge Voltage Control Register
REG05H	0x05	R/W	Charge Termination/Timer Control Register
REG06H	0x06	R/W	BATFET Control and INT Mask
REG07H	0x07	R/W	Low Power Mode and System Voltage Register
REG08H	0x08	R	Status Register
REG09H	0x09	R	Fault Register
REG0AH	0x0A	R/W	Shipping mode delay and NTC control
REG0BH	0x0B	R/W	NTC Temperature Threshold
REG0CH	0x0C	R/W	NTC Action
REG0DH	0x0D	R/W	Battery Discharge Current Limit

REG 00H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VIN_MIN [3]	0	Y	N	R/W	640mV	Offset: 3.88V Range:3.88V – 5.08V Default: 4.36V (0110)
6	VIN_MIN [2]	1	Y	N	R/W	320mV	
5	VIN_MIN [1]	1	Y	N	R/W	160mV	
4	VIN_MIN [0]	0	Y	N	R/W	80mV	
3	IIN_LIM [3]	1	Y	N	R/W	240mA	Offset:50mA Range:50mA -500mA Default: 500mA (1111)
2	IIN_LIM [2]	1	Y	N	R/W	120mA	
1	IIN_LIM [1]	1	Y	N	R/W	60mA	
0	IIN_LIM [0]	1	Y	N	R/W	30mA	

REG 01H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	tRST_DGL[1]	1	Y	N	R/W	00: 8s 01: 12s 10: 16s 11: 20s	The deglitch time of pull INT low to reset system, after t_{RST_DUR}, Vsys recovers. It is also the delay of enter shipping mode if EN_SHIP=1 (by hardware). Default: 10 (16s)
6	tRST_DGL[0]	0	Y	N	R/W		
5	tRST_DUR	0	Y	N	R/W	0: 2s 1: 4s	Default: 2s (0)
4	EN_HIZ(6)	0	Y	Y	R/W	0: Disable, 1: Enable	Default: Disable (0)
3	CEB	1	Y	Y	R/W	0: Charge Enable, 1: Charge Disabled	Charge configuration Default: charge disabled (1) **OTP**
2	VBATT_UVLO [2]	1	Y	Y	R/W	360mV	Battery UVLO Threshold Offset: 2.4V Range: 2.4V- 3.03V Default: 2.76V (100)
1	VBATT_UVLO [1]	0	Y	Y	R/W	180mV	
0	VBATT_UVLO [0]	0	Y	Y	R/W	90mV	

Note:
6) This bit only controls the on and off of the LDO FET.

REG 02H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	ICC [7]	0	Y	Y	R/W	256mA	Fast Charge Current Setting Offset: 2mA Range: 8mA – 456mA Default: 128mA (00111111) OTP Note: ICC<00000011 (mA) is clamped to 00000011 (8mA)
6	ICC [6]	0	Y	Y	R/W	128mA	
5	ICC [5]	1	Y	Y	R/W	64mA	
4	ICC [4]	1	Y	Y	R/W	32mA	
3	ICC [3]	1	Y	Y	R/W	16mA	
2	ICC [2]	1	Y	Y	R/W	8mA	
1	ICC [1]	1	Y	Y	R/W	4mA	
0	ICC [0]	1	Y	Y	R/W	2mA	

REG 03H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	IPRE [3]	0	Y	Y	R/W	16mA	Pre Charge Current Offset: 1mA Range: 1mA-31mA Default: 3mA(0001) OTP
6	IPRE [2]	0	Y	Y	R/W	8mA	
5	IPRE [1]	0	Y	Y	R/W	4mA	
4	IPRE [0]	1	Y	Y	R/W	2mA	
3	ITERM [3]	0	Y	Y	R/W	16mA	Termination Current Offset: 1mA Range: 1mA-31mA Default: 3mA(0001) OTP
2	ITERM [2]	0	Y	Y	R/W	8mA	
1	ITERM [1]	0	Y	Y	R/W	4mA	
0	ITERM [0]	1	Y	Y	R/W	2mA	

REG 04H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VBATT_REG [5]	1	Y	Y	R/W	480mV	Battery Regulation Voltage Offset: 3.60V Range: 3.60V – 4.545V Default: 4.2V (101000) OTP
6	VBATT_REG [4]	0	Y	Y	R/W	240mV	
5	VBATT_REG [3]	1	Y	Y	R/W	120mV	
4	VBATT_REG [2]	0	Y	Y	R/W	60mV	
3	VBATT_REG [1]	0	Y	Y	R/W	30mV	
2	VBATT_REG [0]	0	Y	Y	R/W	15mV	
1	Reserved	NA	NA	NA	NA		
0	VRECH[0]	1	Y	Y	R/W	0: 100mV 1: 200mV	Battery Recharge Threshold (below V_{BATT_REG}) Default: 200mV (1)

REG 05H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_WD_DISCHG	0	Y	N	R/W	0: Disable; 1: Enable	Watchdog Control in discharge mode Default: Disable (0)
6	WATCHDOG [1]	0	Y	N	R/W	00: Disable Timer; 01: 40s; 10: 80s; 11: 160s	I²C Watchdog Timer Limit Default: 40s (01) If Bit [6:5]=00, then watchdog timer is disabled no matter Bit 7 is set or not. OTP
5	WATCHDOG [0]	1	Y	N	R/W		
4	EN_TERM	1	Y	Y	R/W	0: Disable; 1: Enable	Termination Setting (control the termination is allowed or not) Default: Enable (1)
3	EN_TIMER	1	Y	Y	R/W	0: Disable; 1: Enable	Safety Timer Setting Default: Enable Timer (1)
2	CHG_TMR [1]	0	Y	Y	R/W	00: 3hrs; 01: 5hrs; 10: 8hrs; 11: 12hrs	Fast Charge Timer Default: 5hrs (01)
1	CHG_TMR [0]	1	Y	Y	R/W		
0	VBATT_PRE	1	Y	Y	R/W	0: 2.8V; 1: 3.0V	Pre-charge to Fast Charge Threshold Default: 3.0V (1)

REG 06H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I2C Watchdog Timer Reset	0	Y	Y	R/W	0: Normal; 1: Reset	Default: Normal (0)
6	TMR2X_EN	1	Y	Y	R/W	0: Disable 2X extended safety timer during PPM, 1: Enable 2X extended safety timer during PPM	Default: Enable (1)
5	FET_DIS(7)	0	Y	N	R/W	0: Enable 1: Turn Off	Default: Enable (0)
4	PG_INT_Control	0	Y	Y	R/W	0: On; 1: Off	Default: On (0)
3	EOC_INT_Control	0	Y	Y	R/W	0: On; 1: Off	**Charge Completed INT Mask Control** Default: On (0)
2	CHG STATUS_INT_Control	0	Y	Y	R/W	0: On; 1: Off	**Charging Status Change INT Mask Control (charging status contain: not charging, pre charge and charge)** Default: On (0)
1	NTC_INT_Control	0	Y	Y	R/W	0: On; 1: Off	Default: On (0)
0	BATTOVP_INT_Control	0	Y	Y	R/W	0: On; 1: Off	Default: On (0)

Note:
7) This bit controls the on and off of the Battery FET include charge and discharge.

REG 07H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	LPM_EN	0	Y	N	R/W	0: Disable; 1: Enable	Low Power Mode Default: Disable (0)
6	EN_VINLOOP	0	Y	Y	R/W	0: Enable; 1: Disable	Default: Enable (0)
5	TJ_REG [1]	1	Y	Y	R/W	00: 60ºC; 01: 80 ºC; 10: 100 ºC; 11: 120ºC;	Thermal Regulation Threshold Default: 120ºC (11)
4	TJ_REG [0]	1	Y	Y	R/W		
3	VSYS_REG [3]	1	Y	N	R/W	400mV	System Voltage Regulation Offset: 4.2V Range: 4.2V – 4.95V Default: 4.65V (1001) OTP
2	VSYS_REG [2]	0	Y	N	R/W	200mV	
1	VSYS_REG [1]	0	Y	N	R/W	100mV	
0	VSYS_REG [0]	1	Y	N	R/W	50mV	

REG 08H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG_FAULT	0	NA	NA	R	0: Normal; 1: Watchdog timer expiration	Normal (0)
6	Reserved	0	NA	NA	R		
5	CHG_STAT [1]	0	NA	NA	R	000: Not Charging; 001: Pre Charge; 010: CC Charge; 011: CV Charge; 100: Charge Done	Not Charging (000)
4	CHG_STAT [1]	0	NA	NA	R		
3	CHG_STAT [0]	0	NA	NA	R		
2	PPM_STAT	0	NA	NA	R	0: No PPM 1: IN PPM	No PPM (0)
1	PG_STAT	0	NA	NA	R	0: Power Fail, 1: Power Good	Power Fail (0)
0	THERM_STAT	0	NA	NA	R	0: No Thermal Regulation; 1: In Thermal Regulation	Normal (0)

REG 09H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Register Reset	0	Y	N	R/W	0: Normal; 1: Reset	Default: Normal (0)
6	VIN_FAULT	0	NA	NA	R	0: Normal; 1: Input fault (OVP or bad source)	Default: Normal (0)
5	THEM_SD	0	NA	NA	R	0: Normal, 1: Thermal Shutdown	Default: Normal (0)
4	BAT_FAULT	0	NA	NA	R	0: Normal 1: Battery OVP	Default: Normal (0)
3	STMR_FAULT	0	NA	NA	R	0: Normal; 1: Safety Timer Expiration	Default: Normal (0)
2	NTC_FAULT [2]	0	NA	NA	R	000: Normal, 001: NTC hot, 010: NTC warm, 011: NTC cool, 100: NTC cooler, 101: NTC cold,	Default: Normal (000)
1	NTC_FAULT [1]	0	NA	NA	R		
0	NTC_FAULT [0]	0	NA	NA	R		

REG 0AH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	NA	NA	NA	NA		
6	Reserved	NA	NA	NA	NA		
5	tESM_DGL[1]	0	Y	N	R/W	00: 1s; 01: 2s; 10: 4s; 11: 8s;	Enter shipping mode deglitch time Default: 1s (00)
4	tESM_DGL[0]	0	Y	N	R/W		
3	Reserved	NA	NA	NA	NA		
2	tEXSM_DGL	0	Y	N	R/W	0: 80ms; 1: 2s;	Exit shipping mode delay time by Vin plug in Default: 80ms (0) OTP
1	Reserved	NA	NA	NA	NA		
0	EN_NTC	0	Y	Y	R/W	0: Disable; 1: Enable	Default: Disable (0) OTP

REG 0BH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VHOT[1]	0	Y	Y	R/W	00: 146mV; (60°C) 01: 170mV; (55°C) 10: 181mV; (53°C) 11: 199mV; (50°C)	Hot Threshold Default: 146mV (00) OTP
6	VHOT[0]	0	Y	Y	R/W		
5	VWARM[1]	0	Y	Y	R/W	00: 199mV; (50°C) 01: 233mV; (45°C) 10: 248mV; (43°C) 11: 322mV; (35°C)	Warm Threshold Default: 233mV (01)
4	VWARM[0]	1	Y	Y	R/W		
3	VCOOL[1]	1	Y	Y	R/W	00: 534mV; (20°C) 01: 591mV; (17°C) 10: 632mV; (15°C) 11: 751mV; (10°C)	Cool Threshold Default: 751mV (11) OTP
2	VCOOL[0]	1	Y	Y	R/W		
1	VCOOLER	1	Y	Y	R/W	0: 632mV; (15°C) 1: 751mV; (10°C)	Cooler Threshold Default: 751mV (1)
0	VCOLD	1	Y	Y	R/W	0: 982mV; (2°C) 1: 1049mV; (0°C)	Cold Threshold Default: 1049mV (1)

REG 0CH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	COOL_VSET	0	Y	Y	R/W	0: No Action 1: VBATT_REG-100mV	Default: No Action (0)
6	WARM_VSET	0	Y	Y	R/W	0: No Action 1: VBATT_REG-100mV	Default: No Action (0)
5	WARM_ISET[1]	0	Y	Y	R/W	00: no action 01: 50% of ICHG 10: 25% of ICHG 11: 20% of ICHG	Warm Action Default: 01
4	WARM_ISET[0]	1	Y	Y	R/W		
3	COOL_ISET[1]	0	Y	Y	R/W	00: no action 01: 50% of ICHG 10: 25% of ICHG 11: 20% of ICHG	Cool Action Default: 01
2	COOL_ISET[0]	1	Y	Y	R/W		
1	COOLER_ISET[1]	0	Y	Y	R/W	00: no action 01: 50% of ICHG 10: 25% of ICHG 11: 20% of ICHG	Cooler Action Default: 01
0	COOLER_ISET[0]	1	Y	Y	R/W		

REG 0DH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	0	NA	NA	R		
6	Reserved	0	NA	NA	R		
5	Reserved	0	NA	NA	R		
4	Reserved	0	NA	NA	R		
3	IDSCHG[3]	1	Y	Y	R/W	1600mA	BATT to SYS Discharge Current Limit Offset: 200mA Range: 400mA-3.2A Valid Range: 0001 - 1111 Default: 2000mA(1001)
2	IDSCHG[2]	0	Y	Y	R/W	800mA	
1	IDSCHG[1]	0	Y	Y	R/W	400mA	
0	IDSCHG[0]	1	Y	Y	R/W	200mA	

REG 0EH (8)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	SYSOVP_EN	0	NA	NA	R	0: Disable 1: Enable	Default: 0 (Disable)
6	Reserved	0	NA	NA	R		
5	SHIP_METH	0	NA	NA	R	0: by software 1: by hardware	Default: by software (0)
4	ADDR[1]	0	NA	NA	R	00: 08H 01: 0AH 10: 0CH 11: 0EH	Default: 00 (08H)
3	ADDR[0]	0	NA	NA	R		
2	LP FUNC	0	NA	NA	R	0: available 1: not available	Low power function Default: 0
1	Reserved	0	NA	NA	R		
0	Reserved	0	NA	NA	R		

Note:
8) This register is for OTP only and open to customers.

OTP MAP

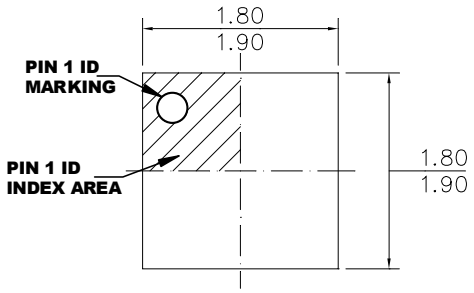
#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	N/A				CEB	N/A		
0x02	ICC: **8mA-456mA / 2mA** step							
0x03	IPRE: **1mA-31mA/2mA step**				ITERM: **1mA-31mA/2mA step**			
0x04	VBATT_REG: **3.6V-4.545V / 15mV** step						N/A	
0x05	N/A	WATCHDOG		N/A				
0x07	N/A				VSYS_REG: 4.2V-4.95V /50mV step			
0x0A	N/A					tEXSM_DGL		EN_NTC
0x0B	VHOT[1]	VHOT[0]	N/A		VCOOL[1]	VCOOL[0]	N/A	
0x0E	SYSOVP_EN	N/A	SHIP_METH	ADDR[1]	ADDR[0]	LP FUNC	N/A	N/A

OTP DEFAULT

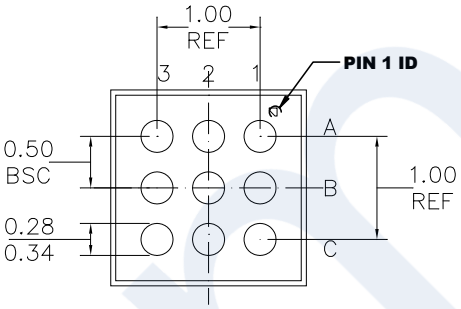
OTP Items	Default
CEB	Disable
ICC	128mA
IPRE	3mA
ITERM	3mA
VBATT_REG	4.2V
WATCHDOG	40s
VSYS_REG	4.65V
tEXSM_DGL	80ms
EN_NTC	Disable
Vhot	146mV
Vcool	751mV
ADDR	08H
LP FUNC	Available
SYSOVP_EN	Disable
SHIP_METH	By software

PACKAGE INFORMATION

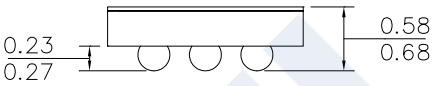
WLCSP (1.85mmx1.85mm)



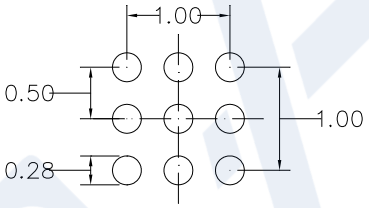
TOP VIEW



BOTTOM VIEW



SIDE VIEW

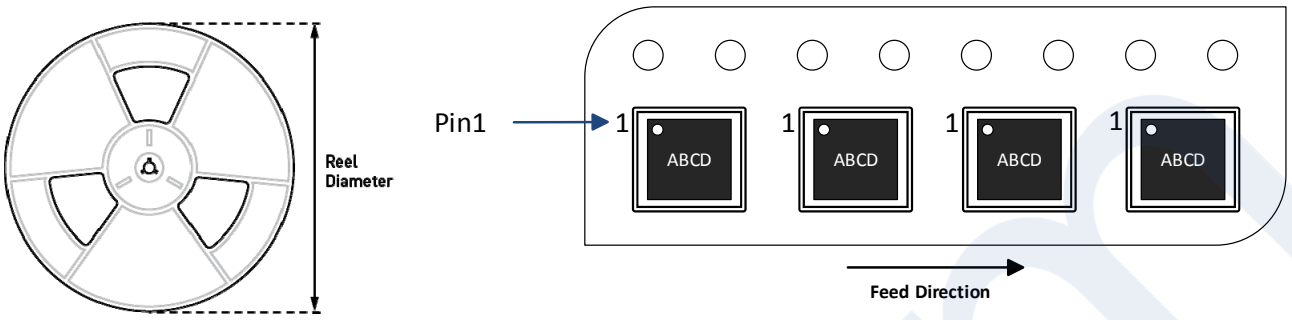


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantiy/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2710GC-xxxx-Z	WLCSP (1.85mmx1.85mm)	3000	N/A	N/A	7 in.	8 mm	4 mm