kinetic technologies™

KTS1800

6.5A$_{RMS}$ VBUS I$_{SINK}$ or I$_{SOURCE}$ Load Switch for 48V EPR Systems

Features

- 3V to 55V Operating Voltage Range
- 59V$_{DC}$ Abs. Max. Rating at VBUS and VSYS
- 6.5A$_{RMS}$ Continuous Current Rating
- 25mΩ typ. On-Resistance from VBUS to VSYS
- 55V, 90ns Over-Voltage Protection (OVP)
  - 4V to 55V External Resistor Programmable
- Transient Voltage Suppression (TVS) at VBUS
  - 48V$_{DC}$ ±130V Surge Protection (IEC61000-4-5)
  - ±30kV ESD Contact Discharge (IEC61000-4-2)
  - ±30kV ESD Air-Gap Discharge (IEC61000-4-2)
- Soft-Start (SS) Limits Inrush Current
- Short-Circuit Protection (SCP) during & after SS
- 21A, 500ns Over-Current Protection (OCP)
- Current-Limit Protection (CLP) in I$_{SOURCE}$ Mode
  - Resistor Adjustable from 0.6 to 5.5A
- "Ideal Diode" Reverse-Current Protection (RCP)
  - V$_F$ = 20mV and 30µs Fast Recovery
  - Diode Direction aligns per I$_{SINK}$ vs. I$_{SOURCE}$ Mode
- Over-Temperature Protection (OTP)
- 3.3V POK Safe LDO
- VBUS Active Discharge Circuit
- FON Logic Input for Fast Role Swap (FRS)
- A/B/C Suffix Versions for EN1/2 I$_{SINK}$ or I$_{SOURCE}$ Logic
- $\overline{FLT}$ Output Flag & Hiccup Auto-Retry after Faults
- -40°C to 85°C Operating Temperature Range
- 63-bump WLCSP 4.81 x 3.79mm (0.5mm pitch)

Brief Description

The KTS1800 is a USB VBUS safety management load switch for up to 312W I$_{SINK}$ or 240W I$_{SOURCE}$ in 48V EPR systems. The operating range is 3V to 55V with input/output withstand up to 59V$_{DC}$. Ultra-fast over-voltage protection (OVP) is internally set to 55V, but optionally adjusted via external resistors. Low on-resistance minimizes heat and voltage droop. Reverse-current protection (RCP) in both sink/source acts as a 20mV "ideal diode" with fast recovery.

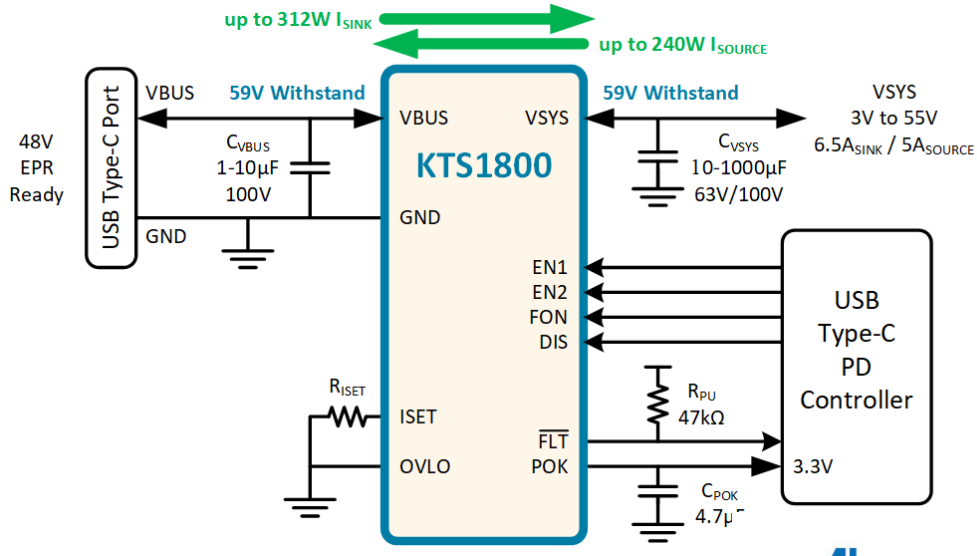
Additional safety management includes short-circuit protection (SCP) during and after soft-start, ultra-fast over-current protection (OCP), programmable current-limit protection (CLP), over-temperature protection (OTP), and an integrated transient voltage suppressor (TVS) for IEC industry standard ±30kV ESD and ±130V surge ratings. Safe POK LDO and VBUS active-discharge circuits are also integrated.

The KTS1800 is packaged in advanced, fully "green" compliant, 4.81mm x 3.79mm, 63-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Workstation & Gaming Notebooks/PCs
- Charger-per-Port Systems
- Monitors, Docking Stations, Conferencing Systems
- Tools, E-Bikes, Battery Power Stations, etc.

Typical Application



KTS1800A Truth Table

EN1	EN2	SWITCH	POK
0	0	OFF	3.3V
0	1	SINK	3.3V
1	0	SOURCE	3.3V
1	1	SHDN	SHDN

Ordering Information

Part Number	Marking[1]	EN1/EN2 Options (see Table 1)	Operating Temperature	Package
KTS1800AENAB-TB	UPYWZNAABB	Default Option	-40°C to +85°C	WLCSP-63
KTS1800BENAB-TB[2]	UQYWZNAABB	Alternative 1	-40°C to +85°C	WLCSP-63
KTS1800CENAB-TB[2]	URYWZNAABB	Alternative 2	-40°C to +85°C	WLCSP-63

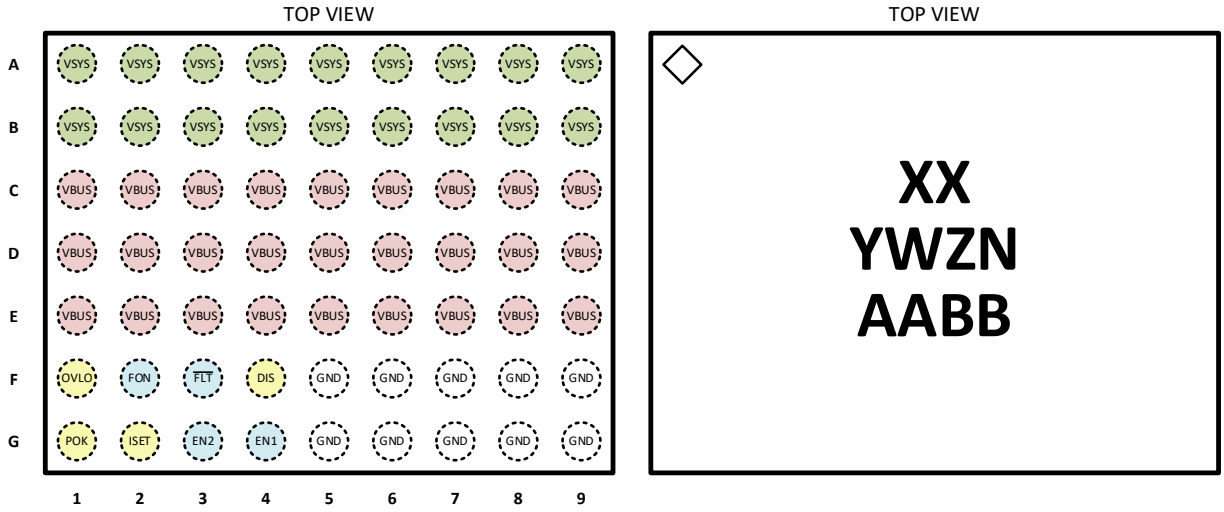
Table 1. EN1/EN2 Mode-Control Options

EN1	EN2	KTS1800A	KTS1800B	KTS1800C
0	0	Switch Off POK LDO On[3]	Switch Off POK LDO On[3]	I_{SINK} Mode POK LDO On
0	1	I_{SINK} Mode POK LDO On	Shutdown	I_{SOURCE} Mode POK LDO On
1	0	I_{SOURCE} Mode POK LDO On	I_{SINK} Mode POK LDO On	Switch Off POK LDO On[3]
1	1	Shutdown	I_{SOURCE} Mode POK LDO On	Shutdown

1. UP, UQ, UR = Device Code, YW = Date Code, ZN = Assembly Code, AABB = Serial Number.
2. Future device; contact an authorized Kinetic Technologies representative for availability.
3. POK LDO On only if VBUS voltage is present and above UVLO.

Pinout Diagram

WLCSP97-63



63-bump 4.810mm x 3.790mm x 0.555mm
WLCSP Package, 0.500mm pitch

Top Mark
XX = Device Code
YW = Date Code, ZN = Assembly Code
AABB = Serial Number

Pin Descriptions

Pin #	Name	Function
A1 to B9	VSYS	Power Switch System-Side Connection – connect to switching regulator output, battery charger input, and/or switching regulator input for systems without rechargeable batteries.
C1 to E9	VBUS	Power Switch VBUS Port-Side Connection – connect to VBUS on USB port.
F1	OVLO	External OVLO Adjustment – connect to GND to use the internally fixed OVP threshold. Connect an external resistive voltage divider from VBUS (or VSYS) to OVLO to GND to set an adjustable OVLO threshold.
F2	FON	Fast Turn-On Logic Input – active-high with internal 1MΩ pull down; enables fast turn-on of I_{SOURCE} mode for USB Fast Role Swap (FRS).
F3	$\overline{FLT}$	Fault Logic Output – active-low, open-drain flag indicates any fault condition(s).
F4	DIS	V_{BUS} Active Discharge Input – active-high analog input with internal 1MΩ pull down; connected to gate of internal V_{BUS} active discharge FET.
G1	POK	Power-OK “Safe LDO” Regulator Output – regulated output voltage when V_{BUS} is present and LDO is enabled via EN1 and EN2. Leave Hi-Z (unconnected) if unused.
G2	ISET	Current Limit Setting – adjusts the I_{SOURCE} mode current limit using a resistor from ISET to GND.
G3	EN2	Enable 2 Logic Input – with EN1, controls operating modes; see Table 1.
G4	EN1	Enable 1 Logic Input – with EN2, controls operating modes; see Table 1.
F5 to F9 G5 to G9	GND	Ground

Absolute Maximum Ratings[4]

Symbol	Description	Value	Units
V_{BUS}	VBUS to GND (continuous)	-0.3 to 59	V
	VBUS to GND (during IEC61000-4-5 surge event)[5]	-5 to 72	
V_{SYS}	VSYS to GND	-0.3 to 59	V
$V_{BUS-SYS}$	VBUS to VSYS	-59 to 59	V
V_{OVLO}	OVLO to GND	-0.3 to V_{BUS}	V
V_{EN1}, V_{EN2}, V_{ISET}, V_{DIS}, V_{POK}, V_{FON}, $V_{\overline{FLT}}$	EN1, EN2, ISET, DIS, POK, FON, $\overline{FLT}$ to GND	-0.3 to 6	V
I_{SW}	Maximum Switch Current (continuous)	6.5	A
	Peak Switch Current (I_{SINK} mode, 5ms, OCP and Pd limited)	21	
T_J	Die Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[6]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (VBUS)	±30	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (VBUS)	±30	kV
V_{SURGE}	IEC61000-4-5 Surge (V_{BUS} = 0V_{DC}+Surge, C_{VBUS} = 0µF)	±180	V
	IEC61000-4-5 Surge (V_{BUS} = 5V_{DC}+Surge, C_{VBUS} = 10µF, R_{LOAD} = 100Ω)	±230	V
	IEC61000-4-5 Surge (V_{BUS} = 48V_{DC}+Surge, C_{VBUS} = 10µF, R_{LOAD} = 400Ω)	±130	V

Thermal Capabilities[7]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	36	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$ ($T_J \leq 125°C$)	2.78	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-27.8	mW/°C

4. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
5. The internal active TVS FET and main NMOSFET on the VBUS pin can withstand up to +72V peak pulse voltage (duration is less than 100µs) based on process standard. The internal active TVS can clamp VBUS voltage up to less than 70V during IEC61000-4-5 +190V surge event.
6. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
7. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions[8]

Symbol	Description	Value	Units
V_{BUS}, V_{SYS}	VBUS, VSYS Operating Voltage	3 to 55	V
V_{EN1}, V_{EN2}, V_{DIS}, V_{FON}, V_{OVLO}	EN1, EN2, DIS, FON, OVLO Input Voltage	0 to 5.5	V
$V_{\overline{FLT}}$	Fault Flag Output Pull-Up Voltage	0 to 5.5	V
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Junction Operating Temperature Range	-40 to 125	°C
C_{VBUS}	VBUS External Local Capacitance	1 to 10	µF
		100	V
C_{VSYS}	VSYS External Capacitance	10 to 2240	µF
		63 or 100	V

Electrical Characteristics[9]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{BUS}	VBUS Supply Operating Voltage Range	I_{SINK} mode	3		55	V
V_{SYS}	VSYS Supply Operating Voltage Range	I_{SOURCE} mode	3		55	V
V_{UVLO}	Under-Voltage Lockout	V_{BUS} rising threshold, I_{SINK} mode		2.5	2.9	V
		V_{SYS} rising threshold, I_{SOURCE} mode		2.75	2.9	V
		Hysteresis, I_{SINK} or I_{SOURCE} mode		150		mV
I_Q	No-Load Supply Current	V_{BUS} = 5V, I_{SINK} mode		420		µA
		V_{BUS} = 48V, I_{SINK} mode		550		
		V_{SYS} = 5V, I_{SOURCE} mode		480		
		V_{SYS} = 48V, I_{SOURCE} mode		610		
I_{Q_POK}	No-Load POK LDO Supply Current	V_{BUS} = 5V, Switch Off, POK On		250		µA
		V_{BUS} = 48V, Switch Off, POK On		310		
I_{SHDN}	Shutdown Supply Current	V_{BUS} = 5V, shutdown mode		3		µA
		V_{BUS} = 48V, shutdown mode		8		
		V_{SYS} = 5V, shutdown mode		3		
		V_{SYS} = 48V, shutdown mode		8		
I_{Q_RCP}	Output Supply Current in RCP	V_{BUS} = 0V, V_{SYS} = 5V, I_{SINK} mode		275		µA
		V_{SYS} = 0V, V_{BUS} = 5V, I_{SOURCE} mode		250		

(continued next page)

8. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

9. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

Electrical Characteristics (continued)[10]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

TVS Surge Clamp Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{TVS_WRK}	Clamp Working Voltage	Positive Working Voltage			59	V
		Negative Working Voltage[11]	-0.3			
V_{TVS_CLMP}	Clamp Breakdown Voltage	I_{IN} = 10mA	63	65	68	V
		I_{IN} = -10mA[11]	-2	-0.6	-0.3	
V_{TVS_SRG}	Clamp Surge Voltage[11]	+180V surge (V_{BUS} = 0V_{DC}+Surge, C_{VBUS} = 0µF)		66	70	V
		-180V surge (V_{BUS} = 0V_{DC}+Surge, C_{VBUS} = 0µF)		-1.8	-4	
V_{TVS_SRG}	Clamp Surge Voltage[11]	+130V surge (V_{BUS} = 48V_{DC}+Surge, C_{VBUS} = 10µF, R_{LOAD} = 400Ω)		67	70	V
		-130V surge (V_{BUS} = 48V_{DC}+Surge, C_{VBUS} = 10µF, R_{LOAD} = 400Ω)		-1.6	-4	

Logic Pin Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High (EN1, EN2, FON)		1.2			V
V_{IL}	Input Logic Low (EN1, EN2, FON)				0.4	V
R_{I_PD}	Input Logic Pull-Down (FON)			1		MΩ
I_{I_LK}	Input Logic Leakage (EN1, EN2)	V_I = 5V	-1		1	µA
V_{OL}	Output Logic Low ($\overline{FLT}$)	I_{O_SINK} = 1mA		0.01	0.2	V
I_{O_LK}	Output Logic High-Z Leakage ($\overline{FLT}$)	V_O = 5V	-1		1	µA

V_{BUS} Active Discharge (DIS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{AD}	Active Discharge Resistance (from V_{BUS}=5V to GND)	V_{DIS} = 3V	0.11	0.22	0.32	kΩ
		V_{DIS} = 2V		0.25		
		V_{DIS} = 1.5V		0.4		
		V_{DIS} = 1.4V		0.5		
		V_{DIS} = 1.2V, T_A = 0°C to +85°C		1.2	3.0	
V_{IH_DIS}	DIS Input High Voltage	R_{AD} < 3kΩ, T_A = 0°C to +85°C	1.2			V
V_{IL_DIS}	DIS Input Low Voltage[11]	R_{AD} is high-Z			0.5	V
R_{DIS_PD}	DIS Internal Pull-Down Resistor			1		MΩ
t_{VBUS_DIS}	V_{BUS} Active Discharge Time[12]	V_{BUS} = 5V, V_{DIS} = 3V, C_{VBUS} = 10µF		6		ms

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10. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
11. Guaranteed by design, characterization and statistical process control methods; not production tested.
12. t_{VBUS_DIS} is the time for VBUS to fall from 5V (vSafe5V) to below 0.8V (vSafe0V). The USB specification for tSafe0V is 0ms to 650ms, so in theory, this can discharge up to 1000µF in case of excessive source bulk capacitance.

Electrical Characteristics (continued)[13]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

POK Safe LDO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POK}	POK LDO Output Voltage	V_{BUS} = 5V, I_{POK} = 0 to 100mA, T_A = +25°C	3.0	3.3	3.6	V
		V_{BUS} = 48V, I_{POK} = 0 to 10mA, T_A = +25°C[11]	3.0	3.3	3.6	V
V_{UVLO_POK}	POK Under-Voltage Lockout[14]	V_{BUS} rising threshold, I_{SINK} or I_{SOURCE} or Off+POKon modes		2.7	2.9	V
		Hysteresis		150		mV
I_{LK_POK}	POK-to-GND Leakage Current[11]	V_{POK} = 5V, V_{BUS} = 0V, T_A = +25°C		0.01	1	µA
I_{POK_VBUS}	POK-to-VBUS Leakage Current at VBUS	V_{POK} = 5V, V_{BUS} = 0V, dark		-0.001		µA

Power Switch Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON}	Switch On-Resistance in I_{SINK} mode T_A = +25°C	V_{BUS} = 5V, I_{SYS} = 0.8A[15]		28		mΩ
		V_{BUS} = 5V, I_{SYS} > 1.2A		25		
		V_{BUS} = 48V, I_{SYS} > 1.2A	15	25	35	
	Switch On-Resistance in I_{SOURCE} mode T_A = +25°C	V_{SYS} = 5V, I_{BUS} = 0.8A[15]		28		
		V_{SYS} = 5V, I_{BUS} > 1.2A		25		
		V_{SYS} = 48V, I_{BUS} > 1.2A	15	25	35	
I_{BUS_OFF}	Switch Off-Leakage at VBUS[11] (tested in shutdown mode)	V_{BUS} = 0V, V_{SYS} = 3V to 55V, dark	-10	-0.001	10	µA
I_{SYS_OFF}	Switch Off-Leakage at VSYS[11] (tested in shutdown mode)	V_{SYS} = 0V, V_{BUS} = 3V to 55V, dark	-10	-0.001	10	µA

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13. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
14. POK Safe LDO is enabled when VBUS is above V_{UVLO_POK}, depending upon EN1 and EN2 status, regardless of OVP, OVLO, and OCP.
15. When tested at 1A or less, the RON is limited by the V_{RCP} specification.

Electrical Characteristics (continued)[16]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Soft-Start (SS) Specifications (see Figure 1)

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DON}	Turn-On Delay Time[17]	Off-to-enabled, FON = 0 or 1[11]		30	50	µs
		I_{SINK}-to-I_{SOURCE}, FON = 1		3		
		I_{SOURCE}-to-I_{SINK}, FON = 1		3		
t_{DEB}	Soft-Start Debounce Time[17]	I_{SINK} or I_{SOURCE}, FON = 0	10	16	25	ms
		I_{SINK}, FON = 1		0		
		I_{SOURCE}, FON = 1		0		
V_{SR_SS}	Soft-Start Voltage Ramp Slew-Rate	I_{SINK} or I_{SOURCE}, FON = 0		1		V/ms
		I_{SINK}, FON = 1, C_{VSYS} = 40µF		50		
		I_{SOURCE}, FON = 1, C_{VBUS} = 10µF		80		
t_R	Soft-Start Voltage Ramp Time	I_{SINK}, FON = 0, V_{SYS} = 10% to 90%		0.8*V_{BUS}		ms
I_{LIM_SS}	Soft-Start Current Limit (for SCP)	I_{SINK}, V_{BUS} = 5V, FON = 0		2		A
		I_{SOURCE}, V_{SYS} = 5V, FON = 0, I_{CLP} > 2A		2		
		I_{SOURCE}, V_{SYS} = 5V, FON = 0, I_{CLP} < 2A, V_{BUS} < 1.8V		2		
		I_{SOURCE}, V_{SYS} = 5V, FON = 0, I_{CLP} < 2A, V_{BUS} > 1.8V		I_{CLP}		
		I_{SINK}, V_{BUS} = 48V, V_{SYS} = 0V, FON = 0		1		
		I_{SOURCE}, V_{SYS} = 48V, V_{BUS} = 0V, FON = 0, I_{CLP} > 1A		1		
t_{LIM_SS}	Soft-Start Current Limit Done Time[18]	I_{SINK} or I_{SOURCE}, FON = 0		2		ms
t_{DOFF}	Turn-Off Delay Time[11, 19]		0	2	10	µs

Fault Flag ($\overline{FLT}$) Recovery and Hiccup Timer Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{HICCUP}	Fault Condition Hiccup Retry Time[20]	after any fault		64		ms
$t_{\overline{FLT}}$	Fault Flag Release Delay after t_{LIM_SS}	after t_{LIM_SS}, FON = 0		4		ms
		after t_{LIM_SS}, FON = 1		2		

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16. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
17. t_{DON} + t_{DEB} is time from enabled logic and valid supply voltage until the output voltage begins to rise.
18. t_{ILIM_SS} is time from when the output voltage exceeds the input voltage minus 0.9V until the soft-start current limit ends.
19. t_{DOFF} is time from enable logic until the output voltage begins to fall.
20. Faults include OVP, OTP, OCP, and SCP. After the fault condition has ended, the hiccup timer triggers, followed by the soft-start sequence, and then the $\overline{FLT}$ flag is released. Other protections that are not classified as faults include RCP and CLP. These non-faults do not trigger the $\overline{FLT}$ flag and hiccup timer. RCP and CLP have fast recovery without initiating a soft-start. UVLO does trigger the $\overline{FLT}$ flag and soft-start, but without the hiccup timer.

Electrical Characteristics (continued)[21]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Over-Voltage Protection (OVP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OVP}	Internally Fixed Over-Voltage Protection	V_{BUS} rising threshold, I_{SINK} mode	53	55	57	V
		V_{SYS} rising threshold, I_{SOURCE} mode	53	55	57	
		Hysteresis		2.3		V
t_{OVP}	OVP Response Time[22]	V_{BUS} > V_{OVP}, C_{VSYS} = 0µF, R_L = 100Ω		90		ns
		V_{SYS} > V_{OVP}, C_{VBUS} = 0µF, R_L = 100Ω		90		
t_{OVP_REC}	OVP Recovery Time[23]		$t_{HICCUP}+t_{DON}+t_{DEB}+t_R$			ms
V_{OVLO}	Externally Adjustable Over-Voltage Lockout	V_{OVLO} enable threshold	76	96	116	mV
		V_{OVLO} rising OVP threshold	1.14	1.195	1.25	V
		Hysteresis		25		mV
t_{OVLO}	OVLO Response Time[24]	R_L = 100Ω, C_{VSYS} = 0µF		300		ns
t_{OVLO_REC}	OVLO Recovery Time		$t_{HICCUP}+t_{DON}+t_{DEB}+t_R$			ms

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{OTP}	IC Junction Over-Temperature Protection	T_J rising threshold		150		°C
		Hysteresis		20		°C
t_{OTP_REC}	OTP Recovery Time		$t_{HICCUP}+t_{DON}+t_{DEB}+t_R$			ms

Over-Current Protection (OCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{OCP}	OCP Current Threshold after t_{LIM_SS}[25]	I_{SINK} mode	15	21		A
		I_{SOURCE} mode	15	21		
t_{OCP}	OCP Response Time[26]			500		ns
t_{OCP_REC}	OCP Recovery Time		$t_{HICCUP}+t_{DON}+t_{DEB}+t_R$			ms

Reverse-Current Protection (RCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RCP}	RCP Droop Regulation Voltage	I_{SINK}, V_{RCP} = V_{BUS}–V_{SYS}, I_{SYS} = 100mA	10	20	30	mV
		I_{SOURCE}, V_{RCP} = V_{SYS}–V_{BUS}, I_{BUS} = 100mA	10	20	30	
t_{RCP_REC}	RCP Fast Recovery Time[27]			30		µs

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21. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
22. t_{OVP} is time from when the input voltage > V_{OVP} until the output voltage stops rising.
23. t_{OVP_REC} is time from when the input voltage < V_{OVP} until the output voltage reaches 90% of the input voltage.
24. t_{OVLO} is time from when V_{OVLO} rises above its OVP threshold until output voltage stops rising.
25. Guaranteed by ATE test mode.
26. t_{OCP} is time from when the switch current > I_{OCP} until switch turns off.
27. t_{RCP_REC} is time from when the output voltage falls 140mV below the input voltage until switch turns back on. Before measuring, first raise the output voltage significantly above the input voltage.

Electrical Characteristics (continued)[28]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Current-Limit Protection (CLP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{LIM_CLP}	Current-Limit Regulation (after t_{LIM_SS})	I_{SINK} mode		n/a		A
		I_{SOURCE} mode, R_{ISET} = 43.2kΩ[11]	0.5	0.6	0.7	
		I_{SOURCE} mode, R_{ISET} = 20.0kΩ	1.10	1.32	1.54	
		I_{SOURCE} mode, R_{ISET} = 15.4kΩ[11]	1.5	1.7	1.9	
		I_{SOURCE} mode, R_{ISET} = 7.87kΩ[11]	3.0	3.3	3.6	
		I_{SOURCE} mode, R_{ISET} = 4.75kΩ[11]	5.0	5.5	6.0	

Short-Circuit Protection (SCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{HSCP_SS}	Hard Short-Circuit Protection SS Voltage (at 3ms into SS ramp)	I_{SINK} mode, V_{SYS} not rising		1.3		V
		I_{SOURCE} mode, V_{BUS} not rising		1.3		
V_{SSCP}	Soft Short-Circuit Protection Voltage (after t_{LIM_SS})	I_{SINK} mode, V_{SYS} falling		0.5*V_{BUS}		V
		I_{SINK} mode, low V_{BUS}, V_{SYS} falling		1.8		
		I_{SOURCE} mode, V_{BUS} falling		0.5*V_{SYS}		
		I_{SOURCE} mode, low V_{SYS}, V_{BUS} falling		1.8		
I_{HSCP}	Hard Short-Circuit Protection Current			I_{OCP}		A
t_{SCP_REC}	SCP Recovery Time		$t_{HICCUP}+t_{DON}+t_{DEB}+t_R$			ms

Timing Diagrams

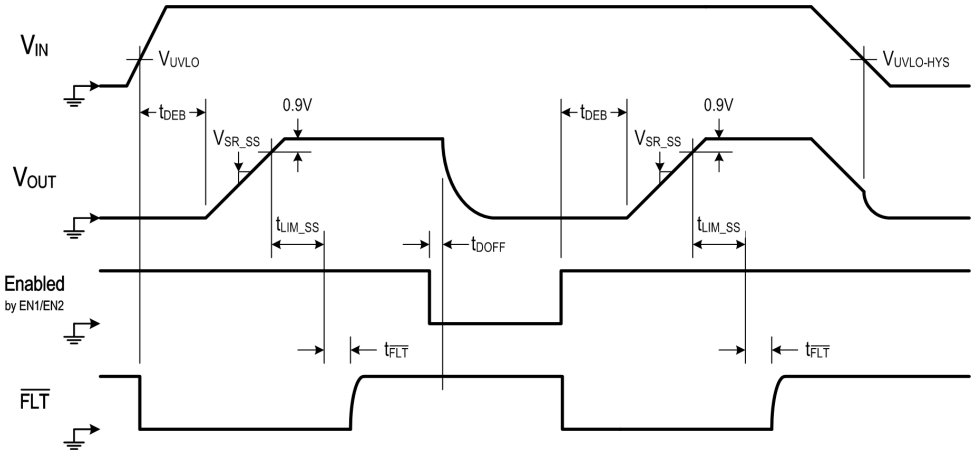


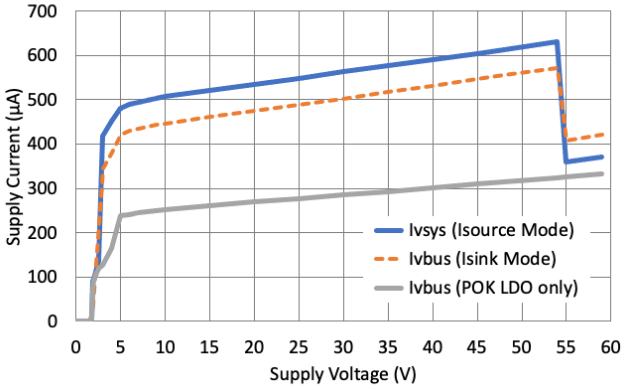
Figure 1. UVLO, Soft-Start and Turn-Off Timing Diagram

28. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

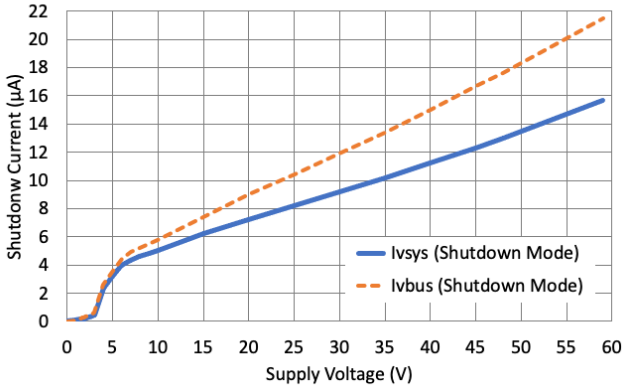
Typical Characteristics

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

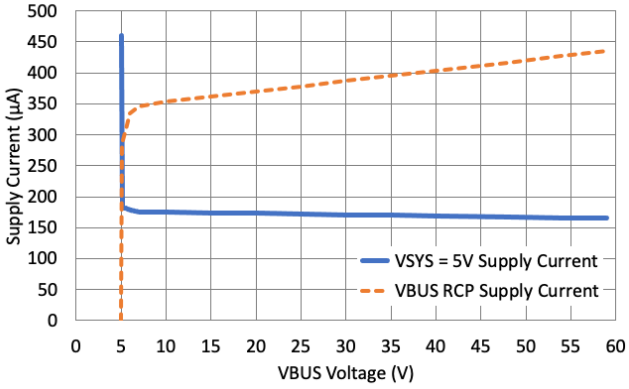
Supply Current vs. Supply Voltage
(enabled, no load)



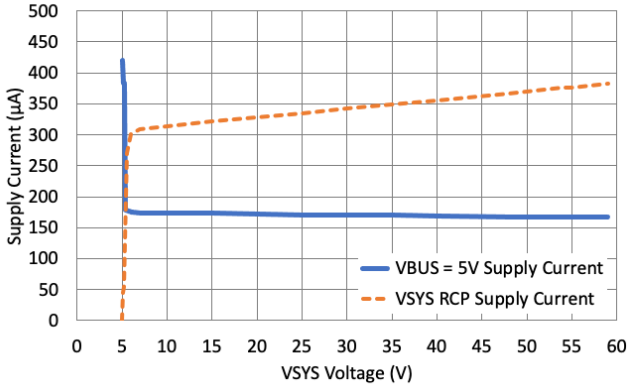
Shutdown Supply Current vs. Supply Voltage
(Shutdown Mode)



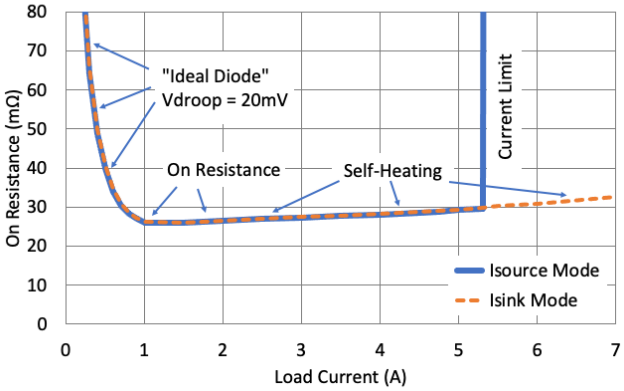
RCP Supply Current in Isource Mode
(V_{SYS} = 5V, enabled, V_{BUS} lifted)



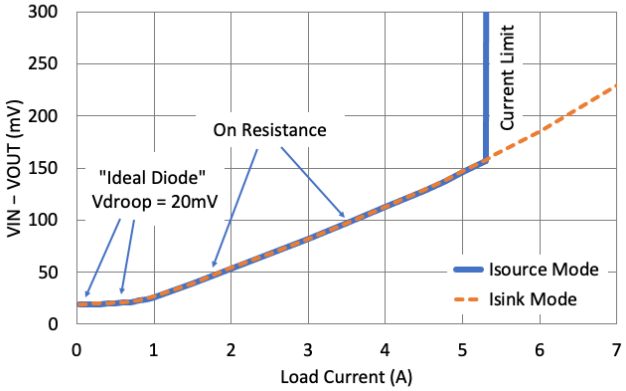
RCP Supply Current in Isink Mode
(V_{BUS} = 5V, enabled, V_{SYS} lifted)



On Resistance vs. Load Current
(V_{IN} ≥ 5V, enabled, R_{ISET} = 4.75kΩ)



"Ideal Diode" Vdroop vs. Load Current
(V_{IN} ≥ 5V, enabled, R_{ISET} = 4.75kΩ)

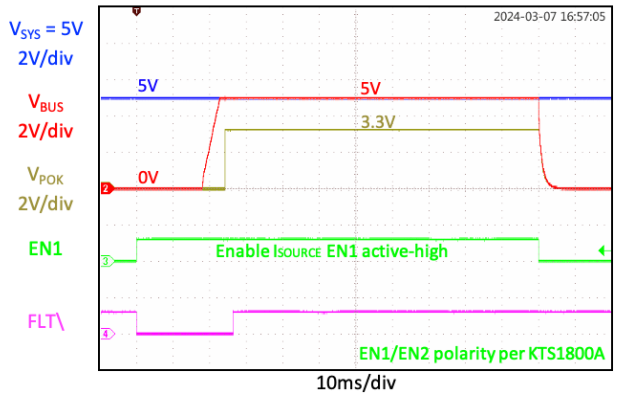


(continued next page)

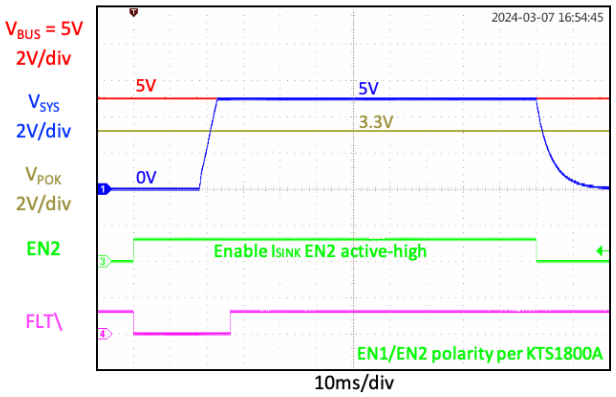
Typical Characteristics

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

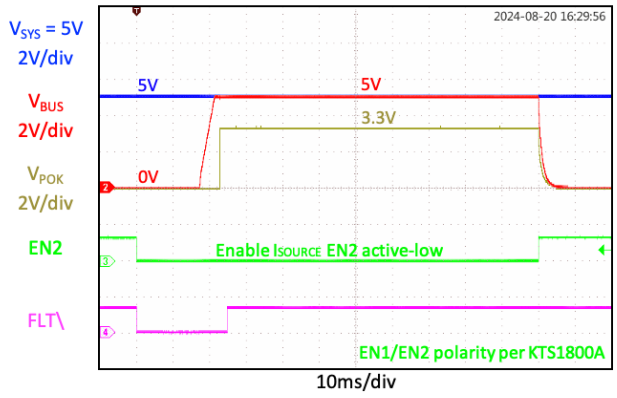
Active-High Enable/Soft-Start in ISOURCE Mode
(VSYS = 5V, EN2 = 0, RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



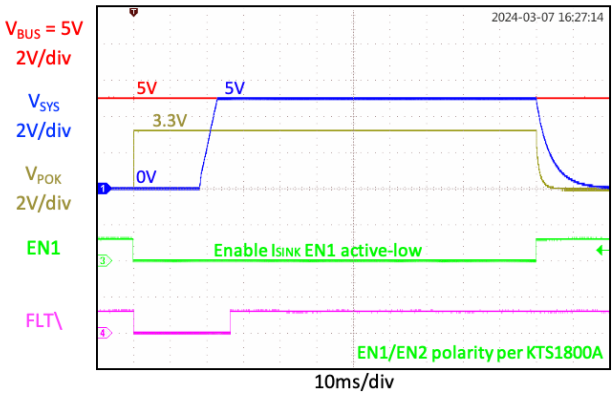
Active-High Enable/Soft-Start in ISINK Mode
(VBUS = 5V, EN1 = 0, RLOAD_VSYS = 100Ω, RLOAD_POK = 300Ω)



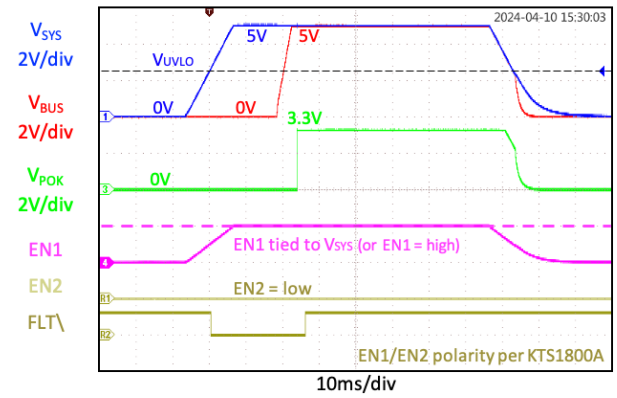
Active-Low Enable/Soft-Start in ISOURCE Mode
(VSYS = 5V, EN1 = 1, RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



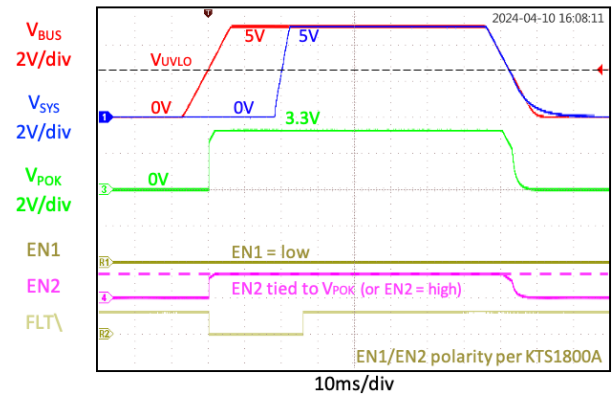
Active-Low Enable/Soft-Start in ISINK Mode
(VBUS = 5V, EN2 = 1, RLOAD_VSYS = 100Ω, RLOAD_POK = 300Ω)



Rising VSYS Enable/Soft-Start in ISOURCE Mode
(RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



Rising VBUS Enable/Soft-Start in ISINK Mode
(RLOAD_VSYS = 100Ω, RLOAD_POK = 300Ω)

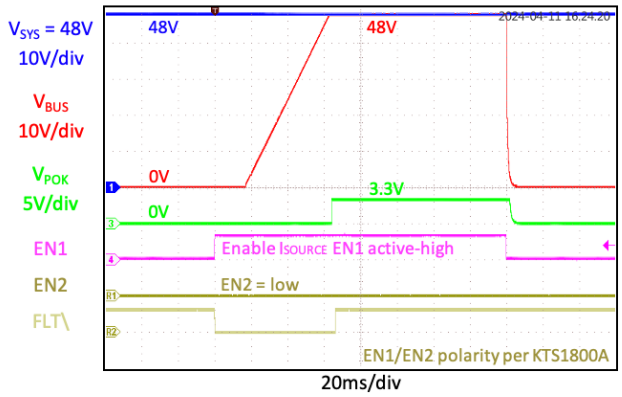


(continued next page)

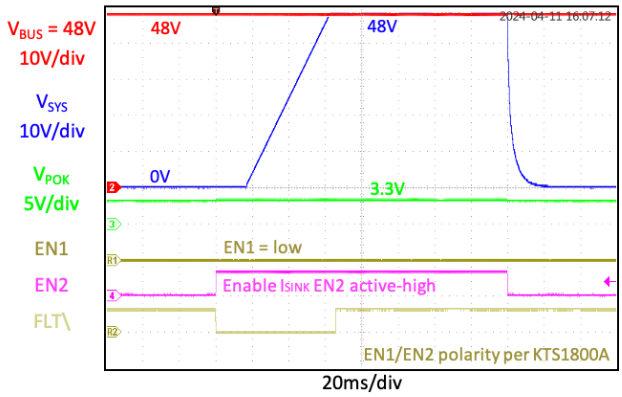
Typical Characteristics (continued)

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

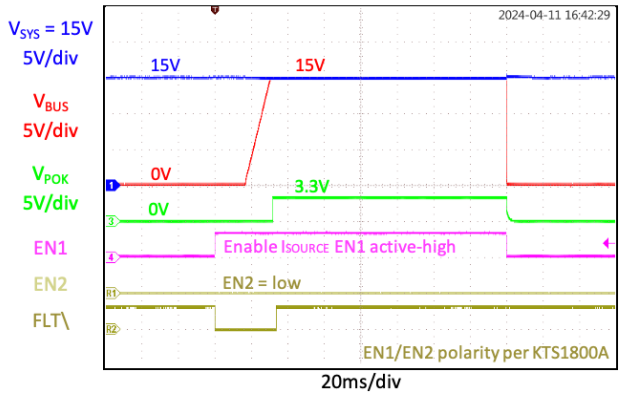
48V Enable/Soft-Start in ISOURCE Mode
(VSYS = 48V, RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



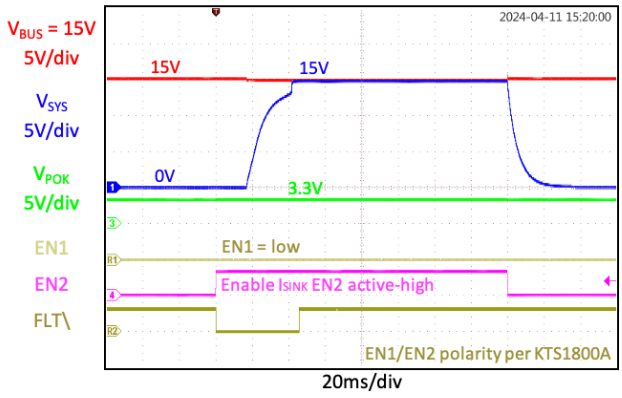
48V Enable/Soft-Start in ISINK Mode
(VBUS = 48V, RLOAD_VSYS = 100Ω, RLOAD_POK = 300Ω)



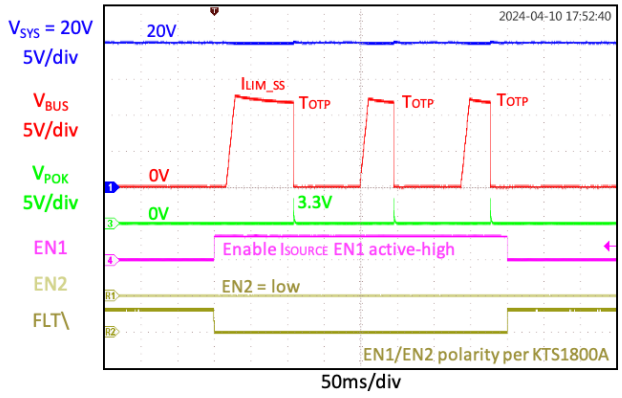
Heavy Load Enable/Soft-Start in ISOURCE Mode
(VSYS = 15V, CVBUS = 10µF, RLOAD_VBUS = 6Ω)



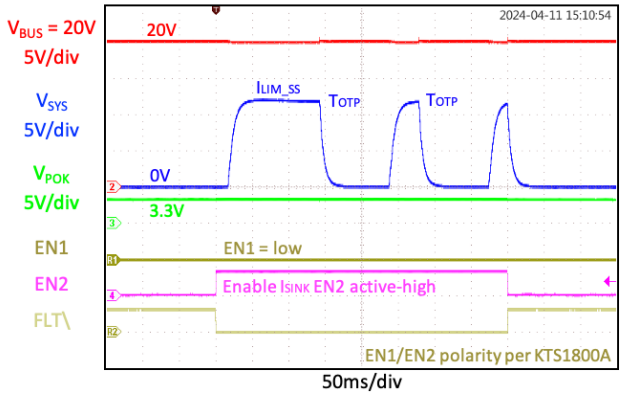
Heavy Load Enable/Soft-Start in ISINK Mode
(VBUS = 15V, CVSYS = 1000µF, RLOAD_VSYS = 6Ω)



Over-Load Enable/Auto-Retry in ISOURCE Mode
(VSYS = 20V, CVBUS = 10µF, RLOAD_VBUS = 6Ω)



Over-Load Enable/Auto-Retry in ISINK Mode
(VBUS = 20V, CVSYS = 1000µF, RLOAD_VSYS = 6Ω)

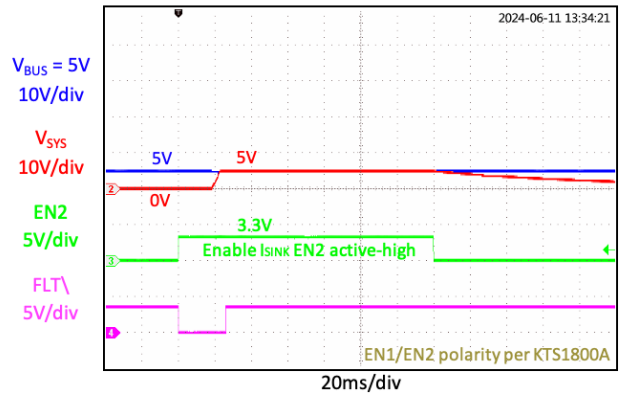


(continued next page)

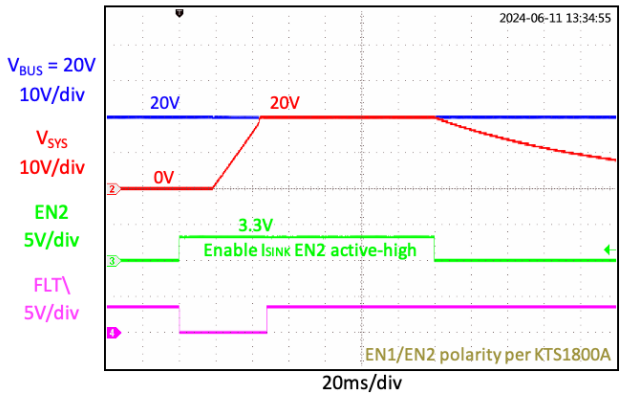
Typical Characteristics (continued)

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

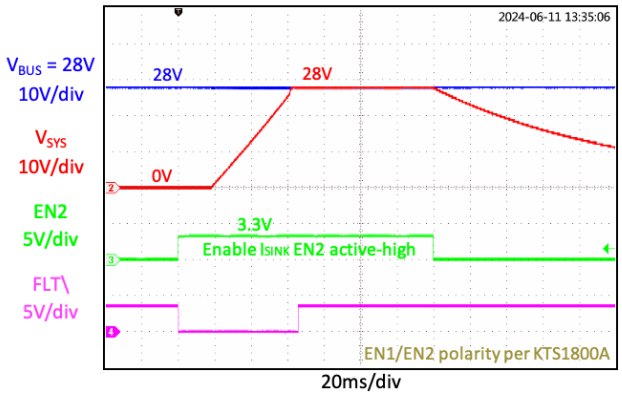
Soft-Start into Big Cap at V_{BUS} = 5V
(C_{BUS} = 10µF, C_{VSYS} = 2200µF + 4x10µF, R_{LOAD_VSYS} = 50Ω)



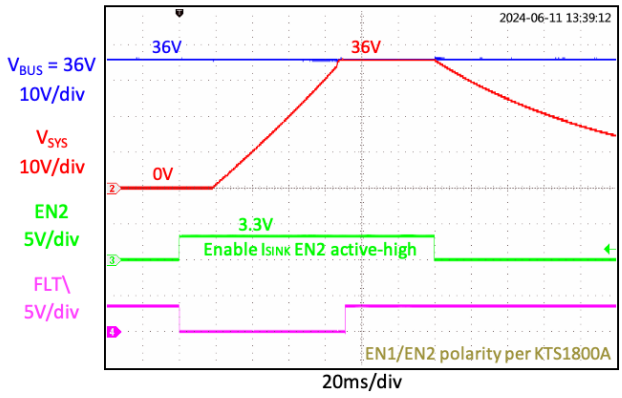
Soft-Start into Big Cap at V_{BUS} = 20V
(C_{BUS} = 10µF, C_{VSYS} = 2200µF + 4x10µF, R_{LOAD_VSYS} = 50Ω)



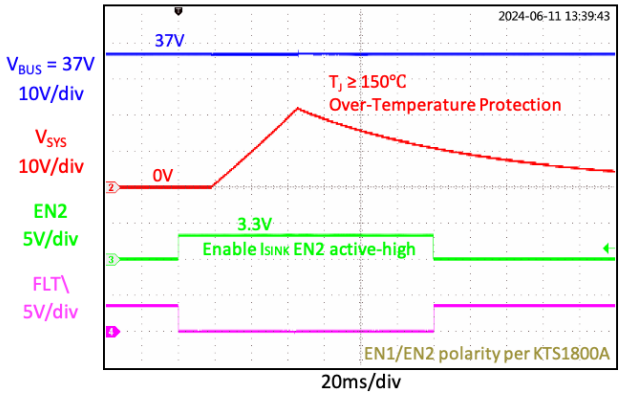
Soft-Start into Big Cap at V_{BUS} = 28V
(C_{BUS} = 10µF, C_{VSYS} = 2200µF + 4x10µF, R_{LOAD_VSYS} = 50Ω)



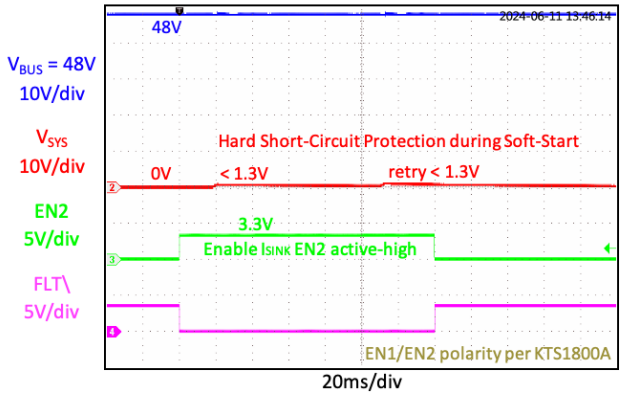
Soft-Start into Big Cap at V_{BUS} = 36V
(C_{BUS} = 10µF, C_{VSYS} = 2200µF + 4x10µF, R_{LOAD_VSYS} = 50Ω)



Soft-Start (OTP) into Big Cap at V_{BUS} = 37V
(C_{BUS} = 10µF, C_{VSYS} = 2200µF + 4x10µF, R_{LOAD_VSYS} = 50Ω)



Soft-Start (SCP) into Big Cap at V_{BUS} = 48V
(C_{BUS} = 10µF, C_{VSYS} = 2200µF + 4x10µF, R_{LOAD_VSYS} = 50Ω)

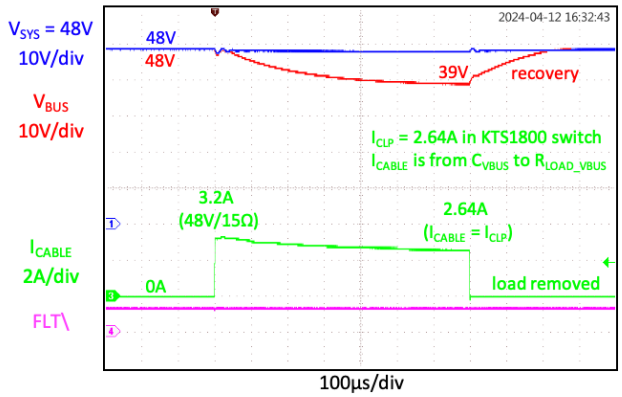


(continued next page)

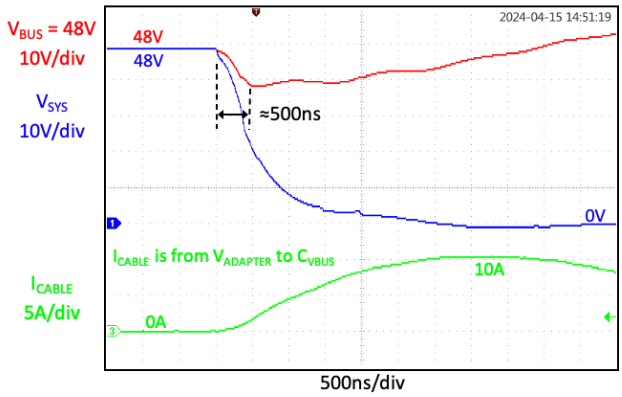
Typical Characteristics (continued)

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

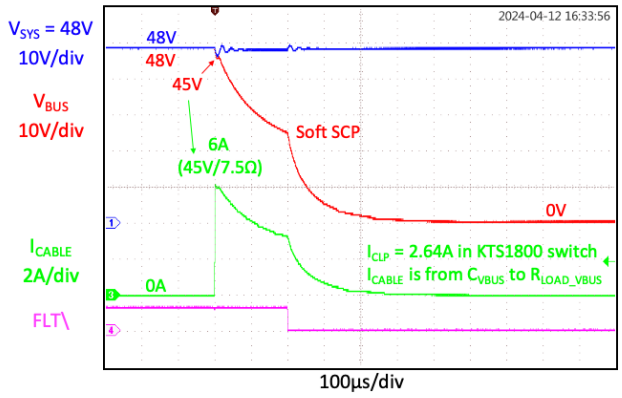
CLP Response with Recovery in ISOURCE Mode
(VSYS = 48V, RISET = 10kΩ, RLOAD_VBUS = 15Ω pulse)



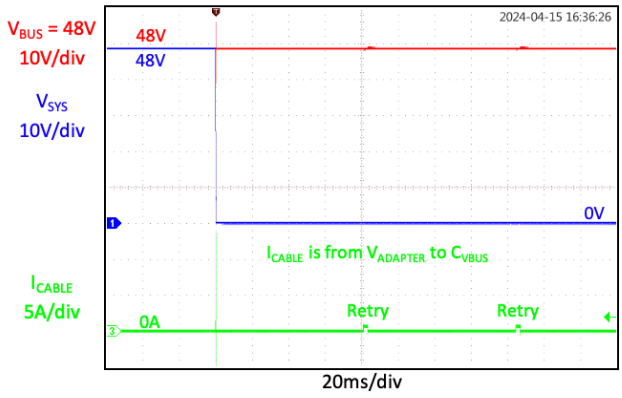
OCP/SCP Response in ISINK Mode
(VBUS = 48V, VSYS = sudden short circuit)



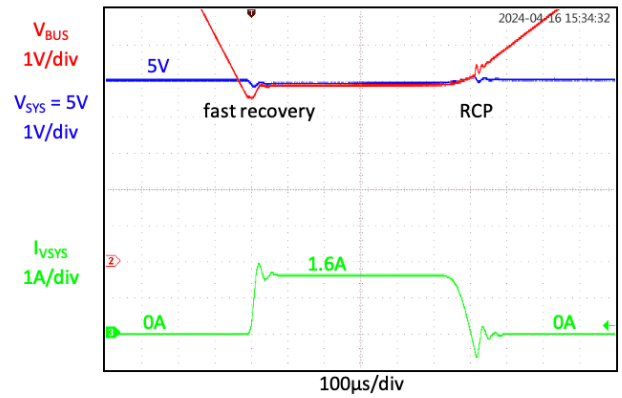
CLP & SCP Response in ISOURCE Mode
(VSYS = 48V, RISET = 10kΩ, RLOAD_VBUS = 7.5Ω pulse)



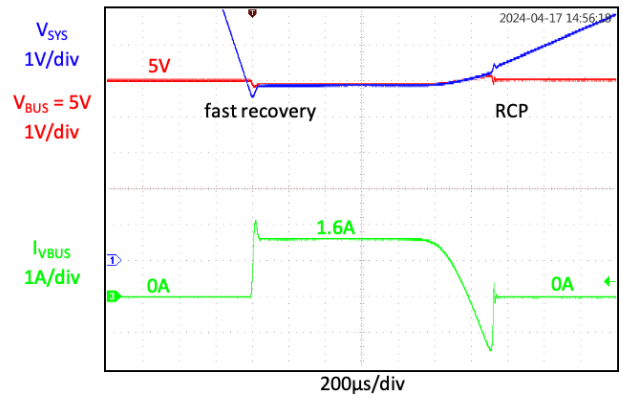
SCP & Auto-Retry Response in ISINK Mode
(VBUS = 48V, VSYS = sudden short circuit)



"Ideal Diode" RCP Response in ISOURCE Mode
(VSYS = 5V, VBUS = 9V → high-Z → 9V, RLOAD_VBUS = 3Ω)



"Ideal Diode" RCP Response in ISINK Mode
(VBUS = 5V, VSYS = 9V → high-Z → 9V, RLOAD_VSYS = 3Ω)



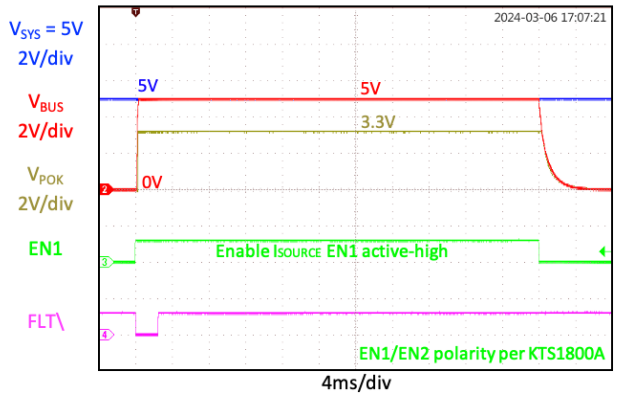
(continued next page)

Typical Characteristics (continued)

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

Fast-On Start-Up in ISOURCE Mode

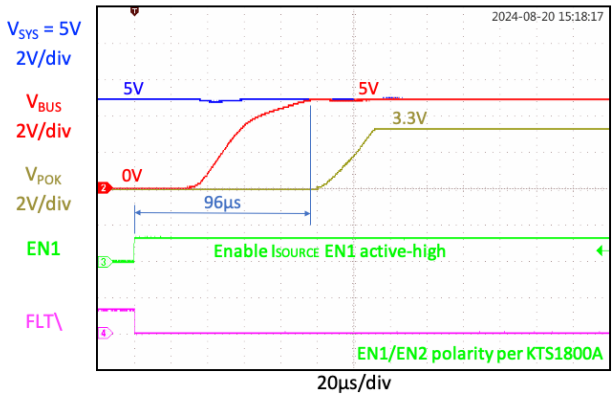
(VSYS = 5V, FON = 1, RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



4ms/div

Fast-On Start-Up in ISOURCE Mode (Zoom In)

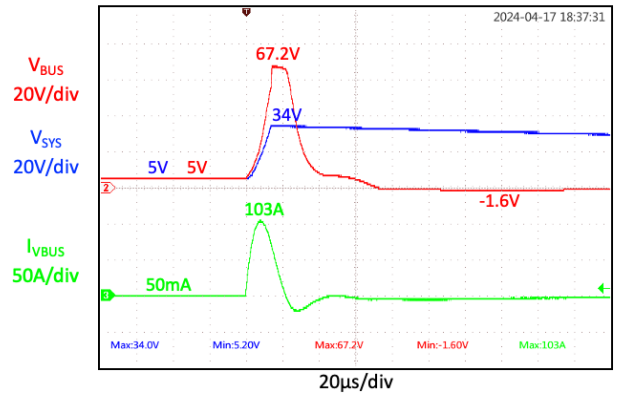
(VSYS = 5V, FON = 1, RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



20µs/div

Surge Transient Response

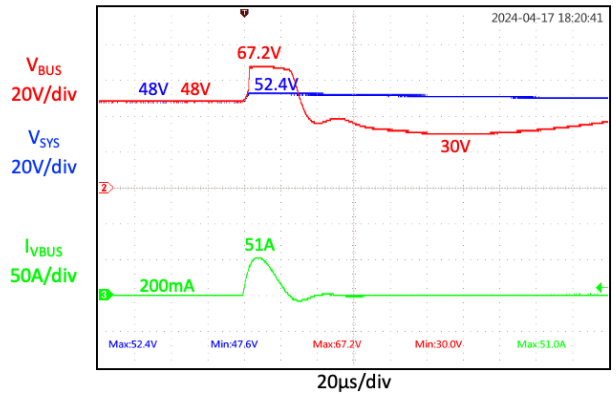
(VBUS = 5VDC + 230VSURGE, CVBUS = 10µF, ISINK Mode)



20µs/div

Surge Transient Response

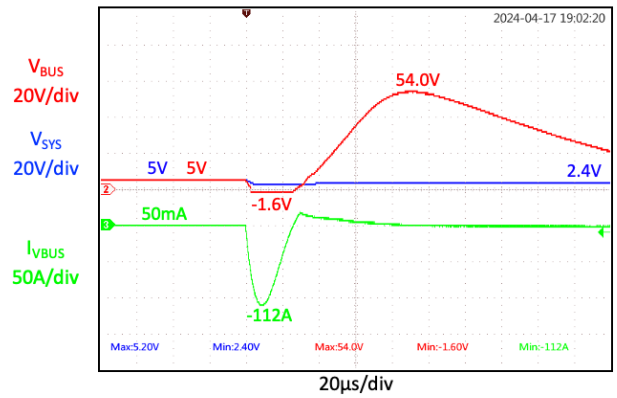
(VBUS = 48VDC + 130VSURGE, CVBUS = 10µF, ISINK Mode)



20µs/div

Surge Transient Response

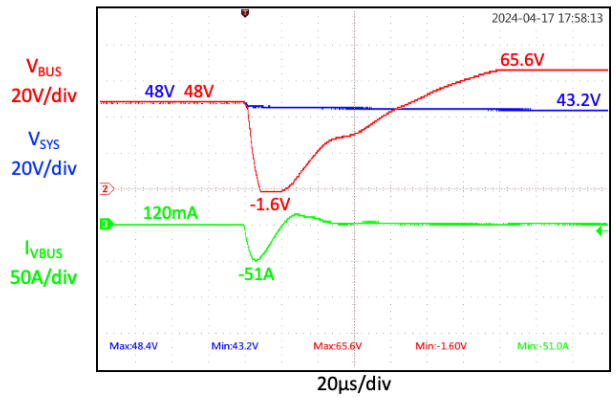
(VBUS = 5VDC - 230VSURGE, CVBUS = 10µF, ISINK Mode)



20µs/div

Surge Transient Response

(VBUS = 48VDC - 130VSURGE, CVBUS = 10µF, ISINK Mode)



20µs/div

Functional Block Diagram

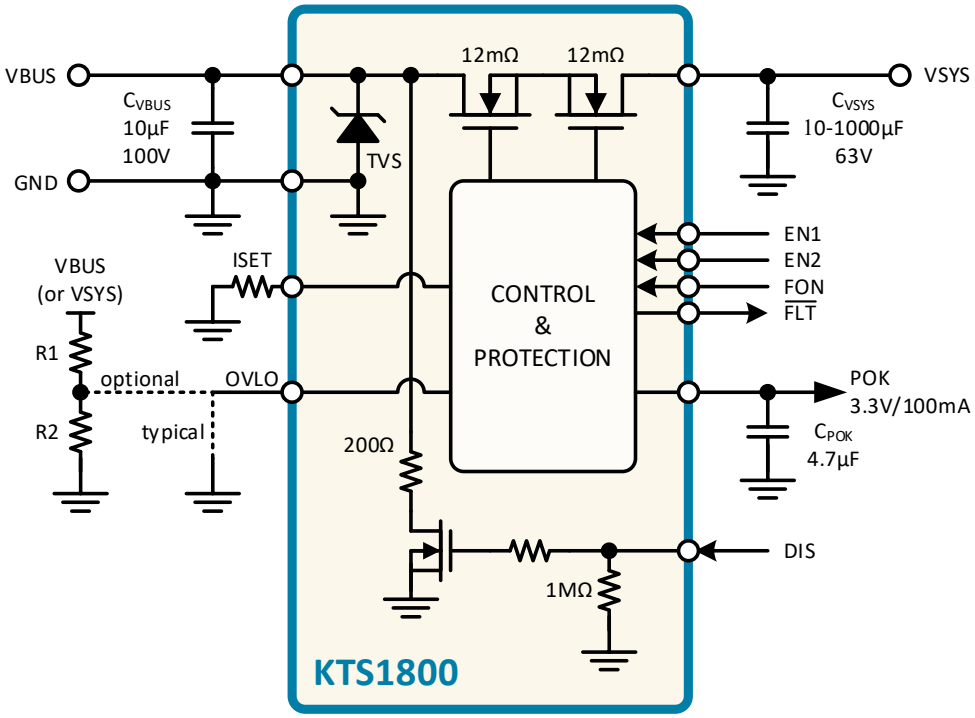


Figure 2. Functional Block Diagram

Functional Description

The KTS1800 is a slew-rate controlled, 25mΩ (typ) low resistance MOSFET bi-directional switch intended to be inserted between a power source and a load to isolate and protect against abnormal voltage and current conditions. Via the enable logic control pins, the operating mode is configured as a dedicated current sink, a dedicated current source, or changed dynamically as a sink or source for dual-role power. Featuring slew-rate controlled soft-start and soft-start current limit to prevent excessive large inrush current, the KTS1800 also features several additional protection functions. These include input under-voltage lockout protection, input over-voltage protection, output short-circuit protection, over-current protection, over-temperature protection, and input transient voltage suppression for ±130V surge (even at $48V_{DC}$ bias) and ±30kV ESD protections. The KTS1800 switch also acts as a reversible "ideal diode" with V_F = 20mV and 30µs fast recovery to ensure current flows in only the intended sink or source direction.

Operating from a wide input voltage range of 3V to 55V, the KTS1800 is optimized for USB Type-C Power Delivery (PD) current-sink or current-source applications up to 48V extended power range (EPR) that require essential protection and enhanced system reliability. While in the OFF state, the KTS1800 blocks voltages of up to 59V on the VBUS and VSYS pins and prevents current flow. While in the ON state, the KTS1800 withstands voltages of up to 59V on the VBUS and VSYS pins, passes valid input voltages and current through its switch, and blocks reverse current flow per its sink or source mode. Due to the ideal-diode behavior, two or more KTS1800 parts can be used in parallel to support systems that benefit from "diode-OR" power routing.

EN1 and EN2 Inputs

The KTS1800 has EN1 and EN2 logic inputs which control the Shutdown vs. I_{SINK} vs. I_{SOURCE} modes and the POK LDO on/off status. See Table 1 in the *Ordering Information* section for various EN1/EN2 mode-control options.

Under-Voltage Lockout (UVLO)

When $V_{BUS} < V_{UVLO}$ in I_{SINK} mode or $V_{SYS} < V_{UVLO}$ in I_{SOURCE} mode, the power switch is disabled. Once V_{BUS} or V_{SYS}, respectively, exceeds V_{UVLO}, the power switch is controlled by the enable pins and fault detection circuits.

Soft-Start (SS)

The internal soft-start function allows the KTS1800 to charge a total output capacitance of 1000µF to 5V without excessive in-rush current. Soft-start controls the output voltage ramp slew-rate at 1V/ms. Use the below formula to calculate the current required to charge a combination of load current and output capacitance:

$$I_{IN\_SS} = I_{LOAD} + C_{OUT}(1V/ms)$$

Note that in addition to the soft-start voltage ramp, a simultaneous soft-start current limit of 2A prevents excessive heat when entering into an output short-circuit or a large total output capacitance conditions. This current limit turns off 2ms after the output voltage ramp exceeds the input voltage minus 0.9V, regardless of whether the output voltage is following the slew rate or limited by the soft-start current limit. After an additional 2ms delay, the $\overline{FLT}$ flag releases to indicate a power good condition. See the *Heavy Load Soft-Start Response* in the *Typical Characteristics* section.

Over-Voltage Protection (OVP)

Once enabled, if the input voltage exceeds the V_{OVP} threshold, the power switch is disabled due to an OVP fault. Once the input voltage drops below V_{OVP} (and no other fault is detected and the device is still logically enabled via EN1/EN2), the power switch is re-enabled after the hiccup timer, turn-on delay, soft-start debounce and soft-start ramp time.

The OVLO pin is used to adjust the over-voltage threshold externally. The default internal over-voltage threshold is 55V when the OVLO pin is tied to GND. Biasing the OVLO pin with a resistive voltage divider adjusts the over voltage threshold from 4V to 55V as in the below formula:

$$V_{OVP} = V_{OVLO}\left(1 + \frac{R1}{R2}\right)$$

where V_{OVLO} = 1.195V. Connect R1 from VBUS to OVLO. Connect R2 from OVLO to ground. For dedicated current source applications, it is optional to connect the resistive voltage divider to VBUS or VSYS, depending upon the needs of the application.

Over-Current Protection (OCP)

The KTS1800 includes output over-current protection (OCP) that protects the IC from damage when an excessive over-current or short-circuit event suddenly appears. The OCP threshold is purposely high above the rated current for the KTS1800 such that system load-pulses do not easily trigger OCP. The OCP circuit disables the power switch, so the current becomes zero. After an OCP event (and no other fault is detected and the device is still logically enabled via EN1/EN2), the power switch is re-enabled after the hiccup timer, turn-on delay, soft-start debounce and soft-start ramp time.

Short-Circuit Protection (SCP)

The KTS1800 includes output short-circuit protection (SCP). In virtually all conditions, the KTS1800 remains undamaged during continuous SCP events.

If an SCP event occurs while the KTS1800 is already enabled and working, OCP is the first line of defense and responds very quickly. In this case, the current from the input capacitor through the switch to the output increases very rapidly as soon as the output voltage begins to collapse. The OCP threshold is purposely high above the rated current for the KTS1800 such that system load-pulses do not easily trigger OCP.

In addition, if the output voltage collapses to less than 50% without reaching OCP, such as during a CLP overload or soft short-circuit event, an SCP fault is triggered, causing the switch to open and triggering a hiccup and auto-retry sequence.

In case of auto-retry (after the hiccup timer) or simply starting into a pre-existing SCP condition, the KTS1800 furthermore includes SCP detection during soft-start if the output voltage is not ramping up. SCP checks if the output voltage has risen to more than 1.3V at 3ms into the soft-start ramp. If not, the KTS1800 terminates soft-start, turns off the switch, and will auto-retry after the hiccup timer. The $\overline{FLT}$ flag remains low until a successful soft-start is completed.

"Ideal Diode" Reverse-Current Protection (RCP)

The KTS1800 offers reverse-current protection regardless of the enable logic level. In shutdown mode, all current flow is blocked. In both I_{SINK} and I_{SOURCE} modes, the RCP acts as a voltage droop regulator. The ideal diode changes orientation along with the I_{SINK} vs. I_{SOURCE} operating mode to ensure that current flows only in the intended direction.

When the voltage on the output is higher than the input voltage minus 20mV, the RCP circuit reduces the MOSFET gate drive to try and maintain the regulated 20mV droop, thereby acting as an "ideal diode" with Vf = 20mV. See Figure 3.

This control method blocks all DC reverse current. During dynamic conditions, the RCP transient loop-bandwidth may allow some reverse current for a short duration until it engages and turns off the switch. However, during recovery, RCP includes a 30µs fast recovery circuit whenever the output falls again below the input voltage. The dynamic performance of RCP is shown in oscilloscope images in the *Typical Characteristics* section. Note that RCP is not defined as a fault condition and has fast recovery without initiating the hiccup and auto-retry sequence.

The RCP circuit makes it possible to connect two or more USB charging ports to a single charger input in a "diode-OR" configuration with autonomous reverse-current blocking. And during Fast Role Swap events, it allows the I_{SOURCE} mode to be enabled even before VBUS falls below 5V, and then RCP fast-recovery catches VBUS quickly to provide uninterrupted power to the load. See the oscilloscope images in the *Typical Characteristics* section.

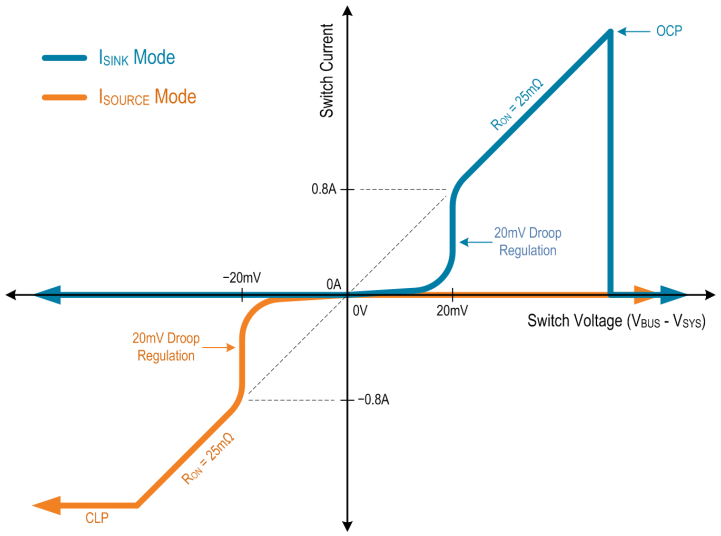


Figure 3. "Ideal Diode" Reverse-Current Protection V-I Curve

Current-Limit Protection (CLP)

Program the I_{SOURCE} mode current limit using an external resistor, R_{ISET}, connected from the ISET pin to ground. See Figure 4 and the *CLP Specifications* section of the *Electrical Characteristics* table. Calculate the value of R_{ISET} using the following formula:

$$R_{ISET} = \frac{26400}{I_{LIM\_CLP}}$$

Whenever the switch current reaches the programmed current limit, the current-limit regulation loop takes control and reduces the gate drive to limit the switch current. During CLP, the switch acts as a constant current source, and the output voltage reduces depending on the load current. Once the load current reduces below the current limit, the output voltage recovers. Note that CLP is not defined as a fault condition and has fast recovery without initiating the hiccup and auto-retry sequence.

However, if the output voltage collapses to less than 50% of the input voltage during a CLP event, an SCP fault is detected, causing the switch to open and triggering a hiccup and auto-retry sequence. Additionally, during CLP events, power dissipation increases, which may trigger an OTP fault if the die becomes too hot. When the chip temperature cools, the device recovers and turns back on via the hiccup and auto-retry sequence.

For added protection, the current-limit regulation loop includes a modest amount of thermal foldback and V_{IN} – V_{OUT} foldback. Both foldbacks are linear functions (as opposed to stepped). The thermal foldback can be seen in the *Typical Characteristics* section within the oscilloscope image for *Over-Load Enable/Auto-Retry in I_{SOURCE} Mode*. The V_{IN} – V_{OUT} foldback is also depicted in Figure 6 and Figure 7 on the *Soft-Start CLP = 2.0A* curve's reduction to 1.0A when V_{IN} – V_{OUT} = 55V. These foldbacks affect both the soft-start current limit and the I_{SOURCE} mode current limit.

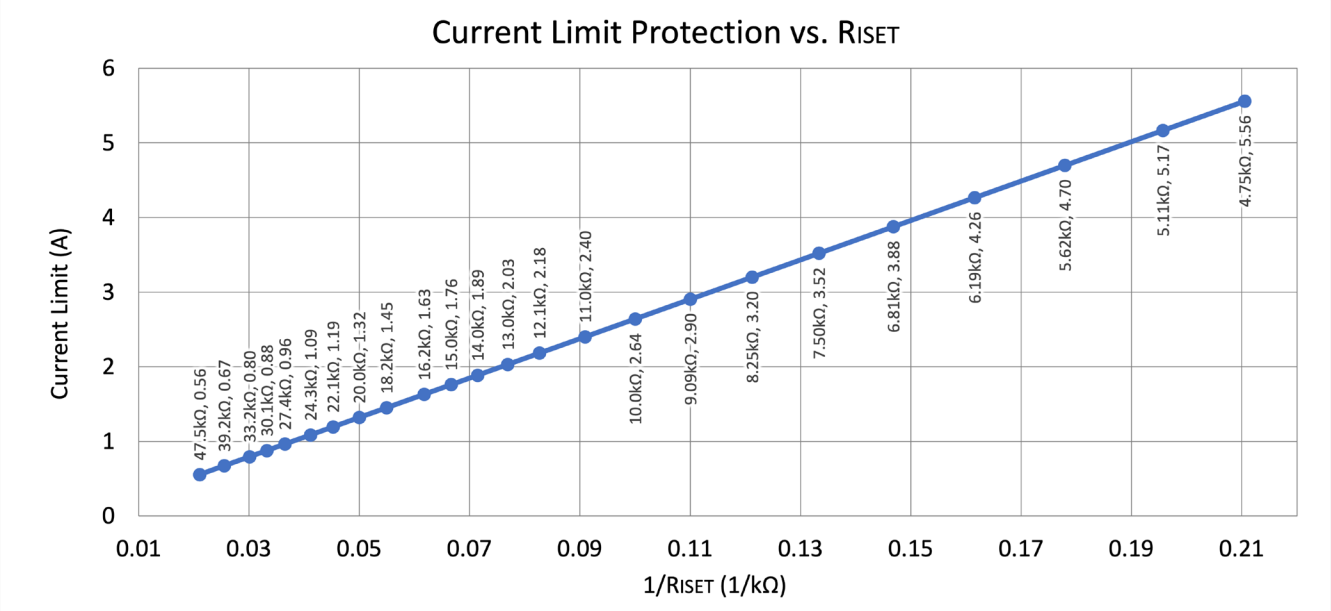


Figure 4. I_{SOURCE} Mode Current Limit Protection vs. R_{ISET} Resistance

Fast Roles Swap (FRS) via Fast Turn On (FON)

To enable USB power delivery (PD) fast role swap (FRS) mode, set the FON pin to logic 1. With FON = 1, the soft-start debounce time is skipped, and the soft-start ramp slew-rate is increased to 50V/ms typ. (for I_{SOURCE} Mode) and 80V/ms typ. (for I_{SINK} Mode). There are two possible role-swap sequences for Fast Turn On:

1. If $V_{OUT} < V_{IN}$, the switch performs a Fast Turn On, and the switch turns on within 150µs max. when V_{IN} = 5V.
2. If $V_{OUT} > V_{IN}$, the switch enters RCP mode and remains OFF. Later, as V_{OUT} falls 20mV below V_{IN}, the RCP naturally recovers. The “ideal diode” fast recovery reduces how far V_{OUT} falls below V_{IN}.

Over-Temperature Protection (OTP)

When device junction temperature exceeds 150°C, the OTP circuit disables the power switch. Once the device junction temperature decreases below 130°C (and no other fault is detected and the device is still logically enabled via EN1/EN2), the power switch is re-enabled after the hiccup timer, turn-on delay, soft-start debounce and soft-start ramp time.

Transient Voltage Suppression (TVS)

The KTS1800 integrates an active clamp transient voltage suppressor (TVS) from VBUS to GND. The integrated TVS circuit and fast OVP switch work as an optimized system to protect the KTS1800 and downstream circuits for IEC surge and ESD events. The TVS protection is always active, whether the KTS1800 is in shutdown, I_{SINK}, I_{SOURCE}, or POK only mode.

$\overline{\text{FLT}}$ Output Flag

The $\overline{\text{FLT}}$ pin indicates the fault and soft-start status. The $\overline{\text{FLT}}$ open-drain output requires an external pull-up resistor with recommended value in the 10kΩ to 200kΩ range. During fault conditions (UVLO, OVP, OCP, SCP, and OTP) and during soft-start (SS), the $\overline{\text{FLT}}$ flag is active low. When there is no fault and after soft-start is finished, the power switch is ON, then the $\overline{\text{FLT}}$ flag is high-Z and pulled up via the external resistor to indicate the power is good and there is no fault condition. CLP and RCP events are not defined as faults by the KTS1800, so the $\overline{\text{FLT}}$ flag remains high-Z during these events. Note that CLP and RCP also have fast recovery without initiating the hiccup and auto-retry sequence. Also note that during CLP over-load events where the output voltage is drooping significantly, OTP or SCP faults may trigger.

Auto-Retry with Hiccup Timer

For fault conditions that cause the switch to open, the KTS1800 automatically restarts via the hiccup timer and soft-start sequence once the fault is removed. If any fault or the same fault is detected again, the switch opens again, and auto-retry repeats. This continues until the fault is removed (normal operation) or the device is shutdown via EN1 and EN2 or input power is removed (UVLO). Note that CLP and RCP events are not defined as fault conditions and have fast recovery without initiating the auto-retry sequence.

VBUS Active Discharge (DIS)

The KTS1800 includes an active discharge circuit to pull VBUS below to vSafe0V within USB Type-C compliant discharge timing specifications. The pull-down resistance depends upon the DIS pin voltage level. See the *DIS Specifications* section of the *Electrical Characteristics* table. As shown in Figure 2, the DIS circuit operation is fully independent of the rest of the IC and does NOT depend upon chip being powered or the EN1/EN2 status.

POK Safe LDO

When VBUS is greater than 2.7V typ, the POK Safe LDO provides an “always on” power source when enabled via the EN1 and EN2 logic inputs (see Table 1), regardless of the OVP, OCP, and SCP fault states. The POK LDO output may be used as either a logic signal or to power downstream components, thereby permitting operation without an installed battery or a dead battery. The POK output is disrupted during OTP (thermal shutdown) and some IEC surge and ESD events. Like most LDOs, the POK output does not sink significant current when its output voltage is held above regulation by another power source, for example, when combining multiple power sources to power a PD controller.

The POK output sources 3.3V at up to 100mA. However, when VBUS is low (between 2.7V and 3.3V), the LDO’s output voltage is in dropout and tracks VBUS. Also, at high VBUS voltages, limit the POK load current to avoid high power dissipation (excessive heat) in the KTS1800. The POK Safe LDO power dissipation is calculated as:

$$P_{D\_POK} = (V_{BUS} - 3.3V) \times I_{LOAD\_POK}$$

As an example, with 48V_{BUS} and 10mA load at POK, the power dissipation is 447mW. The POK power dissipation adds to the power dissipation of the main VBUS-to-VSYS power switch when enabled.

Applications Information

External Component Selection

VBUS Capacitor C_{VBUS}

For most applications, connect a 1µF to 10µF ceramic capacitor as close as possible to the device from VBUS to GND to minimize the effect of parasitic trace inductance. 100V rated capacitors with X5R or better dielectric are recommended. For optimal surge and ESD performance, 10µF is preferred.

VSYS Capacitor C_{VSYS}

For most applications, connect from 10µF to 1000µF total capacitance from VSYS to GND. Typical applications use 30µF to 100µF as needed for system load-transients. At minimum, connect a 10µF ceramic capacitor as close as possible to the device to minimize the effect of parasitic trace inductance. 63V or 100V rated capacitors with X5R or better dielectric are recommended. Lower voltage ratings may be acceptable when using the OVLO pin to set a lower over-voltage protection threshold. For bulk capacitance, add ceramic, polymer or other capacitor technologies in parallel as needed to meet the needs of the application.

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents. The KTS1800 EVB is designed with similar layout as Figure 5, but it extends the fill area for the VSYS, VBUS, and GND copper planes for increased thermal performance. Due to the number of bumps on VSYS and VBUS, these two planes are especially important for heat dissipation and should not be ignored. Adding back-side and/or buried-layer fill area with thermal vias helps significantly. The WLCSP package has very low Theta-JC, which is ideal when using thermally conductive material laid over the IC, external components, and PCB. With good thermal design, applications up to 7A continuous may be supported.

The PCB layout for the KTS1800 is quite simple. Place the VSYS and VBUS capacitors near the IC. Connect the capacitor ground terminals together and to the GND pins using the top-side copper. Route the control signals on buried layers. With 0.5mm bump pitch, signal traces may be routed between bumps to reach inner bumps. Or route the inner bumps using filled, in-pad vias, as these have become more available even in low-cost PCB manufacturing. As an example, the KTS1800 EVB uses filled, in-pad vias. Depending upon the application's needs, connect any unused control pins (OVLO, FON, EN1, EN2, $\overline{FLT}$, and/or DIS) to ground. Even if unused, do not ground the POK Safe LDO output.

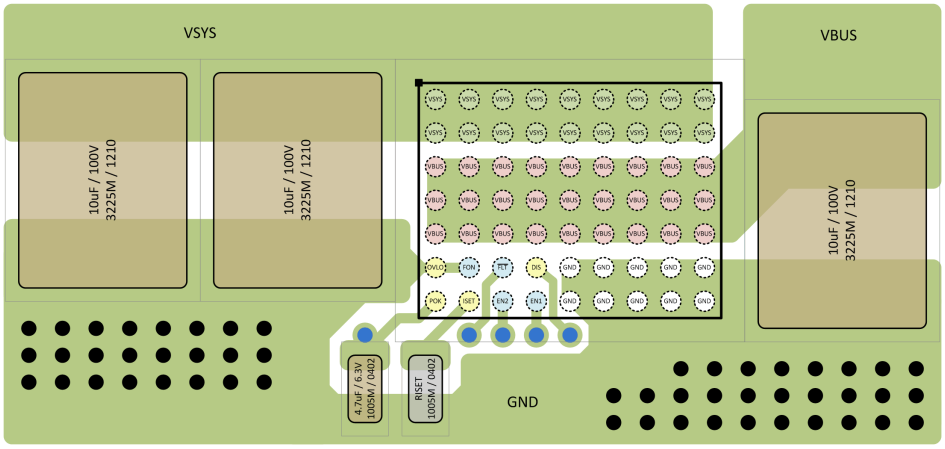


Figure 5. Recommended PCB Layout

Safe Operating Area (SOA)

See Figure 6 and Figure 7 for the SOA of the KTS1800. SOA curves are normally associated with discrete MOSFETs (which are sometimes co-package with a controller IC). In these competing systems, precautions are necessary to stay within the SOA area. However, the KTS1800 is a monolithic IC with integrated protection features to *automatically* keep its operation within the SOA area. For example, it includes over-voltage protection (OVP) and over-current protection (OCP) with very fast response times. It also includes over-temperature protection (OTP) that is measured on the same monolithic die as the integrated power MOSFETs. Additionally, soft-start is controlled with a voltage ramp and current limit protection (Soft-Start CLP) to safely soft-start even in systems with very high capacitance at the output. Furthermore, the integrated TVS and back-to-back MOSFET switch are optimized to work together as a system, including their tolerances over temperature and process corners.

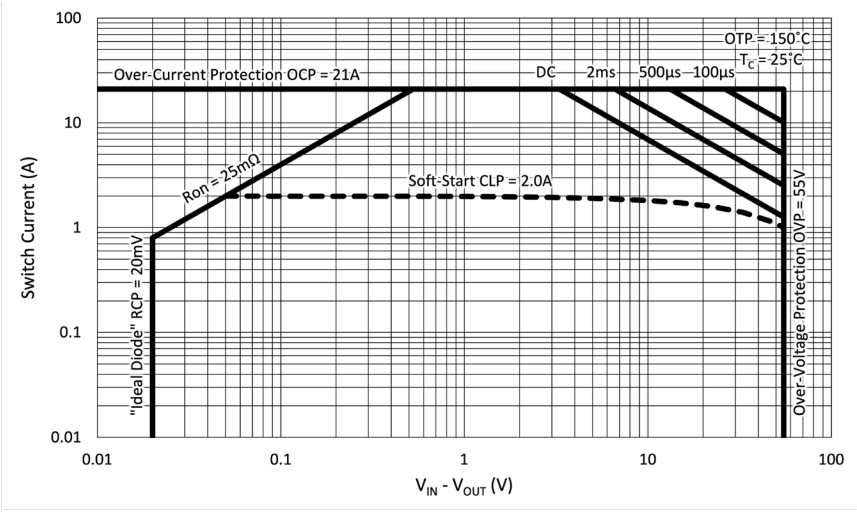


Figure 6. Safe Operating Area (SOA) for T_C = 25°C

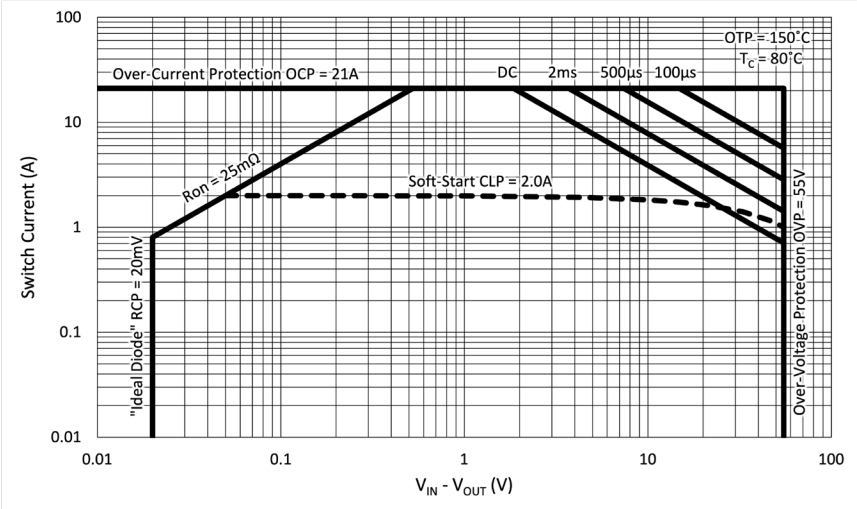
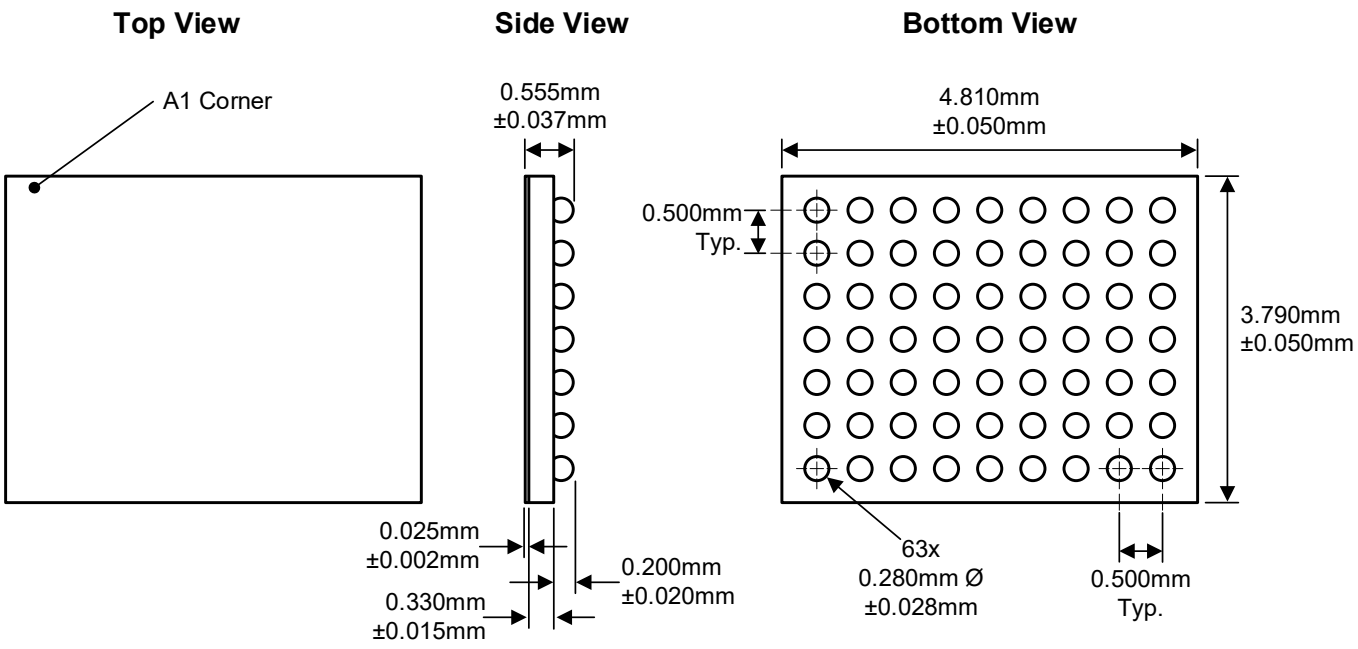


Figure 7. Safe Operating Area (SOA) for T_C = 80°C

Packaging Information

WLCSP97-63 (4.810mm x 3.790mm x 0.555mm)



Recommended Footprint