KTS1652

Single Input Single Output Load Switch with Surge Protection

Features

- 2.75V to 21.5V Operating Voltage Range
- 28V Abs. Max. Rating at VBUS and VOUT
- 9mΩ typ. On-Resistance from VBUS to VOUT
- 6A Continuous Current Rating
  - ▶ 12A Pulse Current Rating (5ms)
- Over-Voltage Protection (OVP) at VBUS
  - ▶ 12.4V (OVLO_SEL = LOW)
  - ▶ 21.9V (OVLO_SEL = HIGH)
- Transient Voltage Suppression (TVS) at VBUS
  - ▶ ±200V Surge Protection (IEC61000-4-5)
  - ▶ ±8kV ESD Contact Discharge (IEC61000-4-2)
  - ▶ ±15kV ESD Air Discharge (IEC61000-4-2)
- Over-Temperature Protection (OTP)
- OV_FLAGB Open-Drain Output Flag
- VBUS detection LDO
- Active VBUS Discharge Control Input
- Active-Low Enable Logic Input
- -40°C to 85°C Operating Temperature Range
- 20-bump WLCSP 2.460 x 1.967mm (0.4mm pitch)

Brief Description

KTS1652 is a low resistance, bi-directional high current load switch with over-voltage protection, over-temperature protection and integrated TVS. The integrated TVS at VBUS is rated up to IEC61000-4-5 ±200V Surge voltage and IEC61000-4-2 Level 4 Electrostatic Discharge, which protects the downstream components from abnormal input conditions.

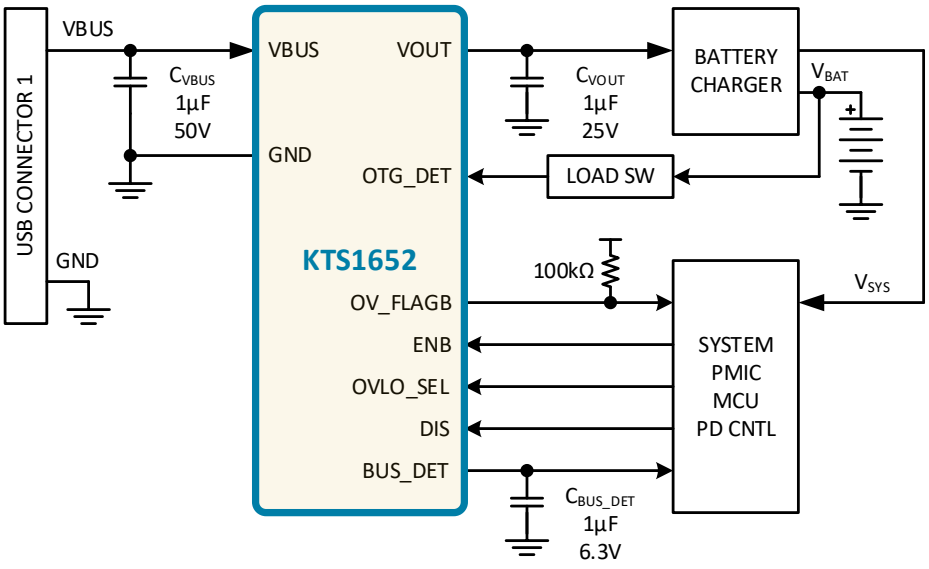
When VBUS is greater than V_{UVLO_BUS}, the integrated LDO provides an "always ON" power source at BUS_DET. BUS_DET voltage is regulated to typically 4.0V, regardless of the status of ENB, so to power downstream components permitting operation without an installed battery.

KTS1652 is packaged in advanced, fully "green" compliant, 2.460 x 1.967mm, 20-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Smartphones, Ultra-Books, Tablets

Typical Application



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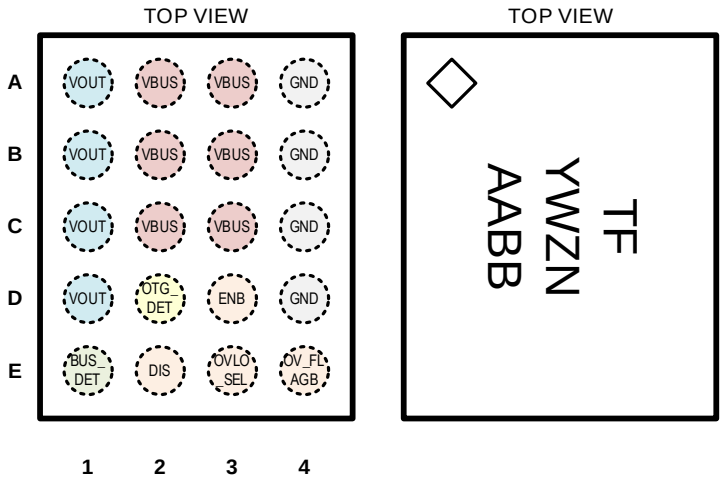
Ordering Information

Part Number	Marking[1]	Operating Temperature	Package
KTS1652EIAC-TA	TFYWZNAABB	-40°C to +85°C	WLCSP54-20

Pinout Diagram

WLCSP54-20



20-bump 2.460mm x 1.967mm x 0.555mm
WLCSP Package, 0.4mm pitch
Top Mark: TF = Device ID, YW = Date Code, ZN = Assembly Code, AABB = Serial Number

1. TF = Device ID, YW = Date Code, ZN = Assembly Code and AABB = Serial Number.

Pin Descriptions

Pin #	Name	Function
A2, A3, B2, B3, C2, C3	VBUS	Power Switch Input/Output and Device Power Supply.
A1, B1, C1, D1	VOUT	Power Switch Input/Output.
D2	OTG_DET	Power Supply Input for charge pump circuit during startup in OTG mode.
E1	BUS_DET	Always on LDO output powered by VBUS.
D3	ENB	Active Low Enable signal for VBUS-VOUT path. An internal 1MΩ pull-down resistor is integrated.
E2	DIS	Active High Enable signal for active discharge path at VBUS. An internal 1-MΩ pull-down resistor is integrated.
E3	OVLO_SEL	Selection of OVLO threshold. An internal 1-MΩ pull-down resistor is integrated. OVLO_SEL = LOW: ➔ OVLO threshold = 12.4 V (typ.) OVLO_SEL = HIGH: ➔ OVLO threshold = 21.9 V (typ.)
E4	OV_FLAGB	Open-drain type output indicating an over-voltage state. An external pull-up resistor is required.
A1, B4, C4, D4	GND	Ground. Connect this pin to system ground.

Absolute Maximum Ratings[2]

Symbol	Description	Value	Units
V_{VBUS}	VBUS to GND (continuous) VBUS to GND (during IEC61000-4-5 surge event)	-0.3 to 28 -5 to 36	V
V_{VOUT}	VOUT to GND	-0.3 to 28	V
V_{BUS_DET}	BUS_DET to GND	-0.3 to 6	V
V_I and V_O	OV_FLAGB, DIS, ENB, OVLO_SEL, OTG_DET to GND	-0.3 to 6	V
$I_{VBUS-VOUT}$	Maximum Switch Current (continuous) Peak Switch Current (duration is Pd limited)	6 12	A
I_{BUS_DET}	BUS_DET Maximum Switch Current (continuous)	> 10	mA
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[3]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (VBUS)	±8	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (VBUS)	±15	kV
V_{SURGE}	IEC61000-4-5 Surge (VBUS to GND)	±200	V

Thermal Capabilities[4]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	74	°C/W
P_D	Maximum Power Dissipation at 25°C (T_J = 125°C)	1.35	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-13.5	mW/°C

(continued next page)

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

3. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.

4. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions

Symbol	Description	Value	Units
V_{BUS}	VBUS Supply Voltage	2.75 to 21.5	V
V_{OUT}	VOUT Output Voltage	2.75 to 21.5	V
V_{BUS_DET}	BUS_DET Output Voltage	3 to 5.5	V
V_I, V_O	Logic Input and Output Voltage	0 to 5.5	V
C_{BUS}	Input Capacitance	1 to 10 50	µF V
C_{OUT}	Output Capacitance	1 to 10 25	µF V
C_{BUS_DET}	Output Capacitance	1 6.3	µF V
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Operating Temperature Range	-40 to 125	°C

(continued next page)

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operating range of T_A = -40°C to +85°C, V_{BUS} = 2.75V to 21.5V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V, I_{BUS} ≤ 2A, ENB = DIS = LOW, OVLO_SEL = Low and C_{BUS} =1µF.

VBUS Supply Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{BUS}	Input Voltage Operating Range			2.75		21.5	V
V_{UVLO_BUS}	Under-Voltage Lockout	V_{BUS} rising threshold Hysteresis		2.25	2.5 150	2.75	V mV
I_{Q_BUS}	No-Load Supply Current	VBUS = 5V, VOUT = open	ENB = L ENB = H		90 90	140 140	µA

VBUS to VOUT Switch Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
R_{ON_VOUT}	Switch On-Resistance	I_{VOUT} = 200mA, T_A = 25°C	V_{BUS} = 5V V_{BUS} = 12V V_{BUS} = 21V		9 9 9	12 12 12	mΩ
t_{ON_VOUT}	Switch Turn-On Time[6]	RL = 100 Ω, C_{VOUT} = 1 µF			1	3	ms
t_{DOFF_VOUT}[7]	Switch Turn-Off Response Time[8]	RL = 100 Ω, C_{VOUT} = 1 µF	OVLO_SEL = L OVLO_SEL = H			50 50	ns
t_{DEB_VOUT}	VBUS Debounce Time[9]				15	20	ms

Over-Voltage Protection (OVP) Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{BUS_OVLO}	Internal Over-Voltage Protection	OVLO_SEL = L	V_{BUS} rising V_{BUS} falling	12.1	12.4 12.1	12.7	V
		OVLO_SEL = H	V_{BUS} rising V_{BUS} falling	21.4	21.9 21.5	22.4	
I_{IN_OVLO}	OVLO Supply Current[10]	OVLO_SEL = L, VBUS = 15V OVLO_SEL = H, VBUS = 23V			120 160	160 180	µA
V_{OUT_MAX}[7]	Maximum VOUT during positive surge[11]	VBUS=11V, +200V Surge, OVLO_SEL=L VBUS=21V, +200V Surge, OVLO_SEL=H				15 23	V

5. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

6. t_{ON_VOUT} is time from the specified test condition and from V_{VOUT} = 10%*V_{VBUS} until V_{VOUT} = 90%*V_{VBUS}.

7. Guaranteed by design, characterization, and statistical process control methods; not production tested.

8. T_{DOFF_VOUT} is time from VBUS = V_{BUS_OVLO} to VOUT stop rising. Measured when VBUS rises from 0V to 15V (OVLO_SEL = L) or from 0V to 25V (OVLO_SEL = H) at 14V/µs Slew Rate.

9. t_{DEB_VOUT} is time from $V_{BUS\_UVLO} \leqslant$ VBUS < V_{BUS_OVLO} to VOUT = 0.1 x VBUS.

10. I_{IN_OVLO} is VBUS input current measured using the specified test condition, together with VOUT = open and ENB = L.

11. V_{OUT_MAX} is measured using the specified test condition, together with ENB = L, VOUT = Open and without any C_{VOUT}.

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operating range of T_A = -40°C to +85°C, V_{BUS} = 2.75V to 21.5V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V, I_{BUS} ≤ 2A, ENB = DIS = LOW, OVLO_SEL = Low and C_{BUS} =1µF.

Active VBUS Discharge Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{VBUS_DIS}	VBUS Discharge Resistance[12]	VBUS = 5V, DIS = 1.8V		550		Ω
$t_{VBUS\_DIS\_ON}$	VBUS Discharge ON Delay Time[13]	VOUT = 5V, DIS pin from Low to High		200		ns
t_{VBUS_DIS}	VBUS Discharge Time[14]	VOUT = 5V, C_{VBUS} = C_{OUT} =1µF, DIS pin from 0V to 1.8V		1.1	5	ms
$t_{VBUS\_DIS\_OFF}$	VBUS Discharge OFF Delay Time[15]	VOUT = 5V, DIS pin from High to Low		1	3	µs

OTG Mode (VOUT to VBUS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage Operating Range		2.75		21.5	V
$V_{OTG\_DET\_UVLO}$	OTG_DET Under-Voltage Lockout	V_{OTG_DET} rising threshold V_{OTG_DET} falling threshold	2.80	2.95 2.80	3.10	V V
$I_{IN\_OTG\_DET}$	OTG_DET Input Supply Current[16]	OTG_DET = 2.5 V, VOUT = 0 V OTG_DET = 5 V, VOUT = 0 V OTG_DET = 4.5 V, VOUT = 5 V OTG_DET = 0 V, VOUT = 5 V		0.2 50 0.4 < 0.1	1 120 1 1	µA
R_{ON_OTG}	Switch On-Resistance in OTG mode	VOUT = 5 V, IBUS = -200 mA, T_A = 25 °C		9	12	mΩ
t_{DON_OTG}	OTG_DET Startup Delay Time[17]	T_A = -40 °C to 85 °C		0.6	1	ms

BUS_DET Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{BUS_DET}	BUS_DET Regulation Output Voltage	VBUS = 5V / 21V, I_{BUS_DET} = 0mA / 10mA, C_{BUS_DET} = 1µF	3.8	4.0	4.2	V
$t_{START\_BUS\_DET}$	Soft-Start Current Limit Done Time[18]			37		ms

12. R_{VBUS_DIS} can be higher than 550Ω when DIS < 1.8V or lower than 550Ω when DIS > 1.8V.

13. $t_{VBUS\_DIS\_ON}$ is time from DIS = L -> H until Discharge path is ON (IOUT = IBUS + Discharge current).

14. t_{VBUS_DIS} is time from when VBUS first begins to fall until VBUS = 10%*VOUT, once DIS = ENB = LOW → HIGH and VOUT source is removed at the same time.

15. $t_{VBUS\_DIS\_OFF}$ is time from DIS = H -> L until Discharge path is OFF (IOUT = IBUS).

16. $I_{IN\_OTG\_DET}$ is OTG_DET input current measured using specified test condition, together with ENB = L, VBUS = Open, TA = -40 °C to 85 °C.

17. t_{DON_OTG} is time from OTG_DET ⩾ $V_{OTG\_DET\_UVLO}$ to VBUS = VOUT (Charge Pump Output Enable).

18. $t_{START\_BUS\_DET}$ is time from VBUS ⩾ V_{BUS_UVLO} to BUS_DET = 10% of target value.

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operating range of T_A = -40°C to +85°C, V_{BUS} = 2.75V to 21.5V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V, I_{BUS} ≤ 2A, ENB = DIS = LOW, OVLO_SEL = Low and C_{BUS} =1µF.

Transient Voltage Suppression (TVS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RW_P}	Positive Reserve Working Voltage				28	V
V_{BR_P}	Positive Breakdown Voltage	I_{VBUS} = 1mA, T_A = 25°C	30	32	34	V
V_{CL_P}[19]	Positive Clamping Voltage	+200V Surge			40	V
$I_{IN\_PK\_P}$[19]	Positive Peak Surge Current	+200V Surge			100	A
V_{F_TVS}	Forward Voltage	I_{VBUS} = -10mA	0.2	0.6	0.8	V
V_{CL_N}[19]	Negative Clamping Voltage	-200V Surge	-6			V
$I_{IN\_PK\_N}$[19]	Negative Peak Surge Current	-200V Surge	-100			A

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{OTP}[19]	IC Junction Over-Temperature Protection	T_J rising threshold Hysteresis		145 20		°C °C

Logic Pin Specifications (OV_FLAGB, ENB, DIS, OVLO_SEL)

Symbol	Description	Conditions	Min	Typ	Max	Units
OV_FLAGB						
$V_{OV\_FLAGB\_OL}$	Output Logic Low	VIO = 1.2V/1.8V, Rpu = 100kΩ			0.36	V
$t_{OV\_FLAGB\_DELAY}$	OV_FLAGB Assertion Delay Time[20]	ENB = H/L			3	µs
$t_{OV\_FLAGB\_REC}$	OV_FLAGB Recovery Debounce Time[21]	ENB = L ENB = H	16 100	20 140		ms µs
ENB, DIS, OVLO_SEL						
V_{IH1}	Input Logic High	VIO = 1.2V/1.8V	0.84			V
V_{IL1}	Input Logic Low	VIO = 1.2V/1.8V			0.54	V
R_{I_PD}	Input Logic Pull-Down			1		MΩ

19 Guaranteed by design, characterization, and statistical process control methods; not production tested.

20. $t_{OV\_FLAGB\_DELAY}$ is time from VBUS ⩾ V_{BUS_OVLO} to OV_FLAGB = L. When ENB = H, Initial VBUS voltage is expected to settle at ⩾ V_{BUS_UVLO} and < V_{BUS_OVLO} for a long time before the over-voltage event.

21. $t_{OV\_FLAGB\_REC}$ is time from VBUS ⩽ V_{BUS_OLVO} to OV_FLAGB = H. When ENB = L, OV_FLAGB Recovery Debounce Time should always be longer than VBUS debounce time + Switch Turn-on delay.

Timing Diagrams

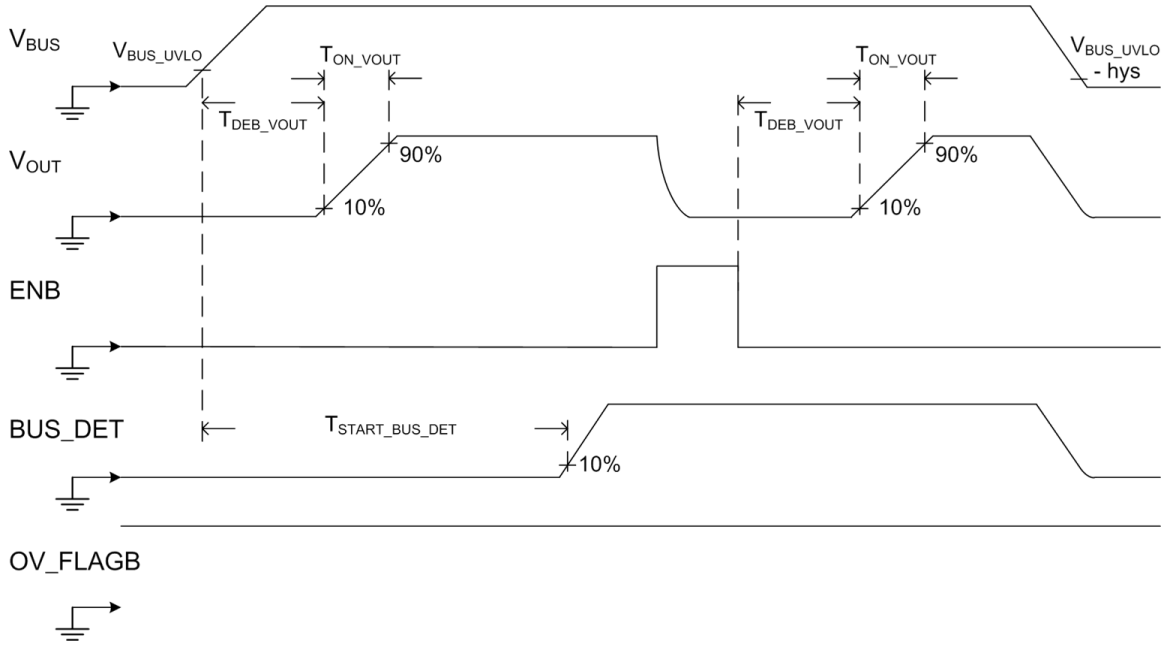


Figure 1. VBUS Ramp-up, Ramp down and ENB Toggling

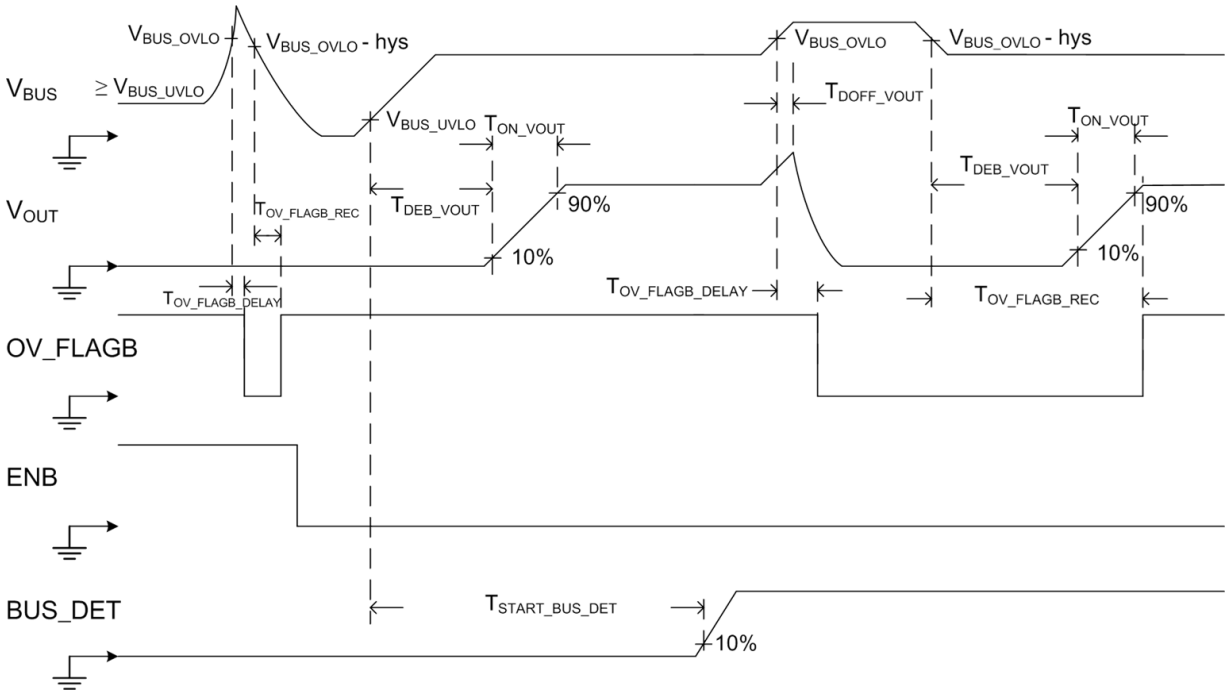


Figure 2. Over Voltage Protection (OVP) Trigger and Recover

Timing Diagrams

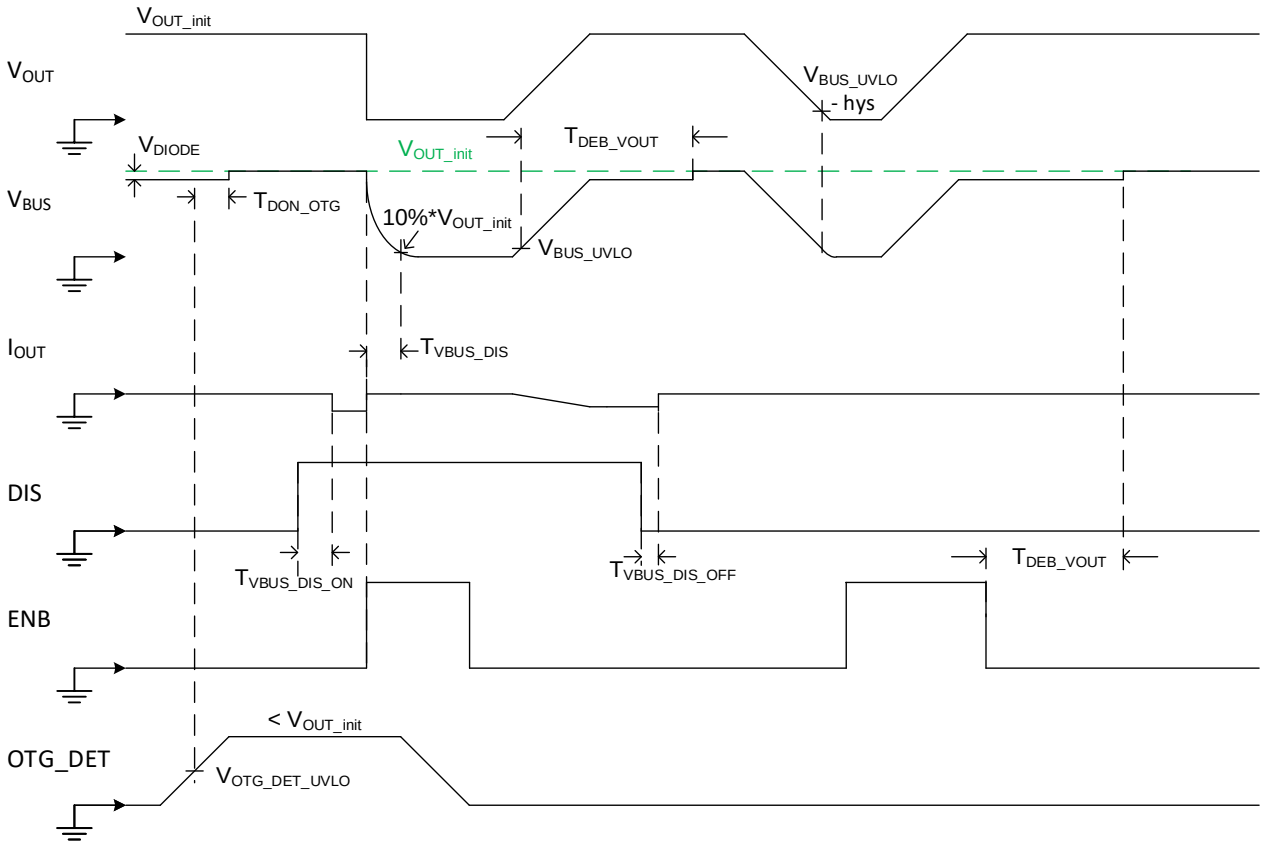


Figure 3. OTG Mode and VBUS Active Discharge

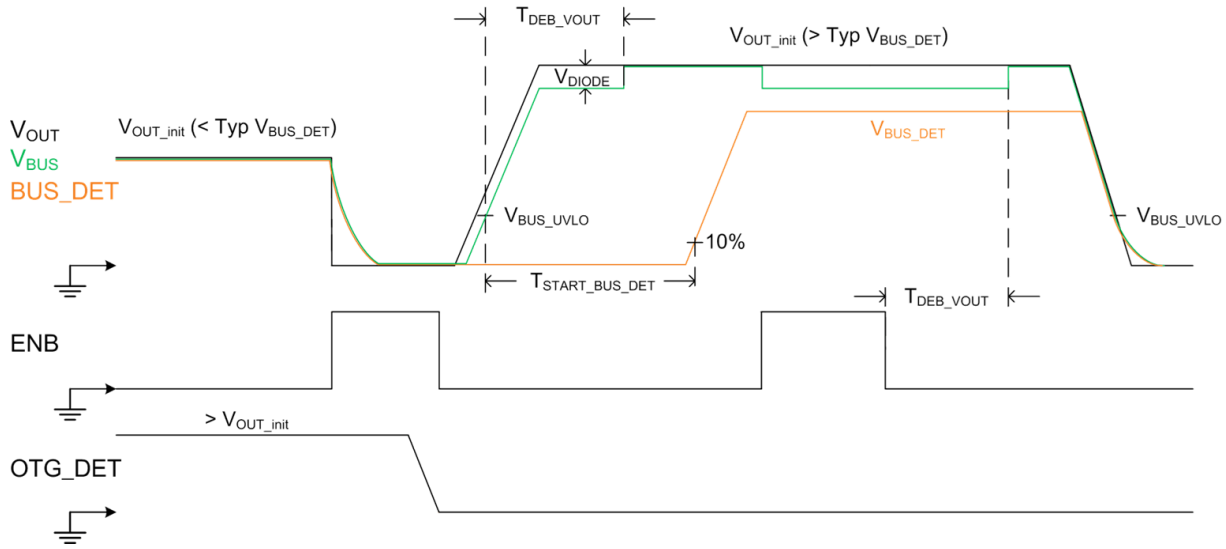


Figure 4. OTG Mode and BUS_DET

Timing Diagrams

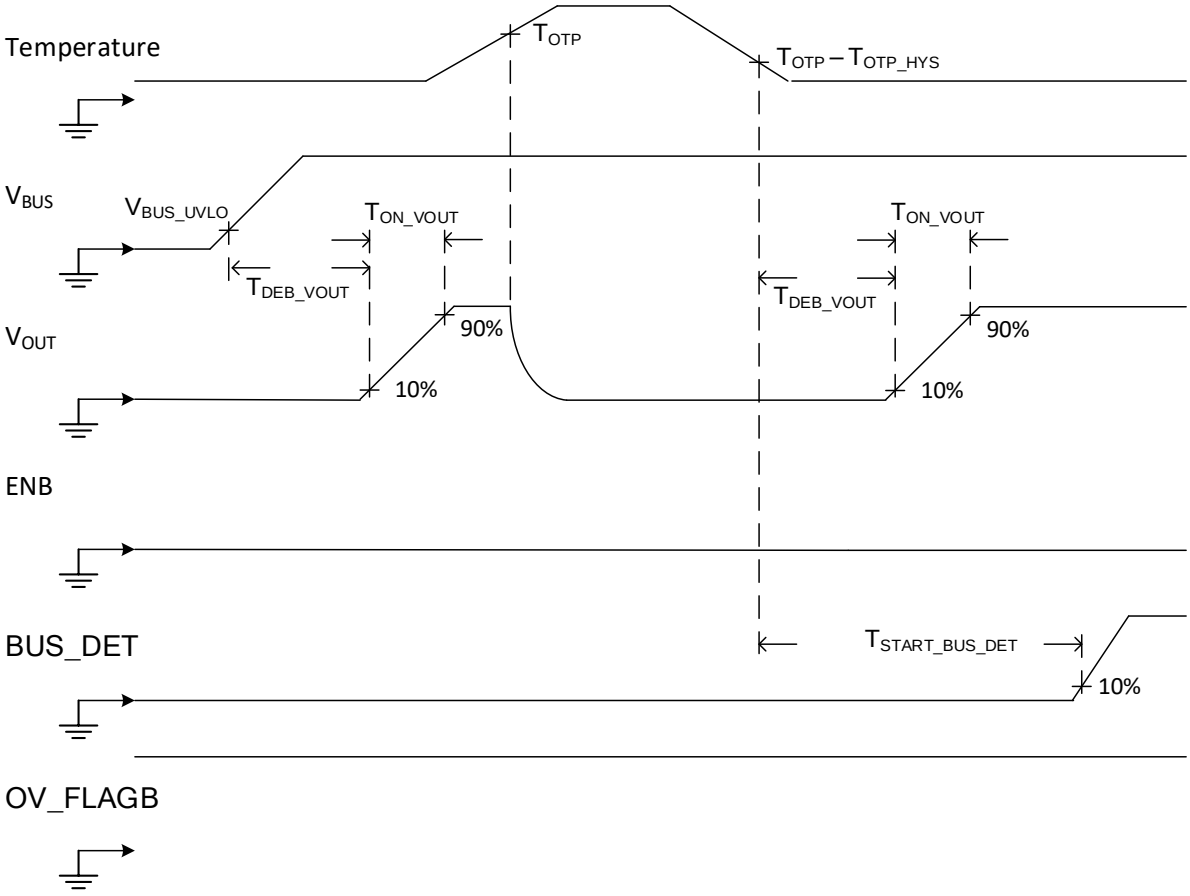


Figure 5. Over Temperature Protection (OTP)

Timing Diagrams

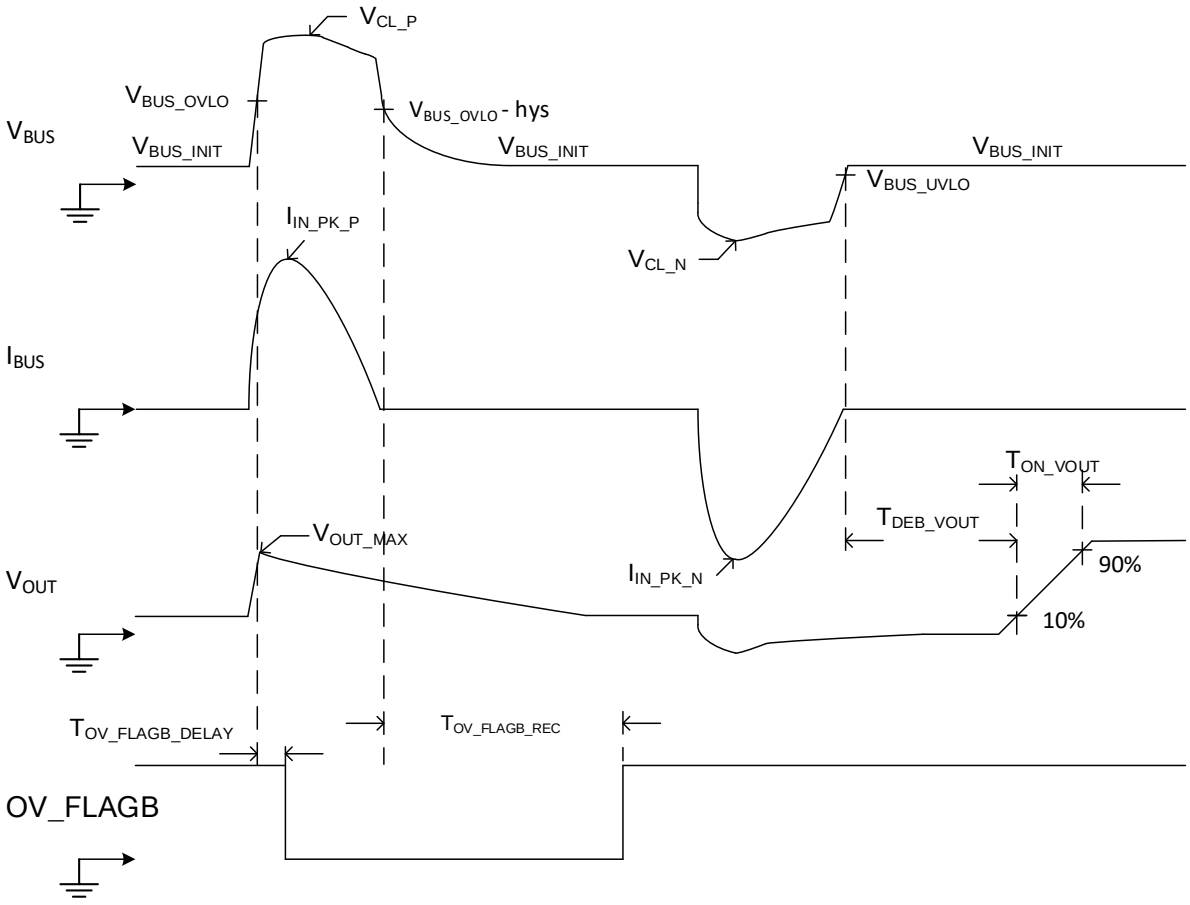
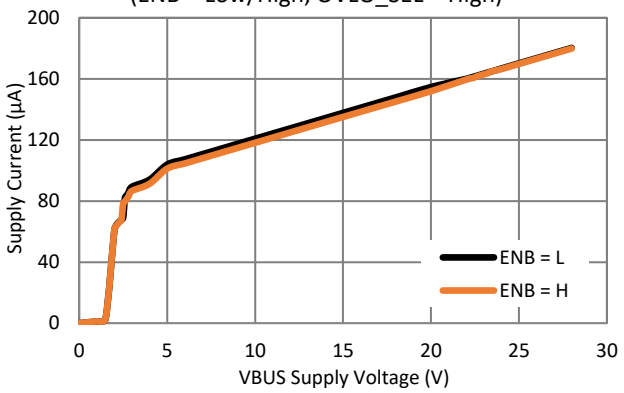


Figure 6. VBUS Surge per IEC61000-4-5 Standard

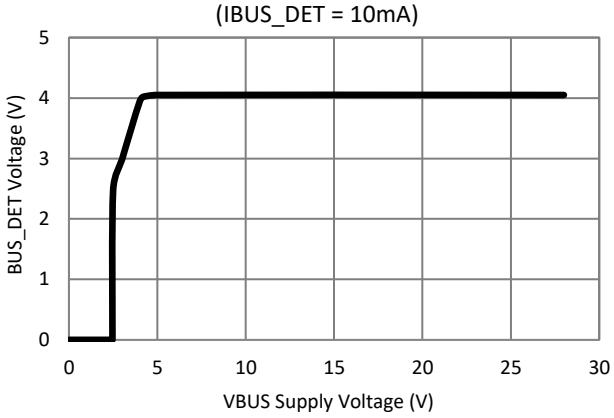
Typical Characteristics

V_{BUS} = 5V, ENB = GND, DIS = GND, OVLO_SEL = GND, C_{VBUS} = 1uF, C_{OUT} = 1µF, CBUS_DET = 1µF and T_A = +25°C unless specified otherwise.

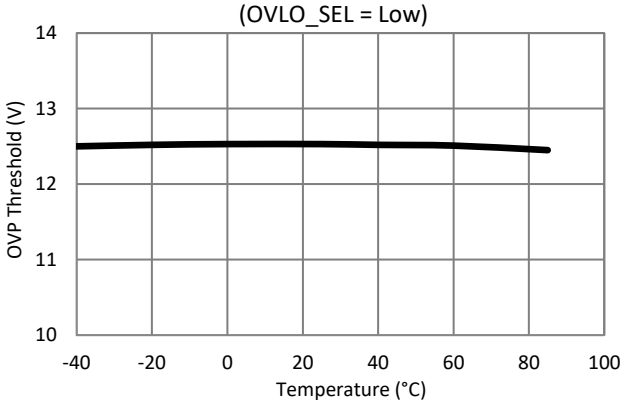
No-Load Supply Current vs. VIN Voltage
(ENB = Low/High, OVLO_SEL = High)



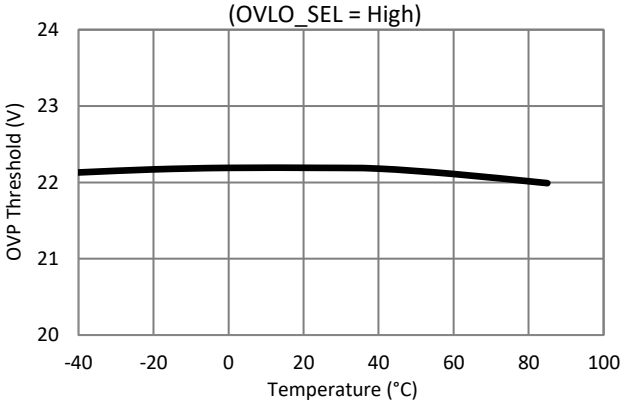
BUS_DET Regulation Voltage vs. VBUS Voltage
(IBUS_DET = 10mA)



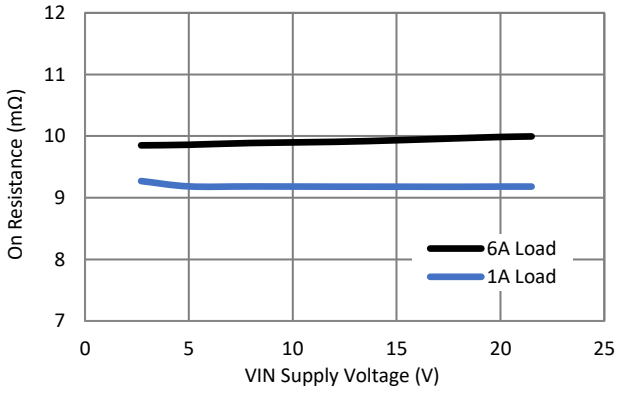
OVP Threshold vs. Temperature
(OVLO_SEL = Low)



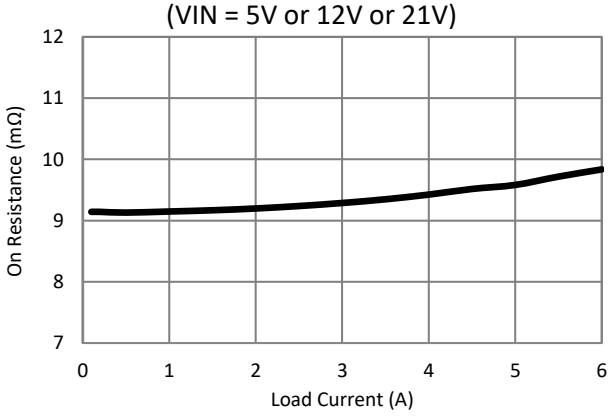
OVP Threshold vs. Temperature
(OVLO_SEL = High)



Switch On-Resistance vs. VIN



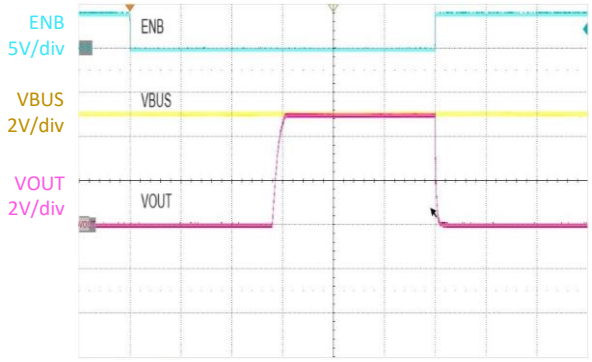
Switch On-Resistance vs. Load Current
(VIN = 5V or 12V or 21V)



Typical Characteristics

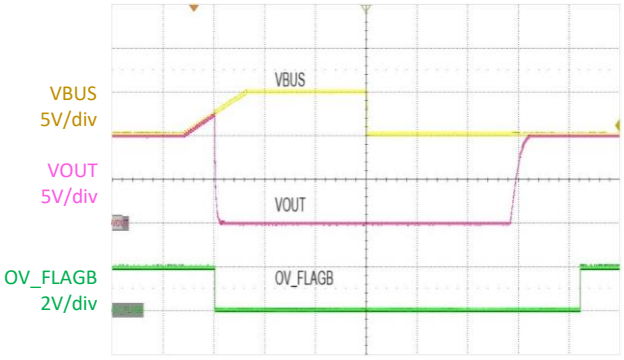
V_{BUS} = 5V, ENB = GND, DIS = GND, OVLO_SEL = GND, C_{VBUS} = 1uF, C_{OUT} = 1µF, CBUS_DET = 1µF and T_A = +25°C unless specified otherwise.

Enable Turn-on, Turn-off Response
(100Ω load)



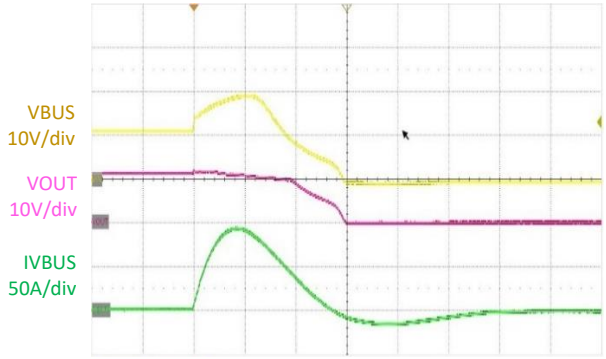
5ms/div

OVP Response with OV_FLAGB and Recovery
(100Ω load, VBUS from 10V to 15V to 10V)



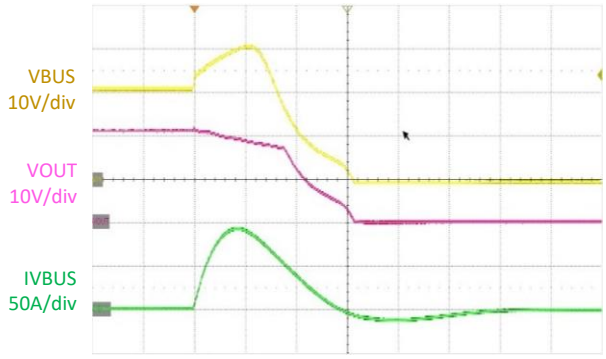
5ms/div

Surge Transient Response
(VBUS = 11VDC, +200V Surge, OVLO_SEL = Low)



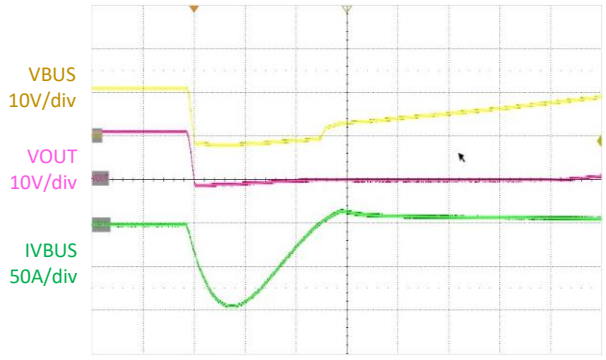
10µs/div

Surge Transient Response
(VBUS = 21VDC, +200V Surge, OVLO_SEL = High)



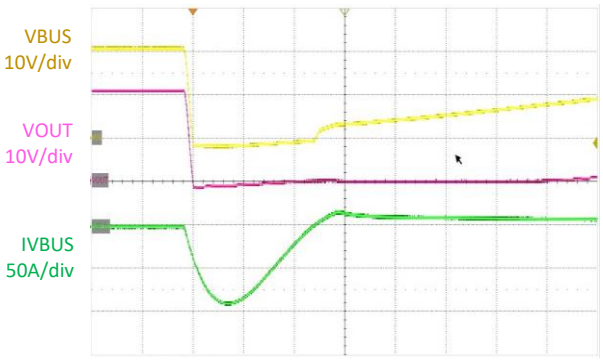
10µs/div

Surge Transient Response
(VBUS = 11VDC, -200V Surge, OVLO_SEL = Low)



10µs/div

Surge Transient Response
(VBUS = 21VDC, -200V Surge, OVLO_SEL = High)



10µs/div

Functional Block Diagram

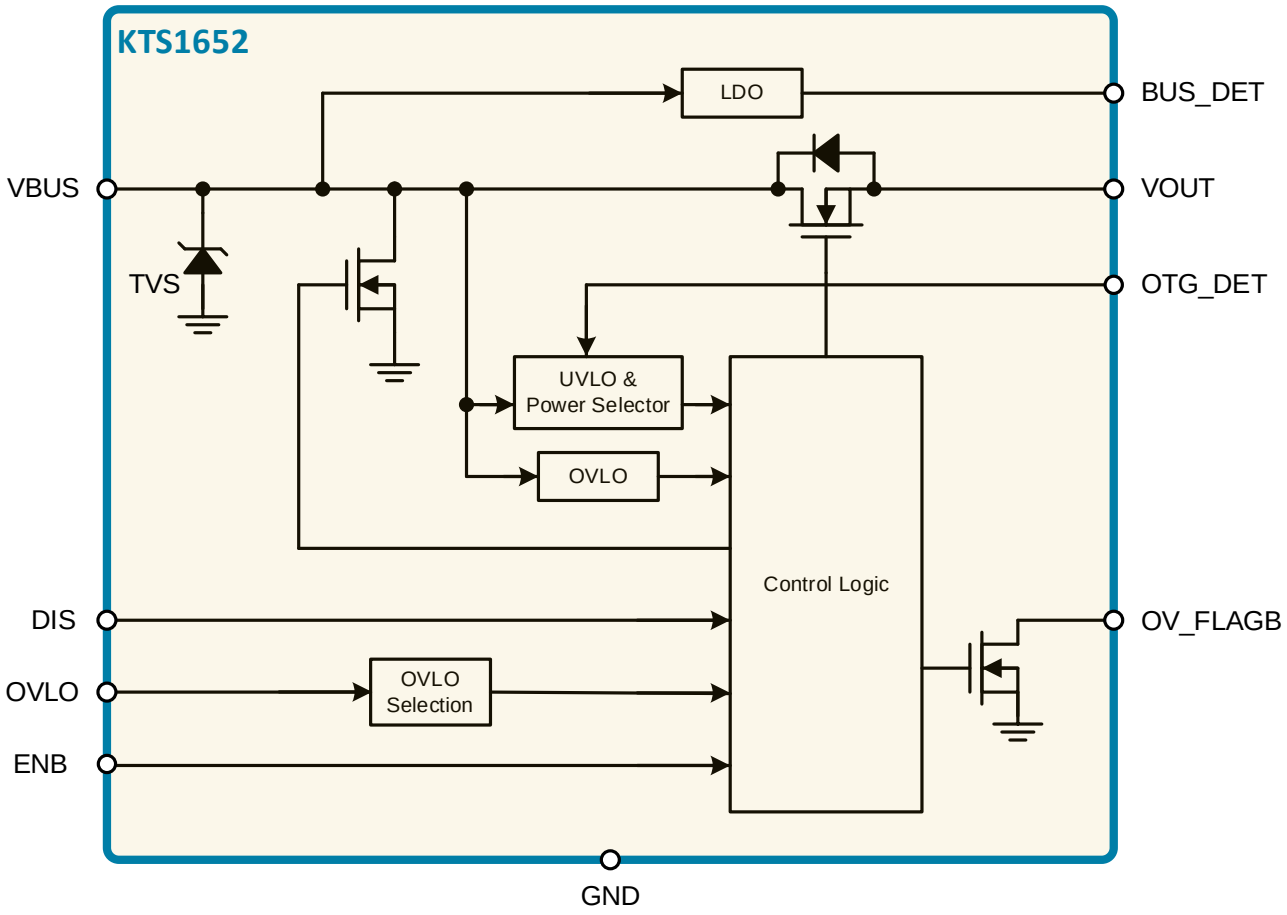


Figure 7. Functional Block Diagram

Functional Description

KTS1652 is a low resistance, bi-directional high current load switch with over-voltage protection, over-temperature protection and integrated TVS. The integrated TVS at VBUS is designed to protect against IEC61000-4-5 ±200V Surge voltage and IEC61000-4-2 Level 4 Electrostatic Discharge, which safeguards the downstream components from abnormal input conditions.

The power switch connected VBUS to VOUT is a low resistance MOSFET switch, which is typically 9mΩ. It is intended to be used on VBUS in USB-C to protect against abnormal voltage and current conditions from a power source to a load. VBUS to VOUT is dedicated to sink current, up to 6A, from VBUS to system side; but can also source the same amount of current from system side to VBUS in OTG mode.

Under-Voltage Lockout (UVLO)

When $V_{BUS} < V_{UVLO\_BUS}$, the power switch is disabled. Once V_{BUS} exceeds V_{UVLO_BUS}, the power switch is controlled by the ENB pin and fault detection circuits.

Over-Voltage Protection (OVP)

When VBUS input voltage is greater than V_{BUS_OVLO}, the power switch is disabled. Once VBUS input source voltage drops below V_{BUS_OVLO} - Hysteresis, and no other fault is detected, the power switch re-enables via debounce time and turn on time. The KTS1652 has 2 preset over-voltage thresholds, 12.4V or 21.9V; and these two thresholds can be selected by biasing OVLO_SEL pin to either logic low or logic high.

Transient Voltage Suppressor (TVS)

KTS1652 has a Transient Voltage Suppressor (TVS) connected from VBUS to GND, which is designed to protect against up to IEC61000-4-5 ±200V Surge voltage and IEC61000-4-2 Level 4 Electrostatic Discharge. The internal TVS positive breakdown voltage is 32V (typ), and it is design guaranteed to clamp VBUS voltage at 40V or lower during +200V Surge. Since KTS1652 OVP response time is fast, VOUT is also design guaranteed not to exceed 15V with VBUS = 11V and V_{OVLO_BUS} = 12.4V, or not to exceed 23V with VBUS = 21V and V_{OVLO_BUS} = 21.9V, when +200V surge is applied at VBUS and VOUT is not loaded with any output capacitance or load. During -200V surge, TVS is forward biased and VBUS negative voltage is limited to -6V or higher. When testing surge on the bench, each surge voltage, either positive or negative, is tested 100 times, with 1 second relief time before the next surge pulse. VBUS I-V curve should not show any shift after the surge test, otherwise it is considered as failed.

USB On-The-Go (OTG) Mode

KTS1652 can be powered up from VBUS or VOUT to enable operation in systems that support USB On-The-Go (OTG). There are two ways to enable OTG mode. One way is to set VOUT > V_{UVLO_BUS} + V_{DIODE} (~1V), and then OTG mode should be ready after VBUS debounce time. The other way to enable OTG mode is by setting OTG_DET pin voltage ≥ VOTG_DET_UVLO, and then VOUT to VBUS power switch should be fully turned on after OTG_DET Startup Delay time for VOUT initial > V_{UVLO_BUS} (2.75V). Since OTG startup delay time is much shorter than VBUS debounce time, the later method to turn on OTG mode is much quicker. In OTG mode, KTS1652 is powered from VOUT or OTG_DET, whichever is higher, instead of VBUS; as a result, the input current at VBUS drops to 1µA or less. VBUS should always equal to VOUT when ENB=L and power is switching from OTG_DET to VOUT, or vice versa. Switch On-Resistance in OTG mode is the same as normal mode (VBUS to VOUT), which is typically 9mΩ, and it can also support up to 6A current to be delivered from VOUT to VBUS.

BUS_DET

When VBUS is greater than V_{UVLO_BUS}, the integrated LDO provides an “always ON” power source at BUS_DET. BUS_DET voltage is regulated to 4.0V typically, regardless of the status of ENB input, so to power downstream components permitting operation without an installed battery. The BUS_DET LDO supplies up to 10mA of output current. BUS_DET should always be coupled with 1µF at least; otherwise, its voltage can overshoot beyond its absolute maximum rating during fast VBUS voltage transient event, such as Surge event.

Over-Temperature Protection (OTP)

When device junction temperature exceeds 145°C, the OTP circuit disables VBUS to VOUT switch. Once the device junction temperature decreases below 125°C, and no other fault is detected, the power switch returns to its previous state via debounce time and switch turn on time.

VBUS Input Discharge

For USB Power Delivery (PD), KTS1652 features an active discharge for the VBUS node. When DIS is set to logic high, the internal 550Ω connected from VBUS to GND is enabled and discharges VBUS from as high as 20V to below 0.8V within 650ms, with sufficient margin for any excess capacitance on VBUS due to the compliance test equipment. Enabling active discharge with a constant voltage at VBUS can cause continuous excessive power dissipation, which should be avoided at all costs.

OV_FLAGB Output Flag

The OV_FLAGB output is an active-low, open-drain output that requires an external pull-up resistor. The pull up resistor value is recommended to be 10 KΩ to 200 KΩ. When there is no over voltage fault and the power switch is ON, the OV_FLAGB flag is high impedance to indicate no fault condition is detected. Whenever over voltage fault (VBUS ≥ V_{OVLO_BUS}) at VBUS triggers OVP, OV_FLAGB pin actively pulls to GND after $T_{OV\_FLAGB\_DELAY}$. Once VBUS recovers back to V_{OVLO_BUS} - hysteresis, OV_FLAGB automatically returns back to high impedance after Recovery Debounce Time ($T_{OV\_FLAGB\_REC}$). OV_FLAGB Recovery debounce time is short (100us) when KTS1652 is not enabled (ENB = H) and VBUS is initially settled at ≥ V_{BUS_UVLO} and < V_{BUS_OVLO} for a long time before the over-voltage event; but it is extended to 20ms (typ) when KTS1652 is already enabled (ENB = L) before OVP event, so to assure OV_FLAGB will be reset to high impedance only after VOUT is fully recovered.

ENB Enable Control

The ENB is an active-low input with an internal 1MΩ pull-down resistor. ENB = H disables the power switch, but it is not intended to reduce input supply current. ENB = L enables the protection circuits and the power switch. A 15ms debounce time deploys before device turns on.

Table 1. BUS_DET and OV_FLAGB Truth Table

VBUS	OTP	ENB	BUS_DET	OV_FLAGB
VBUS < V_{BUS_UVLO}	X	X	OFF	HI-Z
V_{BUS_UVLO} ≤ VBUS < V_{BUS_OVLO}	0	X	ON	HI-Z
	1	X	OFF	HI-Z
VBUS ≥ V_{BUS_OVLO}	0	X	ON	LOW
	1	X	OFF	HI-Z

X = Don't Care

PCB Layout Guidelines

Optimized trace routing and placement are important to assure KTS1652 protection features. The following guidelines are recommended for best system performance:

1. KTS1652 IC package should be placed as close as possible to the USB Type-C connector to maximize ESD, surge and OVP protection for the system.
2. For the printed circuit board, a good thermal design is recommended to support 6A fully loaded current. VBUS, VOUT and GND should have a reasonable size of copper pour, so that it can be used as a thermal dissipating interface. Additional thermal vias can also help to conduct the heat to the other side of PCB, with additional copper plate.
3. Place the input bypass capacitors and output decoupling capacitor as close to VBUS, VOUT and BUS_DET as possible. Connect the ground terminal of the capacitor to the ground plane using multiple vias.
4. Signal trace for OV_FLAGB, ENB, OTG_DET, OVLO_SEL and DIS are low current traces.

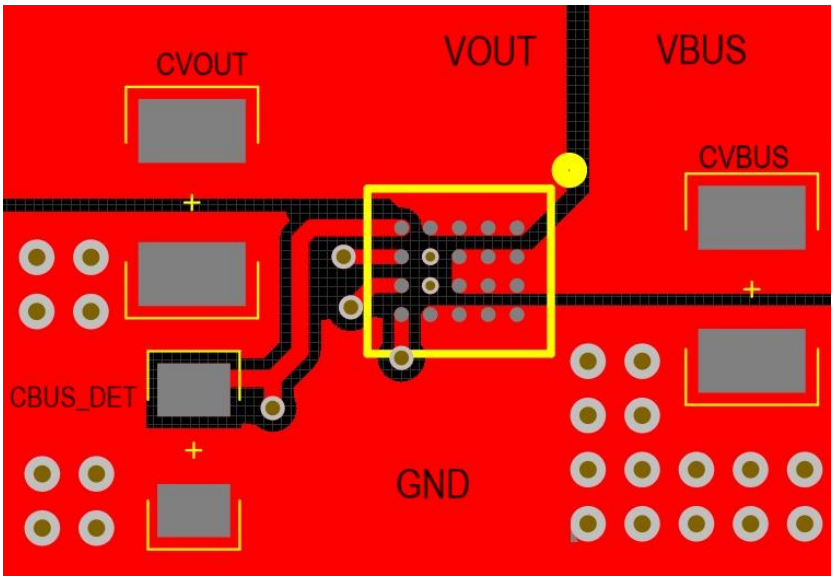
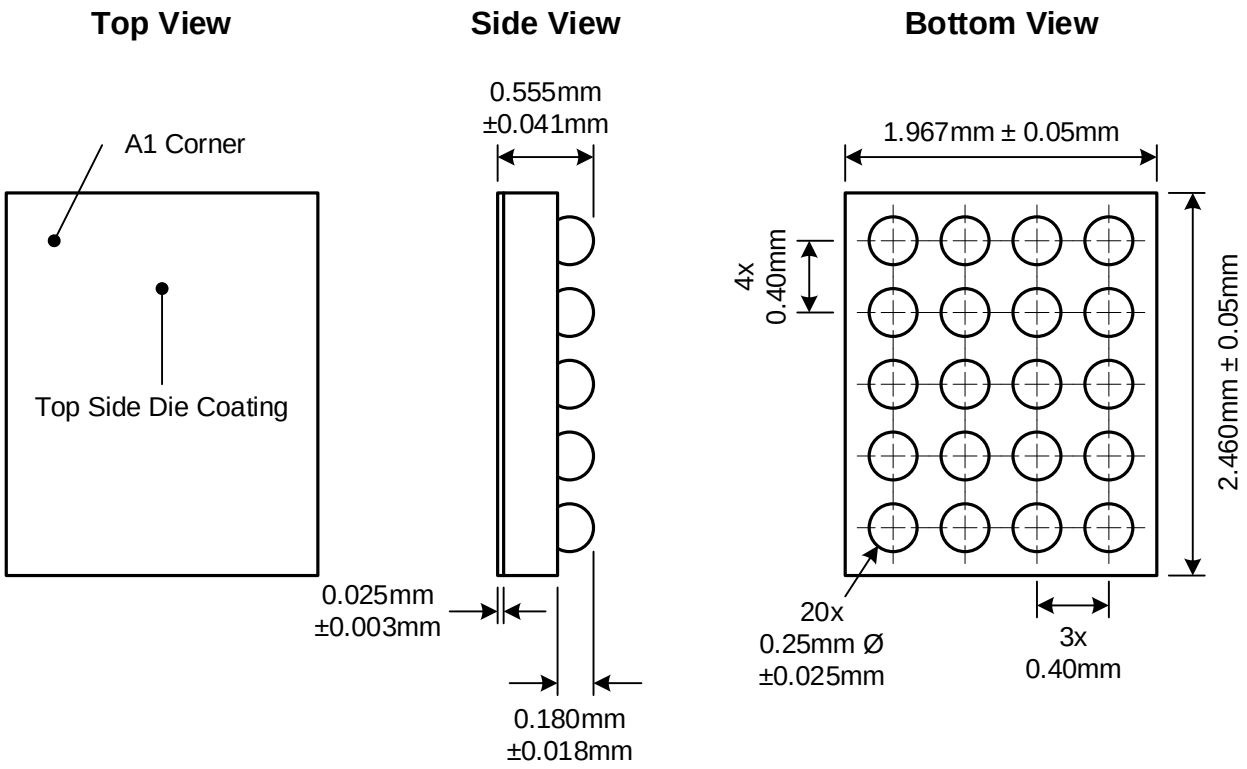


Figure 8. Recommended PCB Layout

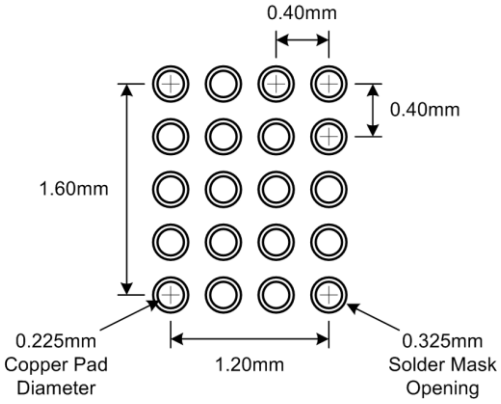
Packaging Information

WLCSP54-20 (2.460mm x 1.967mm x 0.555mm)



Recommended Footprint

(NSMD Pad Type)



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