KTE7200

Low Cost 5W Wireless Power Receiver

Features

- Single-Chip Solution up to 5-watt wireless power
- WPC/Qi v1.2 Standards Compatible
- Optimized for small coil designs
  - Reliable low voltage startup
  - Fixed 5.1V LDO regulated output
  - High efficiency synchronous rectifier for system level efficiency up to 78%
  - Output protection current limit
  - Robust fully internal overvoltage protection
  - Multifunction GPIO with switchable high-precision 20µA current source
- I²C Serial Interface, Enable input, Interrupt output
- -40°C to 85°C Operating Temperature Range
- Standard TQFN-24 package (5mm x 5mm x 0.750mm)

Brief Description

KTE7200 is a robust single chip wireless power receiver optimized for low cost, low component count, and low cost PCB designs. This device is optimized for small low power devices with small coils, while also being capable of as much as 5 watts of output with an appropriate thermal design.

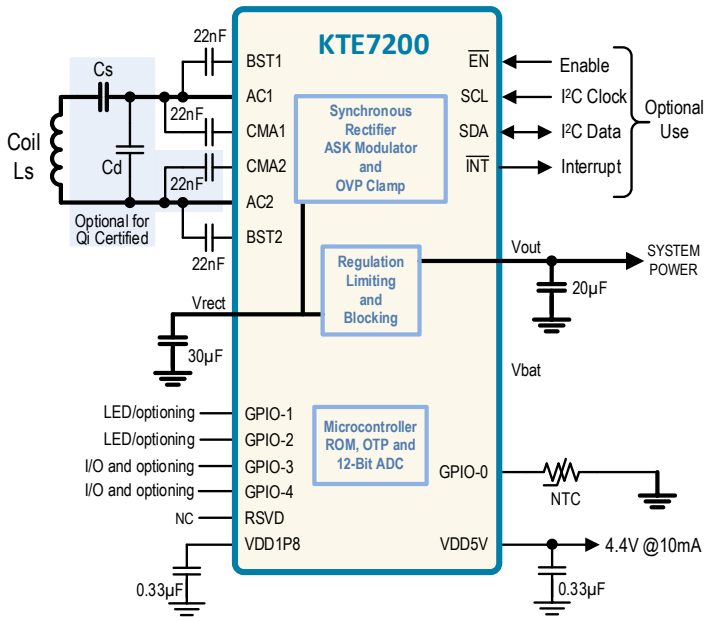
This is a microcontroller based design, optionally configurable by OTP memory, resistor programming features, and/or control via the I2C interface.

KTE7200 is highly integrated including 8k ROM, 8k OTP memory, an LDO regulator with OVP/OCP/RCP, and precision regulated DC output.

Applications

- Earbud Cases, Mice, IoT Devices, Accessories
- Personal Care Products, Toys, etc.
- Other Battery-Powered Equipment
- Battery-free Devices using only wireless power

Typical Application



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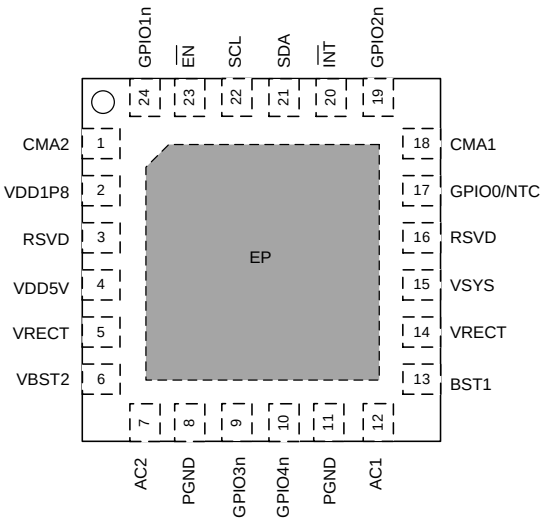
Ordering Information

Part Number[1]	Marking[2]	Default CV	Operating Temperature	Package
KTE7200EUAK-DA-TB	KTE7200-DA YYWWVXXX	5.10V	-40°C to +85°C	TQFN55-24

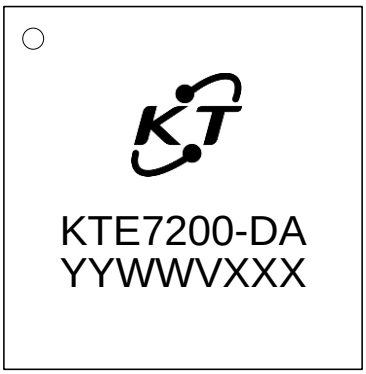
Pinout Diagram

TQFN55-24

TOP VIEW



TOP VIEW



24-Pin 5mm x 5mm x 0.75mm
TQFN Package, 0.65mm pitch

Top Mark

DA = ROM Code

YY = Date Code (Year), WW = Date Code (Week), V = Assembly Code, XXX = Serial Number

1. Firmware code is included in the ordering part number. Please contact Kinetic Sales for further details.
2. DA = ROM Code, YY = Date Code (Year), WW = Date Code (Week), V = Assembly Code, XXX = Serial Number.

Pin Descriptions

Pin #	Name	Function
1	CMA2	Wireless Power ASK Modulation – connect to modulation capacitor
2	VDD1P8	Internal 1.8V LDO Bias – connect an external 1µF bypass capacitor from this pin to the ground plane.
3	RSVD	Reserved. Leave floating (No connect).
4	VDD5V	Internal 5V LDO Bias – connect an external 1µF bypass capacitor from this pin to the ground plane.
5	VRECT	Rectified Output Voltage – connect to bulk storage capacitors
6	VBST2	Boost Pin for AC2 – connect to AC2 bootstrap capacitor
7	AC2	Rectifier Input #1 – connect to power delivery LC tank circuit
8	PGND	Power Ground – connect directly to main ground plane
9	GPIO3	General Purpose I/O – use as input/output per application
10	GPIO4	GPIO-4 General Purpose I/O – use as input/output per application
11	PGND	Power Ground – connect directly to main ground plane
12	AC1	Rectifier Input #1 – connect to power delivery LC tank circuit
13	VBST1	Bootstrap Pin for AC1 – connect to AC2 bootstrap capacitor
14	VRECT	Rectified Output Voltage – connect to bulk storage capacitors
15	VSYS	Main System Voltage Output – connect to client system power bus
16	RSVD	Reserved – connect to ground.
17	GPIO0/NTC	GPIO-3 General Purpose I/O – connect to battery temperature thermistor or other input/output circuitry per application
18	CMA1	Wireless Power ASK Modulation – connect to modulation capacitor
19	GPIO2	GPIO-1 General Purpose I/O – use as input/output per application
20	$\overline{\text{INT}}$	Active-Low Interrupt Open-Drain Output – optional output to client interrupt input function. Connect to ground if not used.
21	SDA	I^2C Data Input/Output – connect to the master's I^2C data line and a pull-up resistor to the system I/O voltage rail.
22	SCL	I^2C Clock Input – connect to the master's I^2C clock output and a pull-up resistor to the system I/O voltage rail.
23	$\overline{\text{EN}}$	Active-Low Enable Input – connect to ground or logic 0 to enable the IC.
24	GPIO1	GPIO-1 General Purpose I/O – use as input/output per application.
PADDLE	GND	Ground paddle must be electrically connected to ground plane

Absolute Maximum Ratings[3]

Symbol	Description	Value	Units
V_{RECT}	VRECT to GND (without internal 25V clamp)	-0.3 to 28	V
V_{RECT} - V_{SYS}	VRECT to VSYS	-6 to 28	V
V_{SYS}	VSYS to GND	-0.3 to 6	V
V_{SYS} - V_{BAT}	VSYS to VBAT	-6 to 6	V
V_{BAT}	VBAT to GND	-0.3 to 6	V
V_{DD5V}	VDD5V to GND	-0.3 to 6	V
V_{DD1P8}	VDD1P8 to GND	-0.3 to 2	V
$V_{\overline{EN}}$	$\overline{EN}$ to GND	-0.3 to 6	V
V_{I2C}	SCL, SDA, $\overline{INT}$ to GND	-0.3 to 6	V
$I_{VRECT-SYS}$	VRECT to VSYS Continuous Current	1.6	A_{RMS}
V_{AC}	AC1, AC2 to PGND	-0.3 to 26	V
$V_{RECT-AC}$	VRECT to AC1, VRECT to AC2	-0.3 to 26	V
V_{BST}	BST1, BST2 to AGND	-0.3 to 26	V
V_{BST-AC}	BST1 to AC1, BST2 to AC2	-0.3 to 6	V
V_{CM}	CMA1, CMA2 to AGND	-0.3 to 26	V
$V_{\overline{EN}}$	$\overline{EN}$ to AGND	-0.3 to 28	V
V_{I2C}	SCL, SDA, $\overline{INT}$ to AGND	-0.3 to 6	V
V_{GPIO}	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4 to AGND	-0.3 to V_{DD5V}+0.3	V
I_{AC}	AC1, AC2 Current	2.6	A
T_J	Operating Temperature Range	-40 to 140	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[4]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV

3. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

4. ESD Ratings conform to JEDEC standards.

Thermal Capabilities[5]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	30.16	°C/W
Θ_{JB}	Thermal Resistance – Junction to Board	8.06	°C/W
P_D	Maximum Power Dissipation at 25°C (T_J = 125°C)	3.32	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-33.17	mW/°C

Recommended Operating Conditions

Symbol	Description	Value	Units
V_{RECT}	Input operating voltage	3.6 to 10	V
C_{SYS}	System output capacitor	10	µF
		6.3	V
C_{VDD5V}	5V bias LDO output capacitor	0.33	µF
		6.3	V
C_{VDD1P8}	1.8V bias LDO output capacitor	0.33	µF
		6.3	V
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Operating Temperature Range	-40 to 140	°C

5. 4-layers PCB, air velocity = 0 m/s. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Electrical Characteristics

Unless otherwise noted, the *Min* and *Max* specs are applied over the recommended operation temperature range of -40°C to +85°C and V_{RECT} = 3.6V to 10V. Typical values are specified at T_A = +25°C with V_{RECT} = 6V.

Supply Specifications (IN)

Symbol	Description	Conditions	Min	Typ	Max	Units
Thermal Shutdown Specifications						
T_{J_SHDN}	IC Junction Thermal Shutdown	T_J rising threshold Hysteresis		140 20		°C °C
Thermal Shutdown Specifications						
R_{ON_CMA}	CMA1, CMA2 On Resistance	I_{CMA} = 200mA		1		W
I_{CMA_LK}	CMA1, CMA2 Leakage Current	V_{CMA} = 10V		1		µA

Supply, Bias & Power Selector Specifications (VRECT, VBAT, VDD5V, VDD1P8)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RECT}	VRECT Operating Range[6]		3.6		10	V
V_{UVP_RECT}	VRECT Under-Voltage Lockout Protection	Rising threshold Hysteresis	2.9	3.2 250		V mV
I_{VRECT}	VRECT No-Load Supply Current	Enabled, $\overline{EN}$ = 0, V_{RECT} = 6.0V Shutdown, $\overline{EN}$ = 1, V_{RECT} = 6.0V		10 100		mA µA
V_{DD5V}	VDD5V Output Voltage register 0xE2 = 0x02	V_{RECT} = 3.6V[6] V_{RECT} = 6.0V[6] V_{RECT} = 10V	 4.28 4.28	3.55 4.38 4.38	 4.48 4.48	V V V
V_{DD1P8}	VDD1P8 Output Voltage register 0xE6 = 0x80	V_{RECT} = 3.6V[6] V_{RECT} = 6.0V[6] V_{RECT} = 10V	1.70 1.70 1.70	1.75 1.75 1.75	1.80 1.80 1.80	V V V
f_{clk}	Internal clock frequency		-2%	4	+2%	Mhz

Logic Pin Specifications ($\overline{EN}$, $\overline{INT}$, POK, CHG)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High ($\overline{EN}$)		1.2			V
V_{IL}	Input Logic Low ($\overline{EN}$)				0.4	V
I_{I_LK}	Input Logic Leakage ($\overline{EN}$)	T_A = 25°C, V_I = 5V	-1	±0.01	1	µA
V_{OL}	Output Logic Low ($\overline{INT}$, POK, CHG)	I_{O_SINK} = 1mA			0.4	V
I_{O_LK}	Output Logic Leakage ($\overline{INT}$, POK, CHG)	TA = 25°C, VO = 5V		0.01	1	µA

(continued next page)

6. These electrical parameters are Guaranteed by Characterization (GBC) and/or Guaranteed by Design (GBD).

Electrical Characteristics (continued)

Unless otherwise noted, the *Min* and *Max* specs are applied over the recommended operation temperature range of -40°C to +85°C and V_{RECT} = 3.6V to 10V. Typical values are specified at T_A = +25°C with V_{RECT} = 6.0V.

I²C Compatible Interface Specifications (SCL, SDA)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RECT}	VRECT Operating Range[6]		3.6		10	V
V_{IL}	Input Logic Low Threshold				0.4	V
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
t_1	SCL clock period[6]		2.5			µs
t_2	Data in setup time to SCL high[6]		100			ns
t_3	Data out stable after SCL low[6]		0			ns
t_4	SDA low setup time to SCL low (Start)[6]		100			ns
t_5	SDA high hold time after SCL high (Stop)[6]		100			ns

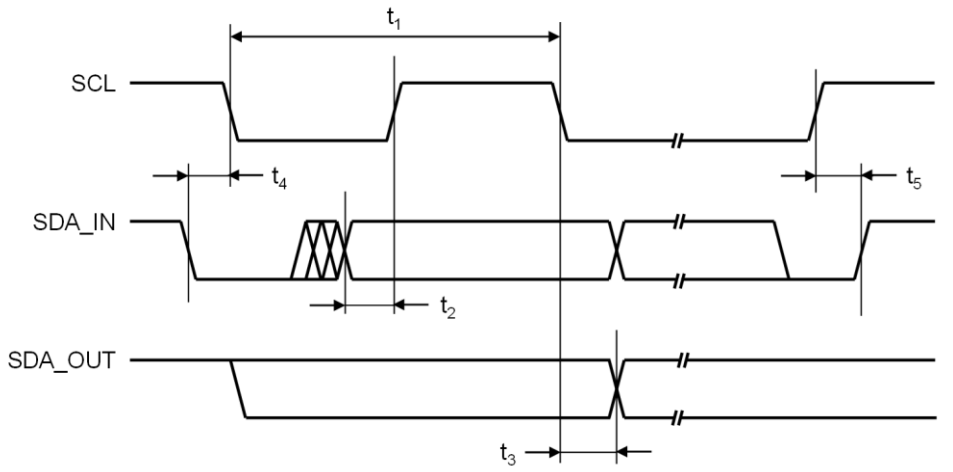


Figure 1. I²C Compatible Interface Timing Diagram

Electrical Characteristics (continued)

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C and V_{IN} = 5V.

OVP/LDO Specifications (VRECT to VSYS)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RECT}	VRECT Operating Range		3.6		10	V
V_{OVP_RECT}	VRECT Over-Voltage Protection	Rising threshold			28	V
I_{OCP_LDO}	Over-Current Protection			3		A
R_{ON_LDO}	OVP/LDO On-Resistance	VRECT to VSYS		0.5		Ω
I_{LK_LDO}	Off Leakage Current	V_{RECT} = 20V, V_{SYS} = 0V, T_A = 25°C V_{RECT} = 20V, V_{SYS} = 5V, T_A = 25°C		1 5		µA µA
C_{VLDO}	VRECT-to-VSYS Constant Voltage Regulation[6]	Setting range in 20mV steps Accuracy at T_A = 25°C Default Setting for KTE7200	3.2	 ±5 5.1	5.2	V % V
V_{SYS_LDR}	VSYS Load Regulation	LDO Mode		150		mV/A
V_{SYS_LNR}	VSYS Line Regulation	LDO Mode		5		mV/V
I_{SYS_PEAK}	Peak Current Capability[6]			1.5		A
$V_{RECT-SYS}$	VRECT to VSYS Dropout Voltage	I_{SYS} = 10mA; V_{RECT} droops 10% below the LDO regulated output value		100		mV

Functional Block Diagram

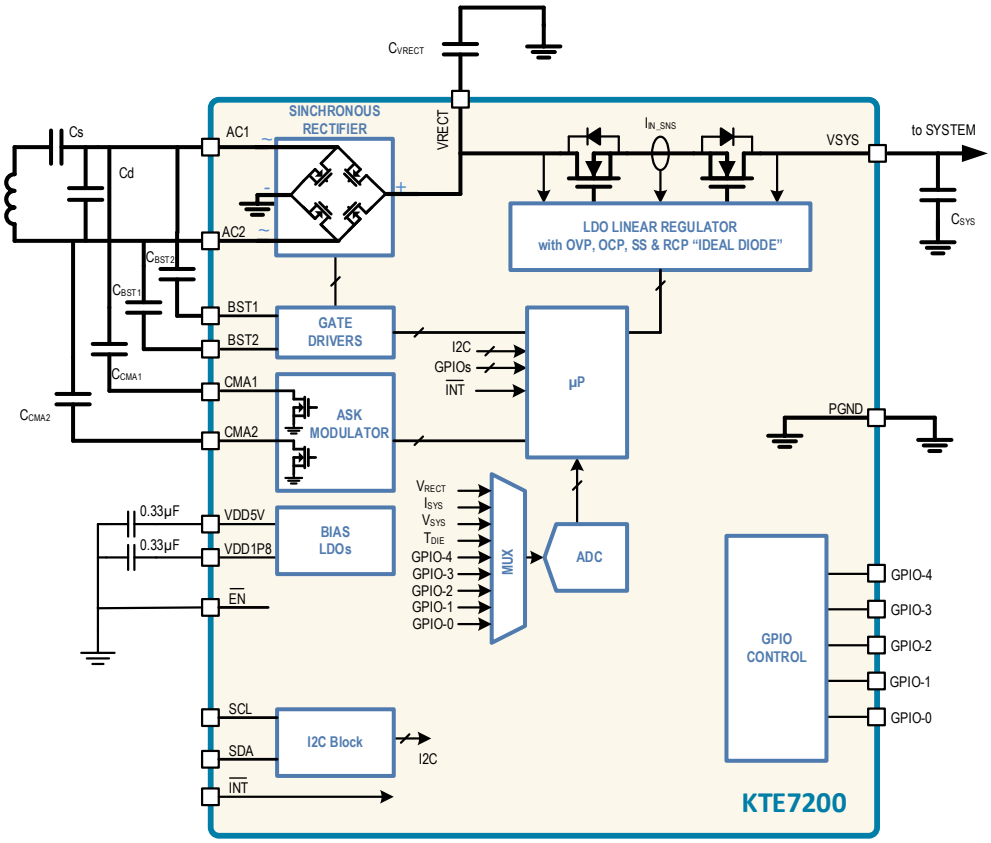


Figure 2. Functional Block Diagram

Functional Description

The KTE7200 integrates a 5W wireless power receiver that conforms to WPC/Qi v1.2 Baseline Power Profile (BPP) standards. AC power is coupled through the connected coil via magnetic induction.

Full-Bridge Synchronous Rectifier

The KTE7200 includes a full-bridge synchronous rectifier comprised of four low-RDSON MOSFET switches for high-efficiency AC-to-DC power conversion. The AC input to the rectifier is at pins AC1 and AC2, while the DC output is from pins VRECT to PGND. The rectified DC voltage and energy are stored on the off-chip capacitors connected to the VRECT pin. The rectifier's inputs, MOSFETs, and output are rated to 26V absolute maximum for robust and reliable performance.

Proprietary Overvoltage Protection

Proprietary overvoltage protection precisely limits the rectifier output to protect the KTE7200 during transient events, such as when dynamically moving the receiver coil on the transmitter pad. Conventional solutions rely upon external bulk capacitors or ISINK resistors to dissipate extra energy and prevent excessive voltage. Instead, the KTE7200 utilizes a proprietary solution that is more robust, does not require any external components, and precisely limits VRECT to 25V.

Low-dropout Linear Regulator

The KTE7200 integrates a high-power, low-dropout (LDO) linear regulator that provides a stable and accurate DC output for system loads up to 0.7A while output voltage is 5.1V. The LDO includes important features such as over-voltage protection (OVP), and over-current protection (OCP).

- **Output Short-Circuit Protection (SCP)** - The high-power LDO is rated to support up to 1A loads. For output over-load and short-circuit conditions, the LDO includes short-circuit protection.
- **Output Under-Voltage Protection (UVP)** - The KTE7200 includes under-voltage protection when VOUT falls below 3.0V.
- **Output Over-Voltage Protection (OVP)** - The KTE7200 includes output over-voltage protection that enables a 10mA current sink at VSYS whenever the output voltage exceeds its nominal regulation set-point by more than 15%. The current sink is disabled when the output voltage returns to within 10% above nominal. This reduces VSYS voltage soar during dynamic load conditions or when the transmitter-to-receiver distance is physically modulated.

The LDO's input is internally connected to the rectifier's output at VRECT, while the regulated output is at VSYS. Communications from the KTE7200 back to the WPC transmitter automatically adjust the transmitter's output power such that the VRECT maintains sufficient headroom for the LDO.

Die Temperature Monitor

The die temperature implements fail-safe thermal shutdown during fault or excessive heat conditions.

Analog-to-Digital Converter (ADC)

Analog-to-Digital Converter (ADC) – The ADC has an input multiplexor (MUX) to sense various voltages, currents, and temperatures.

Embedded Microcontroller and OTP Memory

The KTE7200 includes an embedded microcontroller with 8K bytes of one-time programmable (OTP) memory and firmware.

Optional $\overline{EN}$ Input

The KTE7200 has an optional $\overline{EN}$ logic input pin to enable and disable the IC. Because the KTE7200 is powered from its wireless input, simply connect the $\overline{EN}$ pin to ground for automatic enable/disable operation whenever the receiver is placed on a transmitter or removed, respectively. In applications that require to disable the wireless charger portion for various reasons while the receiver is on the transmitter, optionally drive the $\overline{EN}$ pin with logic 1 for shutdown mode.

Optional $\overline{EN}$ Flag

The KTE7200 includes an optional I^2C serial interface and open-drain interrupt flag intended for use in customized and future versions of the KTE7200. Consult an authorized Kinetic Technologies representative for more information.

GPIO Pins and Optional Configuration

The KTE7200 has five GPIO pins, GPIO0 through GPIO4, which may be used for optional configuration.

Each GPIO is configurable to support a precision internal 20µA current source. Depending upon the application, GPIOs may be left floating (no connect), shorted to ground, or connected to an external setting resistor.

Standard Firmware

The standard firmware in the KTE7200 aligns with the WPC/Qi v1.2 Baseline Power Profile (BPP) standards and can operate autonomously without intervention from the system's applications processor.

Custom Firmware Development

For high-volume applications, Kinetic Technologies may develop customized firmware to meet specialized customer needs. Consult an authorized Kinetic Technologies representative for more information.

Application Schematic

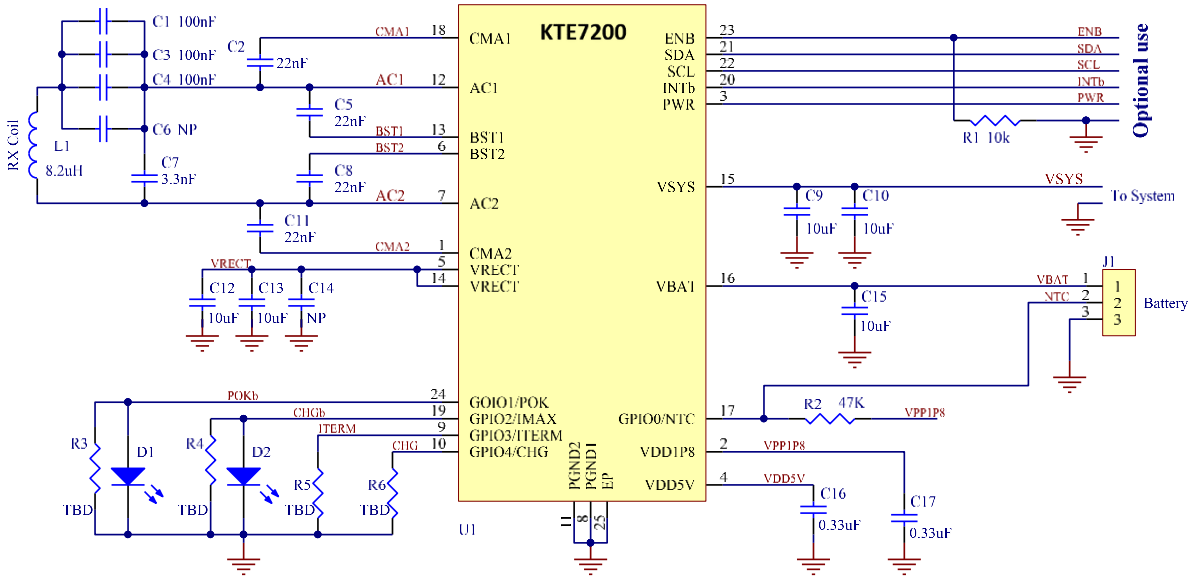


Figure 3. Application Schematic

Bill of Materials

Item	Quantity	Reference	Description	Value	Manufacturer
1	4	C1, C3, C4, C6	CAP CER 0.1µF 50V X5R	100nF	Murata
2	2	C2, C5, C8, C11	CAP CER 0.022µF 50V X7R	22nF	Yageo
3	1	C7	CAP CER 3300PF 50V X7R	3.3nF	Yageo
5	3	C12, C13, C14	CAP CER 10µF 25V X5R	10µF	Murata
5	2	C9, C10, C15	CAP CER 10µF 16V X5R	10µF	Murata
6	2	C16, C17	CAP CER 1µF 10V X5R	1µF	Yageo
7	2	D1, D2	LED GREEN CLEAR 0603 SMD	Green	Any
8	1	R47	RES 47KΩ 1% 1/4W 0402	47K	Any
9	1	R1	RES 10KΩ 1% 1/4W 0402	10K	Any
10	4	R3, R4, R5, R6		TBD	Any
11	1	U1	Wireless power receiver/charger	KTE7200	Kinetic Technologies
12	1	RX coil	WPC receive coil, L = 8.2µH, ACR = 0.22Ω	8	1

External Component Selection

Coil Selection

Select a coil that meets the needs of the application. Consider form-factor, series resistance and inductance. Larger diameter coils generally perform better. Use a shield that is sufficient to prevent magnetic flux from interacting with metallic objects elsewhere in the application. To obtain WPC/Qi certification, the receiver must work with all WPC/Qi certified transmitters.

Capacitor Selection

Ceramic capacitors with X5R, X6S, or X7R ratings are recommended due to their low ESR, low ESL, low temperature coefficients, and small physical sizes. Consider the voltage rating, size, and DC bias derating characteristic of the capacitor.

Cs and Cd Capacitor Selection

Choose Cs and Cd per the guidelines set forth by the WPC/Qi specifications. Use small ceramic capacitors with 50V or more rating.

Select the value of Cs for primary resonance at 100kHz:

$$f_s = \frac{1}{2\pi\sqrt{L'_s C_s}} = 100kHz$$

where L'S is the self-inductance of the coil when placed and aligned on the interface surface of a power transmitter.

Select the value of Cd for secondary resonance at 1MHz:

$$f_d = \frac{1}{2\pi\sqrt{L_s\left(\frac{1}{C_s}+\frac{1}{C_d}\right)^{-1}}} = 1MHz$$

where L_S is the self-inductance of the coil when away from the interface surface of a power transmitter but including any "friendly" magnetic material that is part of the receiver design.

C_{BSTn} Capacitor Selection

Choose ceramic boost capacitors with voltage rating of 50V and 22nF nominal capacitance. Typically, 0402 (1005M) case-size is sufficient.

C_{CMAn} Capacitor Selection

Choose ceramic modulation capacitors with voltage rating of 50V and 22nF nominal capacitance. Typically, 0402 (1005M) case-size is sufficient.

C_{RECT} Capacitor Selection

Choose ceramic rectifier output capacitor(s) with voltage rating of 25V or more, and 4.7µF to 22µF total nominal capacitance. Typically, two 10µF capacitors in parallel, each with 0603 (1608M) case-size or larger, is a good choice. Larger values and larger case-size provide more effective capacitance when considering the DC bias derating characteristic of the capacitor.

C_{SYST} Capacitor Selection

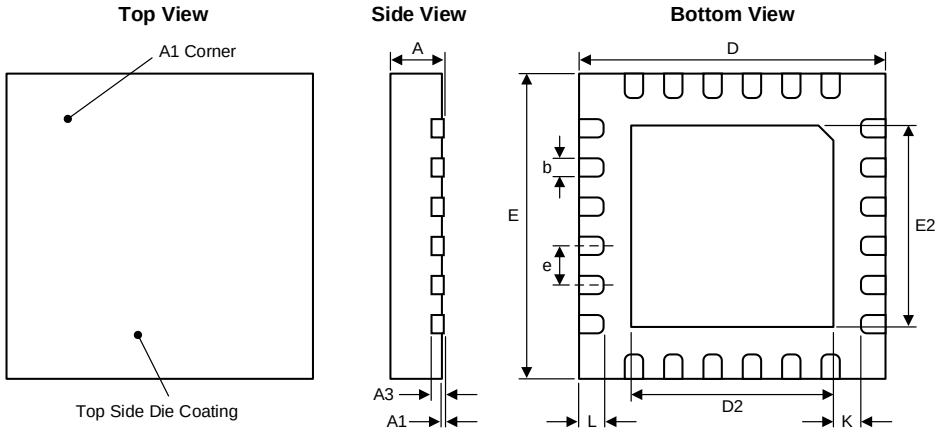
Choose ceramic VSYS output capacitor(s) with voltage rating of 6.3V or more and 10µF total nominal capacitance or more. Larger values and larger case-size provide more effective capacitance when considering the DC bias derating characteristic of the capacitor.

C_{VDD5V} and C_{VDD1P8} Capacitor Selection

Choose ceramic VDD5V and VDD1P8 output capacitors with voltage rating of 6.3V or more and 1µF nominal capacitance each. Typically, 0402 (1005M) case-size is sufficient.

Packaging Information

TQFN55-24 (5.00mm x 5.00mm x 0.75mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.25	0.30	0.35
D		5.00 BSC	
D2	3.25	3.30	3.35
E		5.00 BSC	
E2	3.25	3.30	3.35
e		0.65 BSC	
K	0.20	–	–
L	0.35	0.40	0.45

Recommended Footprint