a module solution provider

WB2072-00

Bluetooth® Low Energy

Wireless MCU Module

ST BlueNRG-355AC Solution

Datasheet

Revision 0.1

Prepared By	Reviewed By	Approved By

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1. OVERVIEW

The certified WB2072-00 module from JORJIN is a wireless MCU module targeting Bluetooth 5.2 low energy applications. This module is based on ST BlueNRG-355AC wireless MCU QFN-32 package chip.

The module is a cost-effective, ultralow power, 2.4-GHz RF devices. Very low active RF and MCU current and low-power mode current consumption provide excellent battery lifetime and allow for operation on small coin cell batteries and in energy-harvesting applications.

1.1. General Features

- STMicroelectronics BlueNRG-LP, 32MHz & 32.768KHz crystals, DC2DC, and chip antenna on a single module.
- Built-in STMicroelectronics BlueNRG-LP, 5x5mm QFN32 (20 GPIOs)
- 2.4-GHz RF Transceiver and Integrated Antenna.
- Bluetooth Low Energy system-on-chip supporting Bluetooth 5.2 specifications:
  - 2 Mbps data rate
  - Long Range (Coded PHY)
  - Advertising Extensions
  - Channel Selection Algorithm #2
  - GATT caching
- Data rate supported: 2 Mbps, 1 Mbps, 500 kbps and 125 kbps
- Operating supply voltage: from 1.7 to 3.6 V
- High performance and ultra-low power Cortex-M0+ 32-bit, 64 MHz
- 256KB Flash, 64KB SRAM, 1KB OTP, 7KB ROM, MPU
- Dynamic current consumption: 18 µA/MHz
- Extensive peripheral set: 2 x SPI / I2S, 1x SPI, 2 x I^2C, 1 x USART, 1 x UART, 6 x PWM, 1 x PDM, 1 x 12-bit ADC
- Supply and reset management
  - High efficiency embedded SMPS step-down converter
  - Ultra-low-power Power-On-Reset (POR) and Power-Down-Reset (PDR)
  - Programmable Voltage Detector (PVD)
- Embedded UART bootloader
- Enhanced security mechanisms such as:
  - Flash read/write protection
  - SWD access can be disabled
  - Secure bootloader
- LGA-42pins package.

- Dimension 15mm(L) x 11mm(W) x 2.6mm(H)
- Temperature range: -40 ℃ to +85 ℃ temperature range
- RoHS Compliance
- Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations
  - ETSI EN 300 328 (Europe)
  - FCC CFR47 Part 15 (US)
  - IC RSS-247 (Canada)
  - ARIB STD-T66 (Japan)
  - NCC LP0002 (Taiwan)
  - AS/NZS 4268 (Australia/New Zealand)
  - KN 301 489 (South Korea)
- Development support
  - Serial wire debug (SWD)
  - 4 breakpoints and 2 watchpoints
- All packages are ECOPACK®2 compliant.

1.2. Applications

- Industrial
- Home and Industrial automation
- Smart Lighting
- Fitness, wellness and sports
- Healthcare, consumer medical
- Security/proximity
- Remote Control
- Assisted Living
- Mobile Phone peripherals
- PC peripherals

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram

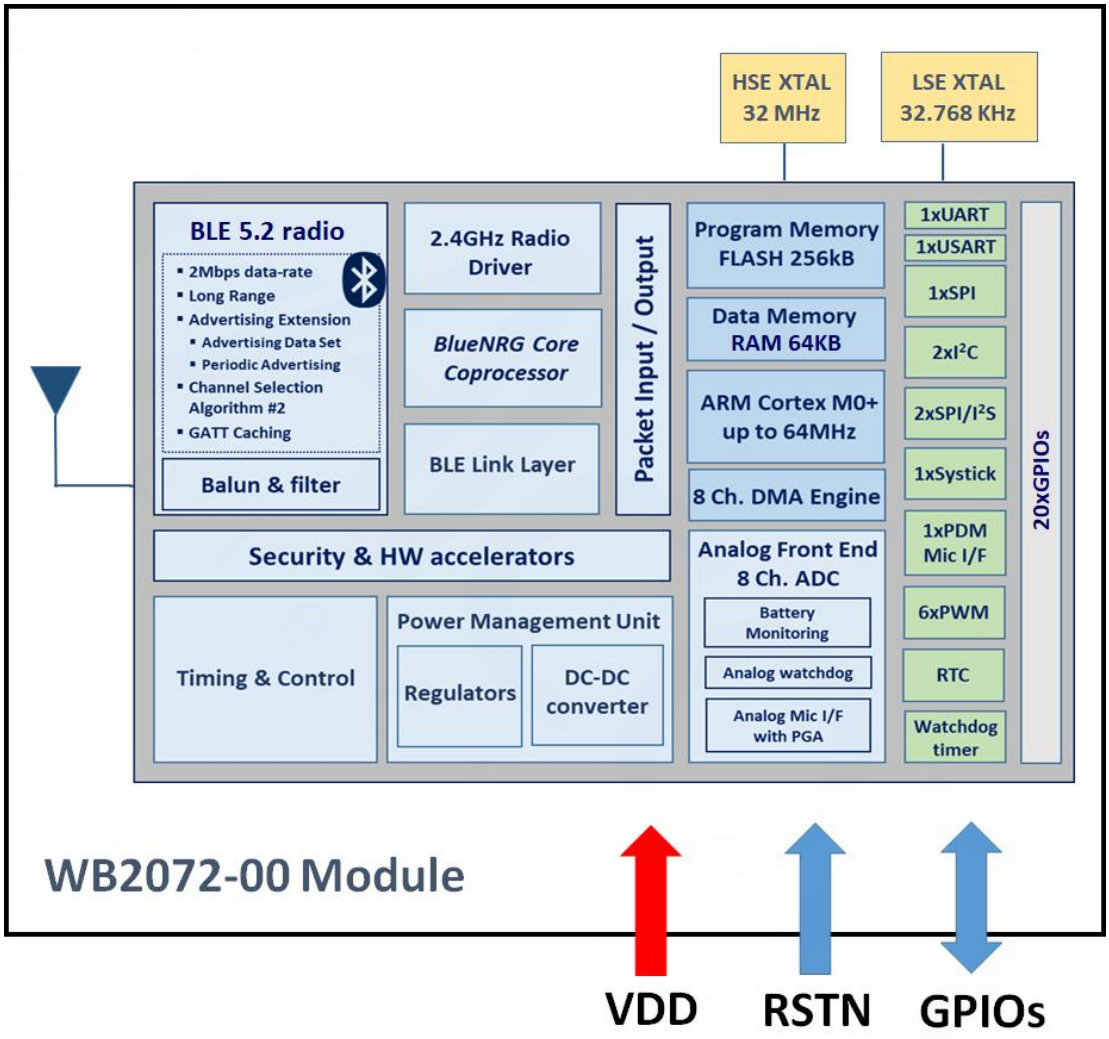


Figure 1 *– Module block diagram*

3. MODULE OUTLINE

3.1. Signal Layout (Top View)

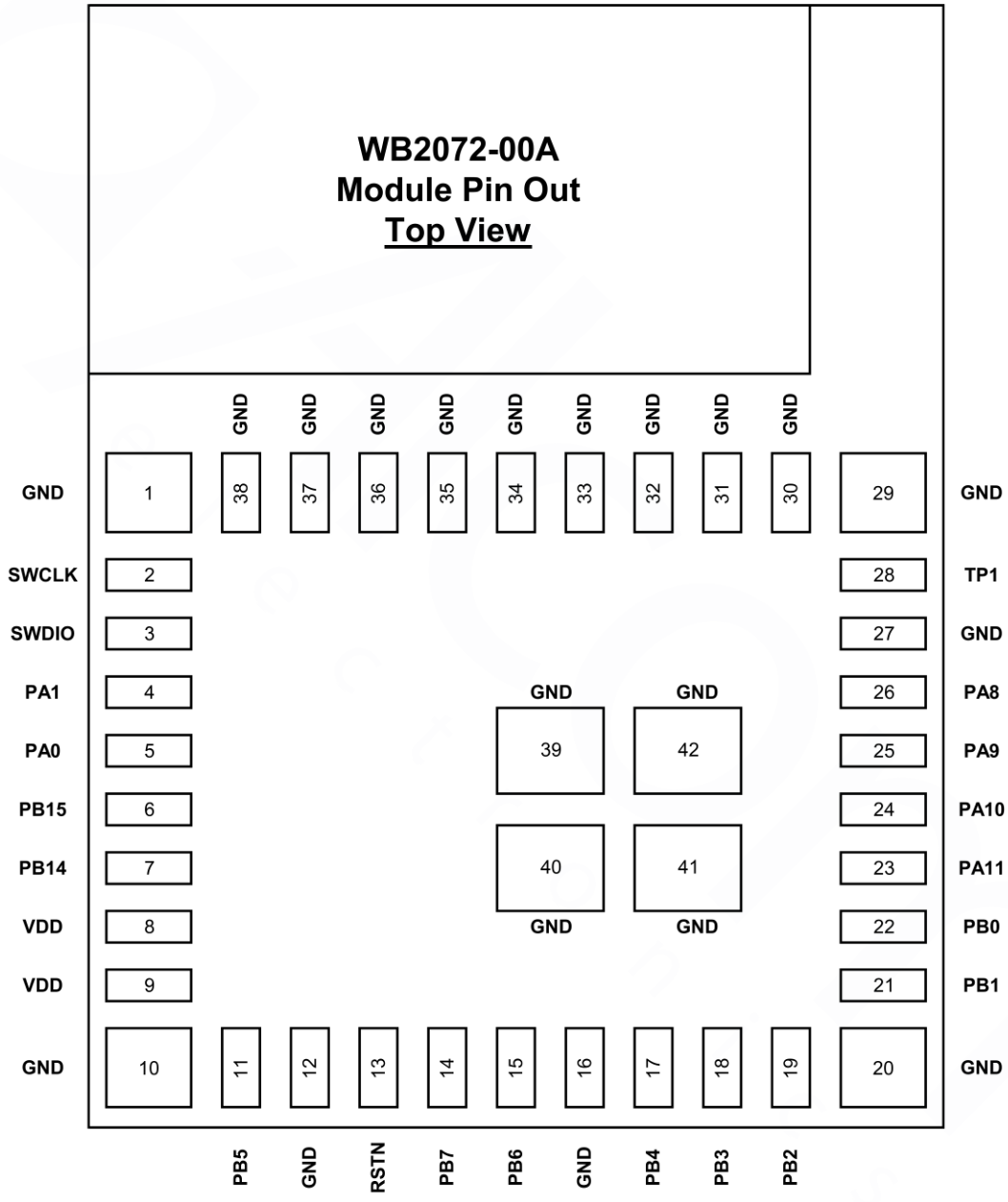


Figure 2 *–Pinout top view*

3.2. Pin Description

Table1 *–Pin Description*

Pin No.	Pin Name	Type	Description
1	GND	S	Ground
2	BLE_SWCLK	I/O	BLE_SWCLK to CMSIS-DAP for programming
3	BLE_SWDIO	I/O	BLE_SWDIO to CMSIS-DAP for programming
4	PA1	I/O	I2C1_SDA, SPI2_MISO, USART_TX, TIM1_CH4
5	PA0	I/O	I2C1_SCL, USART_CTS, SPI2_MCK, TIM1_CH3
6	PB15	I/O	I2C1_SMBA, TX_SEQUENCE, MCO, TIM1_CH4N, TIM1_CH6, USART_TX
7	PB14	I/O	SPI1_MOSI, I2C2_SDA, TIM1_ETR, TIM1_CH3N, TIM1_CH5, USART_RX
8	VDD_MOD	S	1.7-3.6 battery voltage input
9	VDD_MOD	S	1.7-3.6 battery voltage input
10	GND	S	Ground
11	PB5	I/O	LPUART_RX, SPI2_MOSI, PDM_CLK
12	GND	S	Ground
13	BLE_RSTN	I/O	Reset, active-low. No internal pull-up. Built-in 0.1uF capacitor to GND.
14	PB7	I/O	I2C2_SDA, SPI2_SCK, LPUART_RX, TIM1_CH2
15	PB6	I/O	I2C2_SCL, SPI2_NSS, LPUART_TX, TIM1_CH1
16	GND	S	Ground
17	PB4	I/O	LPUART_TX, SPI2_MISO, PDM_DATA
18	PB3	I/O	USART_CTS, LPUART_TX, TIM1_CH4
19	PB2	I/O	USART_RTS_DE, PDM_DATA, TIM1_CH3
20	GND	S	Ground
21	PB1	I/O	SPI1_NSS, PDM_CLK, TIM1_ETR
22	PB0	I/O	USART_RX, LPUART_RTS_DE, TIM1_CH2N
23	PA11	I/O	MCO, SPI1_NSS, SPI3_MOSI, TIM1_CH6
24	PA10	I/O	LCO, SPI1_MISO, SPI3_MCK, TIM1_CH5
25	PA9	I/O	USART_TX, SPI1_SCK,RTC_OUT, SPI3_NSS,TIM1_CH4
26	PA8	I/O	USART_RX, SPI1_MOSI, SPI3_MISO, TIM1_CH3
27	GND	S	Ground
28	TP1	I/O	NC
29~38	GND	S	Ground
39~42	GND	S	Ground

4. MODULE SPECIFICATIONS

4.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to ground (GND).

4.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the following standard conditions:

- Ambient temperature is T_A = 25 °C
- Supply voltage is VDD: 3.3 V
- System clock frequency is 32 MHz (clock source HSI)
- SMPS clock frequency is 4 MHz

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, VDD = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

4.2. Absolute maximum ratings and thermal data

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2 *- Voltage characteristics*

Symbol	Ratings	MIN	MAX	Unit

VDD_MOD	DC-DC converter supply voltage input	-0.3	+3.9	V
PA0 to PA15, PB0 to PB15	DC voltage on digital input/output pins	-0.3	+3.9	V

Note: All the main power and ground pins must always be connected to the external power supply, in the permitted range.

Table 3 *- Current characteristics*

Symbol	Ratings	MAX	Unit
ΣIV_{DD}	Total current into sum of all VDD power lines (source)	130	mA
ΣIV_{GND}	Total current out of sum of all ground lines (sink)	130	
$IV_{DD(PIN)}$	Maximum current into each VDD power pin (source)	100	
$IV_{GND(PIN)}$	Maximum current out of each ground pin (sink)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins	100	
	Total output current sourced by sum of all I/Os and control pins	100	

Table 4 *- Thermal characteristics*

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-40 to +125	℃
T_J	Maximum junction temperature	125	℃

4.3. Operating conditions

4.3.1 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

***Table 5**- Current consumption*

Symbol	Parameter	Conditions	Typ.	Unit
I_{DD}(RUN)	Supply current in RUN mode	fHCLK = 64 MHz All peripherals disabled	2.40	mA
		fHCLK = 32 MHz All peripherals disabled	1.98	
		fHCLK = 16 MHz All peripherals disabled	1.62	
I_{DD}(DEEPSTOP)	Supply current in DEEPSTOP (1)	Timer OFF	0.65	µA
		Timer source LSI	1.25	
		Timer source LSI RTC ON	1.30	
		Timer source LSI IWDG ON	1.27	
		Timer source LSI RTC and IWDG ON	1.33	
		Timer source LSE	1.00	
		Timer source LSE RTC ON	1.06	
		Timer source LSE IWDG ON	1.02	
		Timer source LSE RTC and IWDG ON	1.07	
I_{DD}(SHUTDOWN)	Supply current in SHUTDOWN		0.12	µA
I_{DD}(RST)	Current under reset condition		1.34	mA

(1) The current consumption in DEEPSTOP is measured considering the entire SRAM retained.

***Table 6**- Peripheral current consumption at VDD = 3.3 V, sysclk at 32 MHz, SMPS on*

Parameter	Test conditions	Typ.	Unit
ADC		80	µA
DMA		39	
GPIOA		2	
GPIOB		2	
I2C1		40	
I2C2		39	

I2S2	Peripheral clock at 32 MHz	46	µA
I2S3	Peripheral clock at 32 MHz	47	
IWDG		11	
LPUART		52	
PKA		50	
RNG		64	
RTC		14	
SPI1		35	
SPI2	Peripheral clock at 16 MHz	40	
SPI3	Peripheral clock at 16 MHz	42	
Systick		8	
TIM1		248	
USART		81	
SYSCFG		33	
THSENS		301	
CRC		9	

4.3.2 General operating conditions

***Table 7**- General operating conditions*

Symbol	Parameter	Conditions	MIN	MAX	Unit
f_{HCLK}	Internal AHB clock frequency		1	64	MHz
f_{PCLK0}	Internal APB0 clock		1	64	
f_{PCLK1}	Internal APB1 clock		1	64	
f_{PCLK2}	Internal APB2 clock frequency		16	32	
V_{DD}	Standard operating voltage		1.7	3.6	V
V_{FBSMPS}	SMPS feedback voltage		1.4	3.6	
V_{DDRF}	Minimum RF voltage		1.7	3.6	
V_{IN}	I/O input voltage		-0.3	VDD+0.3	
P_D	Power dissipation at T_A =85 °C(1)			30	mW
T_A	Ambient temperature	Maximum power dissipation	-40	85	℃
T_J	Junction temperature range		-40	85	

(1) T_A cannot exceed the T_J max.

4.3.3 RF general characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

***Table 8**- Bluetooth Low energy RF general characteristics*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{RANGE}	Frequency range(1)		2400		2483.5	MHz
RF_{CH}	RF channel center frequency(1)		2402		2480	MHz
PLL_{RES}	RF channel spacing(1)			2		KHz
Δ F	Frequency deviation(1)			250		KHz
Δ f1	Frequency deviation average(1)		450		550	KHz
C_{Fdev}	Center frequency deviation(1)	During the packet and including both initial frequency offset and drift			±150	KHz
Δ fa	Frequency deviation Δf2 (average) / Δ f1 (average) (1)		0.80			
R_{gfsk}	On air data rate(1)		1		2	Mbps
STacc	Symbol time accuracy(1)				±50	ppm
MOD	Modulation scheme		GFSK			
BT	Bandwidth-bit period product			0.5		
Mindex	Modulation index(1)		0.45	0.5	0.55	
PMAX	Maximum Output	At antenna connector, VSMPS = 1.9 V, LDO code	6.3	7	7.7	dBm
PMIN	Minimum Output	At antenna connector		-20		dBm
PRFC	RF power accuracy	@ 27°C		±1.5		dB
		All temperatures		±2.5		

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

4.3.4 RF transmitter characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

***Table 9**- Bluetooth Low Energy RF Transmitter characteristics at 1 Mbps not coded*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit

P_{BW1M}	6 dB Bandwidth for modulated carrier	Using resolution bandwidth of 100kHz	550			KHz
$P_{RF1, 1 Ms/s}$	In-band emission at ±2MHz(1)	Using resolution bandwidth of 100 kHz and average detector			-20	dBm
$P_{RF2, 1 Ms/s}$	In-band emission at ±[3+n]MHz, where n=0,1,2.. (1)	Using resolution bandwidth of 100 kHz and average detector			-30	dBm
P_{SPUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector			-41	dBm
$Freq_{drift}$	Frequency drift	Integration interval #n – integration interval #0, where n=2,3,4..k	-50		+50	KHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #1 – integration interval #0	-23		+23	KHz
$IntFreq_{drift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-5), where n=6,7,8..k	-20		+20	KHz
$DriftRate_{max}$	Maximum drift rate(1)	Between any two 10-bit groups separated by 50μs	-20		+20	KHz/50μs
Z_{RF1}	Optimum RF load (Impedance at RF1 pin)	@ 2440 MHz		40		Ω

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

***Table 10**- Bluetooth Low Energy RF Transmitter characteristics at 2 Mbps not coded*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW1M}	6 dB Bandwidth for modulated carrier	Using resolution bandwidth of 100kHz	670			KHz
$P_{RF1, 2Ms/s}$	In-band emission at ±4MHz(1)	Using resolution bandwidth of 100kHz and average detector			-20	dBm
$P_{RF2, 2Ms/s}$	In-band emission at ±5MHz(1)	Using resolution bandwidth of 100kHz and average detector			-20	dBm
$P_{RF3, 2Ms/s}$	In-band emission at ±[6+n]MHz, where n=0,1,2.. (1)	Using resolution bandwidth of 100kHz and average detector			-30	dBm
P_{SPUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector			-41	dBm

$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=2,3,4..k	-50		+50	KHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #1 – integration interval #0	-23		+23	KHz
$IntFreq_{drift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-5), where n=6,7,8..k	-20		+20	KHz
$DriftRate_{max}$	Maximum drift rate(1)	Between any two 10-bit groups separated by 50μs	-20		+20	KHz/50μs
Z_{RF1}	Optimum RF load (Impedance at RF1 pin)	@ 2440 MHz		40		Ω

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

***Table 11**- Bluetooth Low Energy RF Transmitter characteristics at 1 Mbps LE coded (S=8)*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW}	6 dB Bandwidth for modulated carrier	Using resolution bandwidth of 100kHz	500			KHz
$P_{RF1, LE coded}$	In-band emission at ±2MHz(1)	Using resolution bandwidth of 100kHz and average detector			-20	dBm
$P_{RF2, LE coded}$	In-band emission at ±[3+n]MHz, where n=0,1,2.. (1)	Using resolution bandwidth of 100kHz and average detector			-30	dBm
P_{SPUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector			-41	dBm
$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=1,2,3..k	-50		+50	KHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #3 – integration interval #0	-19.2		+19.2	KHz
$IntFreq_{drift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-3), where n=7,8,9..k	-19.2		+19.2	KHz
$DriftRate_{max}$	Maximum drift rate(1)	Between any two 16-bit groups separated by 48μs	-19.2		+19.2	KHz/48μs
Z_{RF1}	Optimum RF load (Impedance at RF1 pin)	@ 2440 MHz		40		Ω

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

4.3.5 RF receiver characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

***Table 12**- Bluetooth Low Energy RF receiver characteristics at 1 Msym/s uncoded*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-94		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source (Impedance at RF1 pin)	@ 2440 MHz		40		Ω
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal=-67dBm, PER < 30.8%		8		dBc
$C/I_{1\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 1MHz$	Wanted signal=-67dBm, PER < 30.8%		-1		dBc
$C/I_{2\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 2MHz$	Wanted signal=-67dBm, PER < 30.8%		-35		dBc
$C/I_{3\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal=-67dBm, PER < 30.8%		-47		dBc
C/I_{Image}	Image frequency Interference $f_{interference} = f_{image}$	Wanted signal=-67dBm, PER < 30.8%		-25		dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel to image frequency $f_{interference} = f_{image} \pm 1MHz$	Wanted signal=-67dBm, PER < 30.8%		-25		dBc
Out of Band Blocking (Interfering signal CW)						
C/I_{Block}	Interfering signal frequency 30MHz – 2000 MHz	Wanted signal=-67dBm, PER < 30.8%, Measurement resolution 10 MHz		5		dBm
C/I_{Block}	Interfering signal frequency 2003 MHz – 2399 MHz	Wanted signal=-67dBm, PER < 30.8%, Measurement resolution 3MHz		-5		dBm
C/I_{Block}	Interfering signal frequency 2484 MHz – 2997 MHz	Wanted signal=-67dBm, PER < 30.8%, measurement resolution 3MHz		-5		dBm
C/I_{Block}	Interfering signal frequency	Wanted signal=-67dBm, PER < 30.8%,		10		dBm

	3000 MHz – 12.75 GHz	measurement resolution 25MHz				
Intermodulation characteristics (CW signal at f1, BLE interfering signal at f2)						
P_IM(3)	Input power of IM interferer at 3 and 6 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-27		dBm
P_IM(-3)	Input power of IM interferer at -3 and -6 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-40		dBm
P_IM(4)	Input power of IM interferer at ±4 and ±8 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-32		dBm
P_IM(5)	Input power of IM interferer at ±5 and ±10 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-32		dBm

***Table 13**- Bluetooth Low Energy RF receiver characteristics at 2 Msym/s uncoded*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-91		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source (Impedance at RF1 pin)	@ 2440 MHz		40		Ω
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal=-67dBm, PER < 30.8%		8		dBc
$C/I_{2\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 2MHz$	Wanted signal=-67dBm, PER < 30.8%		-14		dBc
C/I_{4MHz}	Adjacent Interference $f_{interference} = f_{RX} \pm 4MHz$	Wanted signal=-67dBm, PER < 30.8%		-41		dBc
$C/I_{6\ MHz}$	Adjacent Interference f interference = f RX ± (6+2n) MHz [n = 0,1,2…]	Wanted signal=-67dBm, PER < 30.8%		-45		dBc
C/I_{Image}	Image frequency Interference $f_{interference} = f_{image\text{-}2M}$	Wanted signal=-67dBm, PER < 30.8%		-25		dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel to image	Wanted signal=-67dBm, PER <		-14		dBc

	frequency $f_{interference} = f_{image-2M} \pm 2MHz$	30.8%				
Out of Band Blocking (Interfering signal CW)						
C/I_{Block}	Interfering signal frequency 30MHz – 2000 MHz	Wanted signal=-67dBm, PER < 30.8%, Measurement resolution 10 MHz		5		dBm
C/I_{Block}	Interfering signal frequency 2003 MHz – 2399 MHz	Wanted signal=-67dBm, PER < 30.8%, Measurement resolution 3MHz		-5		dBm
C/I_{Block}	Interfering signal frequency 2484 MHz – 2997 MHz	Wanted signal=-67dBm, PER < 30.8%, measurement resolution 3MHz		-5		dBm
C/I_{Block}	Interfering signal frequency 3000 MHz – 12.75 GHz	Wanted signal=-67dBm, PER < 30.8%, measurement resolution 25MHz		10		dBm
Intermodulation characteristics (CW signal at f_1, BLE interfering signal at f_2)						
P_IM(6)	Input power of IM interferer at 6 and 12 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-27		dBm
P_IM(-6)	Input power of IM interferer at -6 and -12 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-30		dBm
P_IM(8)	Input power of IM interferer at ±8 and ±16 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-30		dBm
P_IM(10)	Input power of IM interferer at ±10 and ±20 MHz distance from wanted signal	Wanted signal=-64dBm, PER < 30.8%		-28		dBm

***Table 14**- Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded (S=2)*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-97		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source (Impedance at RF1 pin)	@ 2440 MHz		40		Ω
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO-channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal=-79dBm, PER < 30.8%		2		dBc

$C/I_{1\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 1MHz$	Wanted signal=-79dBm, PER < 30.8%		-5		dBc
$C/I_{2\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 2MHz$	Wanted signal=-79dBm, PER < 30.8%		-38		dBc
$C/I_{3\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal=-79dBm, PER < 30.8%		-50		dBc
C/I_{Image}	Image frequency Interference $f_{interference} = f_{image}$	Wanted signal=-79dBm, PER < 30.8%		-30		dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel to image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal=-79dBm, PER < 30.8%		-34		dBc

***Table 15**- Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded (S=8)*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-100		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source (Impedance at RF1 pin)	@ 2440 MHz		40		Ω
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal=-79dBm, PER < 30.8%		1		dBc
$C/I_{1\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 1MHz$	Wanted signal=-79dBm, PER < 30.8%		-4		dBc
$C/I_{2\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 2MHz$	Wanted signal=-79dBm, PER < 30.8%		-39		dBc
$C/I_{3\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal=-79dBm, PER < 30.8%		-53		dBc
C/I_{Image}	Image frequency Interference $f_{interference} = f_{image}$	Wanted signal=-79dBm, PER < 30.8%		-33		dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel to image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal=-79dBm, PER < 30.8%		-32		dBc

4.3.6 Embedded reset and power control block characteristics

***Table 16**- Embedded reset and power control block characteristics*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{RSTTEMPO}$	Reset temporization after PDR is detected	VDD rising			500	us
VPDR	Power-down reset threshold			1.63		V
VPVD0	PVD threshold 0	Falling edge		2.02		V
VPVD1	PVD threshold 1	Falling edge		2.17		
VPVD2	PVD threshold 2	Falling edge		2.33		
VPVD3	PVD threshold 3	Falling edge		2.49		
VPVD4	PVD threshold 4	Falling edge		2.61		
VPVD5	PVD threshold 5	Falling edge		2.78		
VPVD6	PVD threshold 6	Falling edge		2.87		

4.3.7 Wakeup time from low power modes

The wakeup times reported are the latency between the event and the execution of the instruction.

The device goes in Low-power mode after the WFI (Wait For Interrupt) instruction.

***Table 17**- Low power mode wakeup timing*

Symbol	Parameter	Conditions	Typ.	Unit
$T_{WUDEEPSTOP}$	Wakeup time from DEEPSTOP mode to RUN mode	Wakeup from GPIO. Boot in Flash memory	110	µs

4.3.8 High speed crystal requirements

High speed external oscillator must be supplied with an external 32 MHz crystals that are specified for a 6 to 8pF loading capacitor. The BlueNRG-LP include internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one.

These internal load capacitors, are made by a fixed one, in parallel with a 6-bit binary weighted capacitor bank. Thanks to low CL step size (LSB is typically 0.07pF), very fine Crystal tuning is possible. With typical XTAL sensitivity of -14ppm/pF, it is possible to trim a 32MHz crystal, with a resolution of 1ppm

The requirements for the external 32 MHz crystal are reported in the table below.

***Table 18**- HSE crystal requirements*

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Oscillator frequency			32		MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.			±50	ppm
ESR	Equivalent series resistance				100	Ω
P_D	Drive level				100	µW
CL	HSE Crystal load capacitance	27 °C, typical corner GMCONF = 3	5(1)	7(2)	9.2(3)	pF
CLstep	HSE crystal load capacitance LSB value	27 °C, GMCONF = 3 XOTUNE code between 32 and 33		0.07		pF

(1) XOTUNE programed at minimum code = 0

(2) XOTUNE programed at center code = 32

(3) XOTUNE programed at maximum code = 63

4.3.9 Low speed crystal requirements

The low speed clock can be supplied with an external 32.768 kHz crystal oscillator. The requirements for the external 32.768 kHz crystal are reported in the table below.

***Table 19**- LSE crystal requirements*

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal Frequency			32.768		KHz
ESR	Equivalent series resistance				90	KΩ
P_D	Drive level				0.1	µW

4.3.10 High speed ring oscillator characteristics

***Table 20**- HSI oscillator characteristics*

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal Frequency			64		MHz

4.3.11 Low speed ring oscillator characteristics

***Table 21**- LSI oscillator characteristics*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal Frequency	Trimmed by software		33		KHz
$\Delta F_{RO\_\Delta T}/F_{RO}$	Frequency spread vs. temperature	Standard deviation		140		ppm/℃

4.3.12 PLL characteristics

Characteristics measured over recommended operating conditions unless otherwise specified.

***Table 22**- PLL characteristics*

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PN_{SYNTH}	RF carrier phase noise	At ±1MHz offset from carrier (measured at 2.4GHz)		-110		dBc/Hz
		At 2.4GHz ±3MHz offset from carrier (measured at 2.4GHz)		-114		dBc/Hz
		At 2.4GHz ±6MHz offset from carrier (measured at 2.4GHz)		-128		dBc/Hz
		At ±25MHz offset from carrier		-135		dBc/Hz
$LOCK_{TIMETX}$	PLL lock time to TX	With calibration @2.5 ppm		150		µs
$LOCK_{TIMERX}$	PLL lock time to RX	With calibration @2.5 ppm		110		µs
$LOCK_{TIMERXTX}$	PLL lock time RX to TX	Without calibration @2.5 ppm		47		µs
$LOCK_{TIMETXRX}$	PLL lock time TX to RX	Without calibration @2.5 ppm		32		µs

4.3.13 Flash memory characteristics

The characteristics below are guaranteed by design.

***Table 23**- Flash memory characteristics*

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
t_{prog}	32-bit programming time		20	40	µs
t_{prog_burst}	4x32-bit burst programming time		20	40	

t_{ERASE}	Page (2 Kbyte) erase time		20	40	ms
t_{ME}	Mass erase time		20	40	
I_{DD}	Average consumption from VDD	Write mode	3		mA
		Erase mode	3		
		Mass erase	5		

***Table 24**- Flash memory endurance and data retention*

Symbol	Parameter	Test conditions	Min.	Unit
N_{END}	Endurance	T_A = -40 to +85 ℃	10	kcycles
t_{RET}	Data retention	T_A = 85 ℃	10	Years

4.3.14 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n + 1) supply pins). This test conforms to the ANSI/JEDEC standard.

***Table 25**- ESD absolute maximum ratings*

Symbol	Parameter	Conditions	Class	Max.(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	Conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CBM)}$	Electrostatic discharge voltage (charge device model)	Conforming to ANSI/ESDA/STM5.3.1 JS-002	C2a	500	

(1) Guaranteed by characterization results.

4.3.15 I/O port characteristics

Unless otherwise specified, the parameters given in the tables below are derived from tests performed under the conditions summarized in General operating conditions. All I/Os are designed as CMOS-compliant.

***Table 26**- I/O static characteristics*

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
VIL	I/O input low level voltage	1.62 V < VDD < 3.6 V			0.3xVDD	V
VIH	I/O input low level voltage		0.7xVDD			

I_{lkg}	Input leakage current	0 <= VIN <= Max(VDDx) (1)			±100	nA
		Max(VDDx) (1) <= VIN <= Max(VDDx) (1) +1V			650	
		Max(VDDx) (1) + 1V < VIN <= 5.5 V			200	
R_{PU}	Pull up resistor	VIN=GND	25	40	55	KΩ
R_{PD}	Pull down resistor	VIN=GND	25	40	55	
C_{IO}	I/O pin capacitance			5		pF

(1) Max(VDDx) is the maximum value among all the I/O supplies.

All I/Os are CMOS-compliant (no software configuration required).

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL} / V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified.

- The sum of the currents sourced by all the I/Os on VDD, plus the maximum consumption of the MCU sourced on VDD, cannot exceed the absolute maximum rating ΣIVDD.
- The sum of the currents sunk by all the I/Os on VSS, plus the maximum consumption of the MCU sunk on GND, cannot exceed the absolute maximum rating ΣIVGND.

The characteristics below are guaranteed by characterization.

***Table 27**- Output voltage characteristics*

Symbol	Parameter	Conditions	Min.	Max.	Unit
VOL	Output low level voltage for an I/O pin	CMOS port (1) |IIO| = 8 mA VDD ≥ 2.7 V		0.4	V
VOH	Output high level voltage for an I/O pin		VDD-0.4		
VOL	Output low level voltage for an I/O pin	|IIO| = 20 mA VDD ≥ 2.7 V		1.3	
VOH	Output high level voltage for an I/O pin		VDD-1.3		
VOL	Output low level voltage for an I/O pin	|IIO| = 4 mA VDD ≥ 1.62 V		0.4	
VOH	Output high level voltage for an I/O pin		VDD-0.45		

(1) CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

4.3.16 RSTN pin characteristics

The RSTN pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 4.3.2 General operating conditions. The characteristics

below are guaranteed by design.

***Table 28**- RSTN pin characteristics*

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$VIL_{(RSTN)}$	RSTN input low level voltage				0.3 x VDD	V
$VIH_{(RSTN)}$	RSTN input high level voltage		0.7 x VDD			
$Vhys_{(RSTN)}$	RSTN Schmitt trigger voltage hysteresis			200		mV
RPU	Weak pull up equivalent resistor	VIN=GND	25	40	55	KΩ

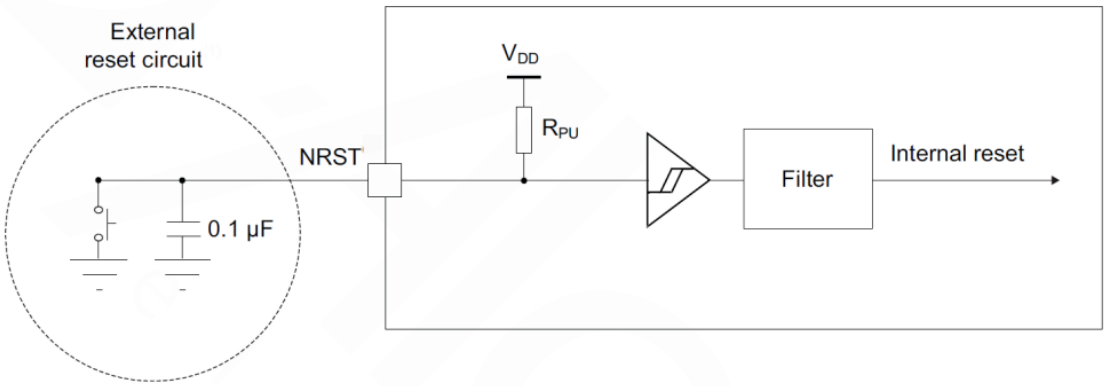


***Figure 3** - Recommended RSTN pin protection*

Note:

The external reset circuit protects the device against parasitic resets.

The user must ensure that the level on the RSTN pin can go below the V_{IL}(RSTN) max. level specified in the table, otherwise the reset is not taken into account by the device. The external capacitor on RSTN must be placed as close as possible to the device.

4.3.17 ADC characteristics

***Table 29**- ADC characteristics (HSI must be set to PLL mode)*

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ch_diff_num	Number of channels for differential mode				4	
Ch_se_num	Number of channels for single ended mode				8	
$IBAT_{ADCBIAS}$	ADC biasing consumption at battery	Biasing blocks turned on		145		mA

$IBAT_{ADCACTIVE}$	ADC active consumption at battery	ADC activated in differential mode		185		mA
VDDA	Analog supply voltage		1.2		1.32	V
R_{AIN}	Input impedance	In DC		250		KΩ
R_{in}	Internal access resistance	VBOOST is enabled for VDD < 2.7 V			550	Ω
C_{in}	Input sampling capacitor			4		pF
T_s	Sampling period			1		µs
T_{sw}	Sampling time			125		ns
DR	Output data rate			200		k samples/s
$FRMT_{output}$	Output data format			16		bits
T_L	Latency time	200 kSps		5		µs
$T_{STARTUP}$	Start-up time	From ADC enable to conversion start			1	µs
DNL	Differential non-linearity			±0.7		LSB
INL	Integral non-linearity			±1		LSB
SNR Diff	Signal to noise ratio	Differential input @1 kHz, -1 dBFs		72		dB
STHD Diff	Signal to THD ratio (10 harmonics)	Differential input @1 kHz, -1 dBFs		80		dB
ENOB Diff	Effective number of bits	Differential input @1 kHz, -1 dBFs		11.5		bits
SNR SE	Signal to noise ratio	Single ended @1 kHz, -1 dBFs		70		dB
STHD SE	Signal to THD ratio (10 harmonics)	Single ended @1 kHz, -1 dBFs		75		dB
ENOB SE	Effective number of bits	Single ended @1 kHz, -1 dBFs		11		bits
	ADC_ERR_1V7	Absolute error when used for battery measurement at 1.7V, 2.4V, 3.0V,3.6V		13		mV
	ADC_ERR_2V4			0		
	ADC_ERR_3V0			-9		
	ADC_ERR_3V6			-22		

4.3.18 Temperature sensor characteristics

***Table 30**- Temperature sensor characteristics*

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{rERR}	Error in temperature		±4		℃
T_{SLOPE}	Average temperature coefficient		8		LSB/℃

T_{ICC}	Current consumption		415		µA
T_{TS-OUT}	Output voltage level at 30°C (+-5°C)		2533		V

4.3.19 Timer characteristics

The characteristics below are guaranteed by design.

***Table 31**- TIM1 characteristics*

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 64 MHz		15.625		ns
R_{esTIM}	Timer resolution			16		bit
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 64 MHz	0.015625		1024	µs
t_{MAX_COUNT}	Maximum possible count time	$f_{TIMxCLK}$= 64			67.10	s

***Table 32**- IWDG min./max. timeout period at 32 kHz (LSE)*

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

4.3.20 I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev.03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. The 20 mA output drive requirement in Fast-mode Plus is supported partially.

This limits the maximum load Cload supported in Fast-mode Plus, given by these formulas:

- t_r (SDA/SCL) = 0.8473 x R_p x C_{load}
- R_p (min) = [V_{DD} - V_{OL} (max)] / I_{OL} (max)

where R_p is the I^2C lines pull-up.

All I^2C SDA and SCL I/Os embed an analog filter.

The characteristics below are guaranteed by design.

***Table 33**- I²C analog filter characteristics*

Symbol	Parameter	Min.	Max.	Unit
tAF	Maximum pulse width of spikes that are suppressed by the analog filter	50	110	ns

4.3.21 SPI characteristics

The parameters for SPI are derived from tests performed according to fPCLKx frequency and supply voltage conditions.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x VDD

The characteristics below are guaranteed by design.

***Table 34**- SPI characteristics*

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCK}	SPI clock frequency	Master mode		-	32	MHz
		Slave mode		-	32(1)	
t_{su}(NSS)	NSS setup time		4 / f_{PCLK}	-	-	-
t_h(NSS)	NSS hold time		2 / f_{PCLK}	-	-	-
tw(SCKH)	SCK high and low time	Master mode	1 / f_{PCLK} - 1.5	1 / f_{PCLK}	1 / f_{PCLK}+1	ns
tw(SCKL)			1 / f_{PCLK} - 1.5	1 / f_{PCLK}	1 / f_{PCLK}+1	
t_{su}(MI)	Data input setup time	Master mode	1	-	-	
t_{su}(SI)	Data input setup time	Slave mode	1	-	-	
t_h(MI)	Data input hold time	Master mode	3	-	-	
t_h(SI)	Data input hold time	Slave mode	1	-	-	
t_a(SO)	Data output access time	Slave mode	5	-	40	
t_{dis}(SO)	Data output disable time	Slave mode	5	-	38	
t_v(SO)	Data output valid time	Master mode	-	2	8	

		Slave mode	-	12	39	
t_h(SO)	Data output valid time	Master mode	2		-	ns
		Slave mode	4		-	

(1) The maximum frequency in slave transmitter mode is determined by the sum of tv(SO) and tsu(MI), which has to fit SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while duty(SCK) = 50 %.

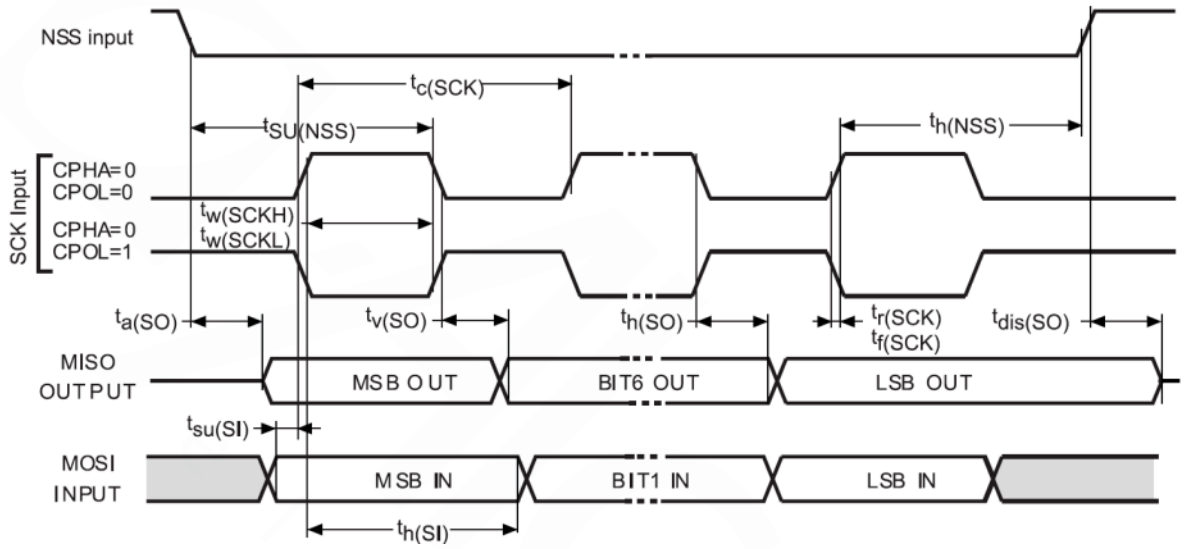


Figure 4 *- SPI timing diagram - slave mode and CPHA = 0*

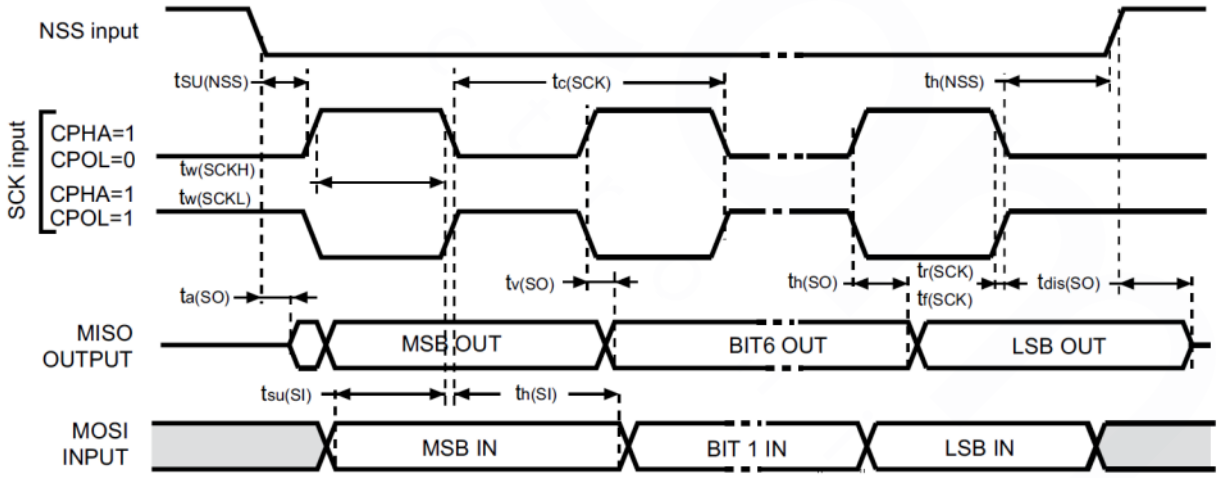


Figure 5 *- SPI timing diagram - slave mode and CPHA = 1*

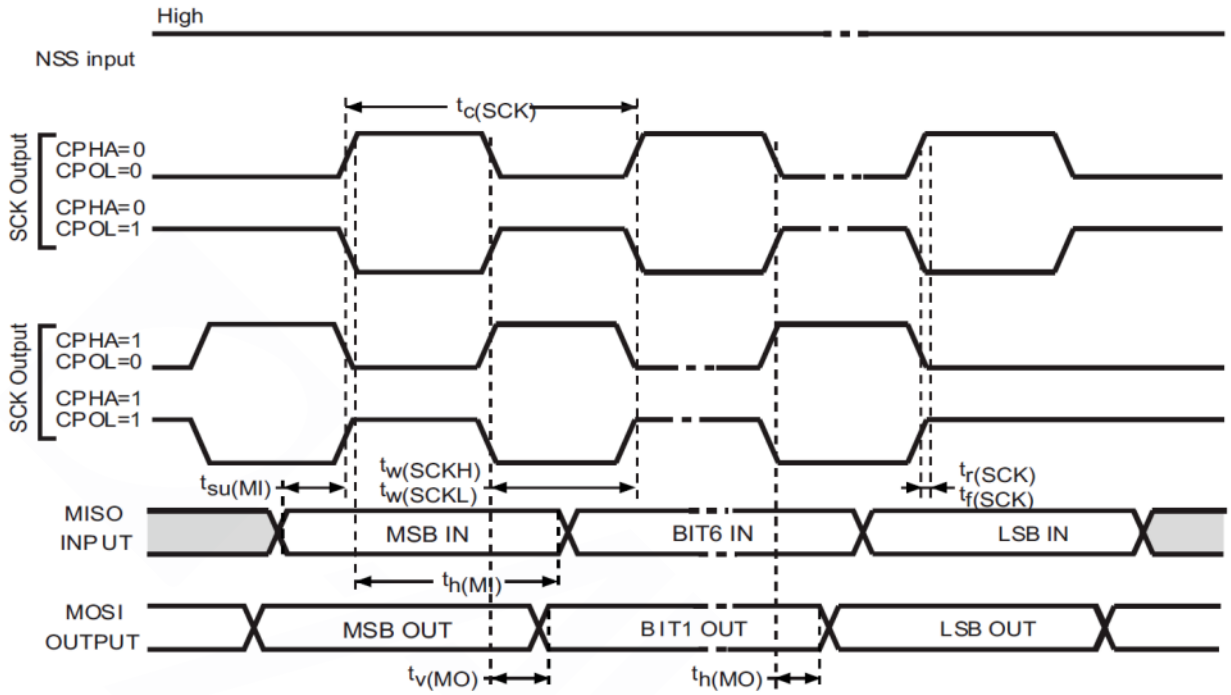


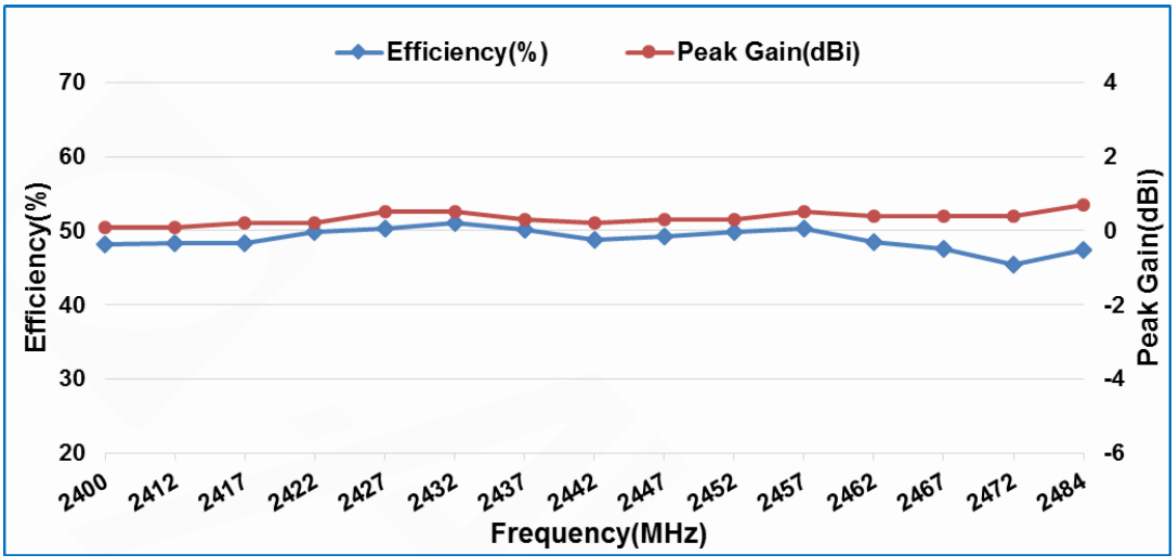
Figure 6 *- SPI timing diagram - master mode*

4.3.22 Typical characteristics

There are some typical performance plots measured on the BlueNRG-355AC device in the BlueNRG-LP data sheet, and the plots relevant for the WB2072-00 module. Please visit STMicroelectronics web site https://www.st.com/resource/en/datasheet/bluenrg-lp.pdf

4.4. Chip Antenna Characteristics

Measured on the Jorjin WB2072E00A EM board with T_A = 25°C



Frequency (MHz)	2400	2412	2417	2422	2427	2432	2437	2442	2447	2452	2457	2462	2467	2472	2484
Efficiency (dB)	-3.2	-3.2	-3.2	-3.0	-3.0	-2.9	-3.0	-3.1	-3.1	-3.0	-3.0	-3.2	-3.2	-3.4	-3.2
Efficiency (%)	48.2	48.3	48.3	49.9	50.3	51.0	50.1	48.8	49.3	49.9	50.3	48.4	47.5	45.5	47.4
Peak Gain (dBi)	0.1	0.1	0.2	0.2	0.5	0.5	0.3	0.2	0.3	0.3	0.5	0.4	0.4	0.4	0.7

Figure 7 *– Efficiency vs. Frequency*

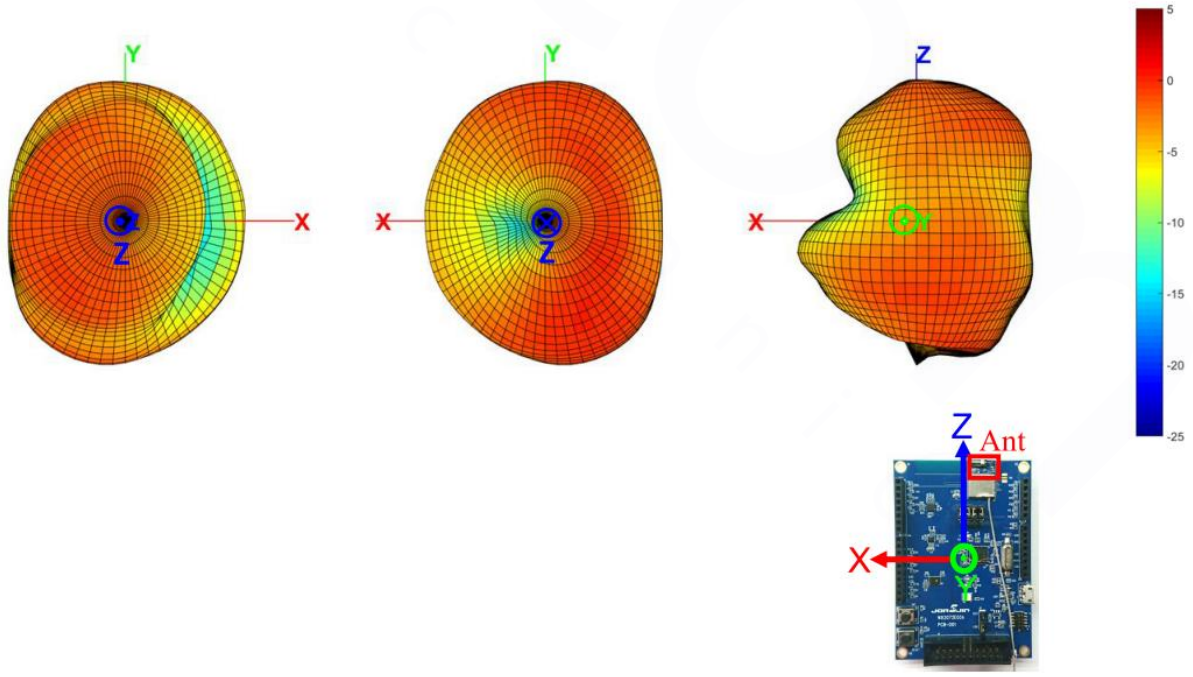


Figure 8 *– 3D Pattern*

5. DESIGN RECOMMENDATIONS

5.1. Module Layout Recommendations

Follow these module layout recommendations:

- Antenna

For a module with on board chip antenna, to eliminate the influence from other components or ground, recommended that the module is placed in the corner of main PCB, and define a clearance area around the antenna, where no grounding or signal trace are contained. The clearance area applies to all layers of the main PCB. The recommended dimensions of the main PCB keep out area are shown in bellow.

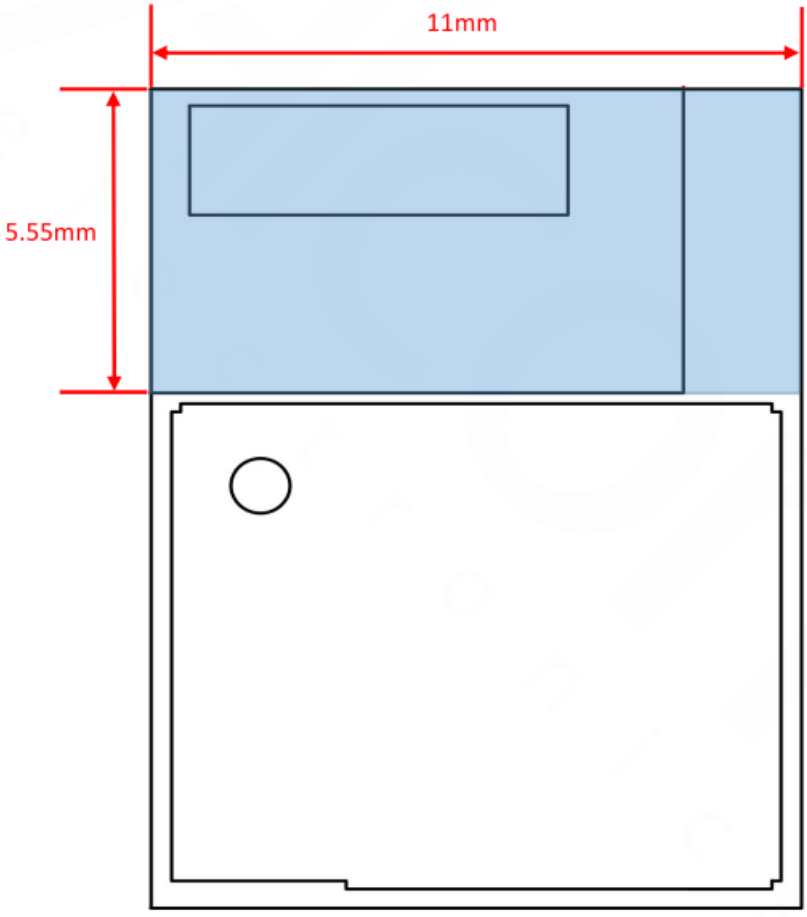


Figure 9 *–PCB keep out area*

- RF test point

There are RF test points in the bottom side of this module. It is only for module production used. Do not connect any signal to these test points (leave no connection) in the module. And do not design test point in the main board. Please reserve a clearance in the top-side copper plane underneath the RF test pads. Do not route any signal or place via in this keep out area.

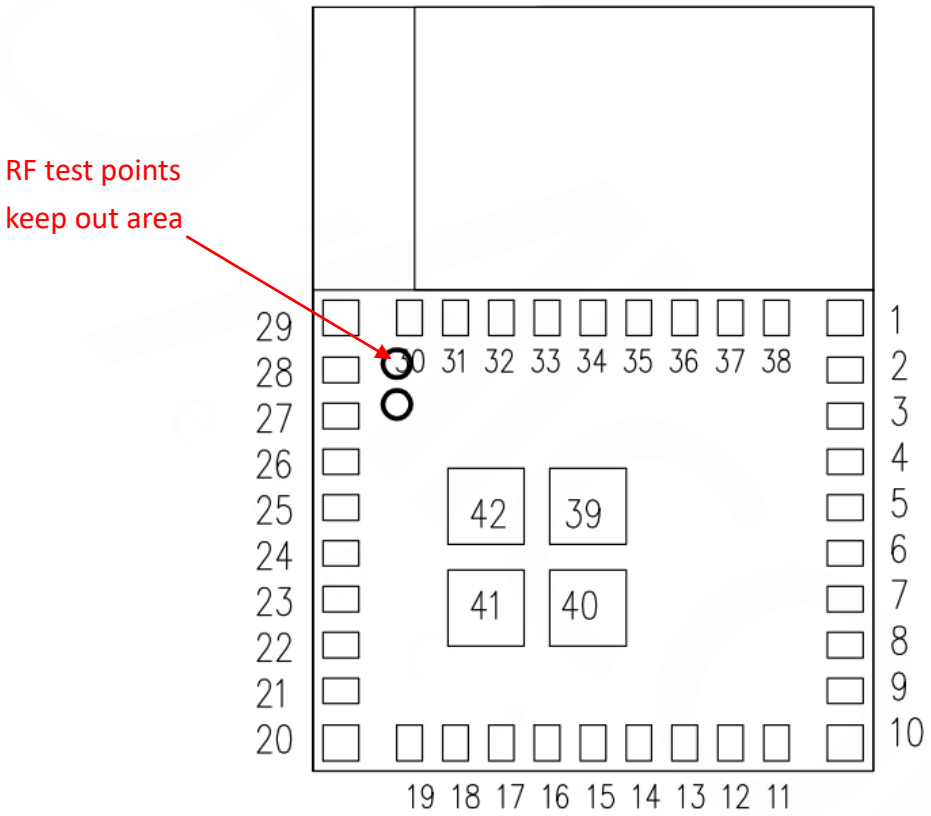


Figure 10 *–RF Point*

5.2. Reference Schematic

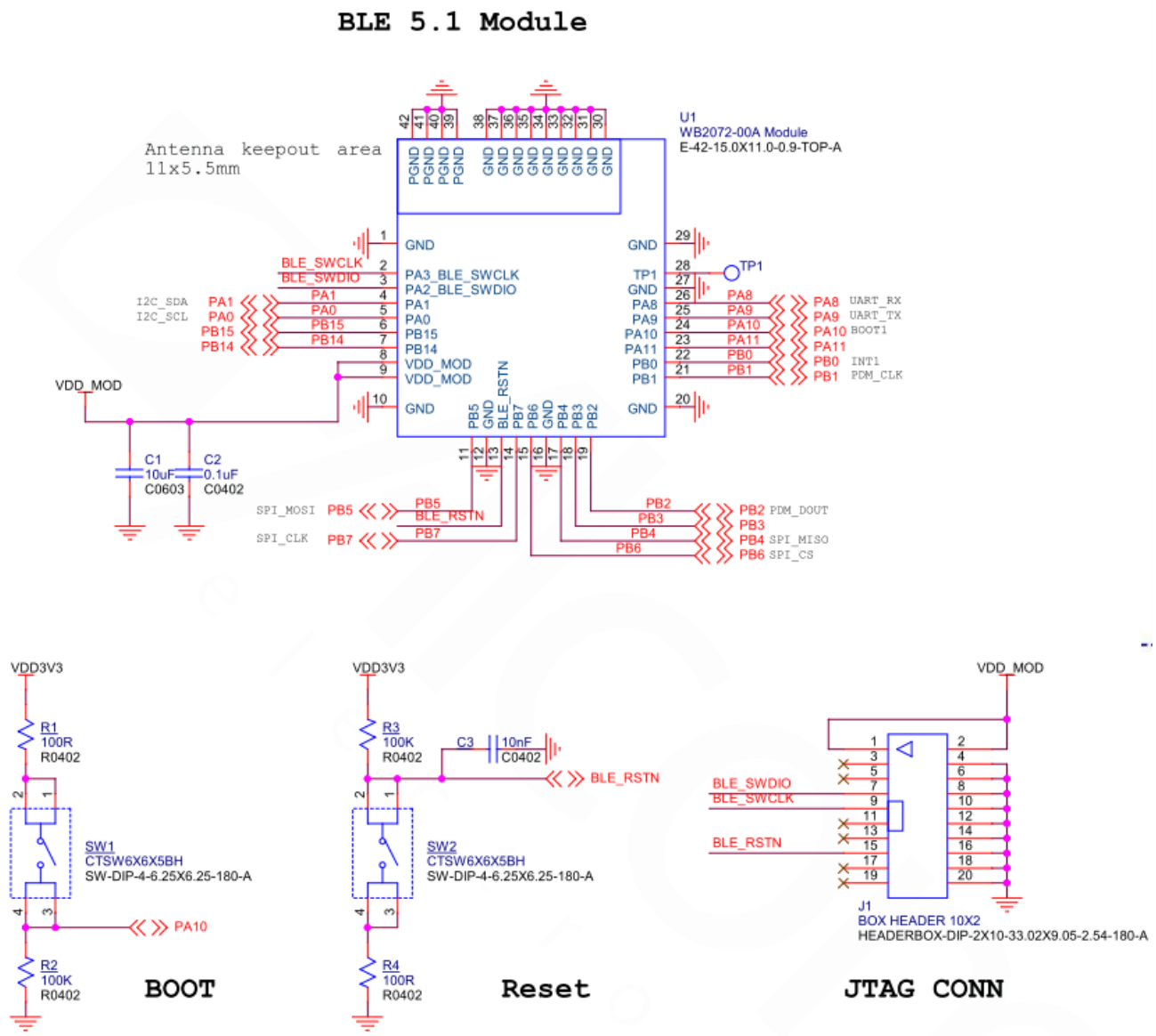


Figure 11 – *Reference Schematic*

6. PACKAGE INFORMATION

6.1. Module Mechanical Outline

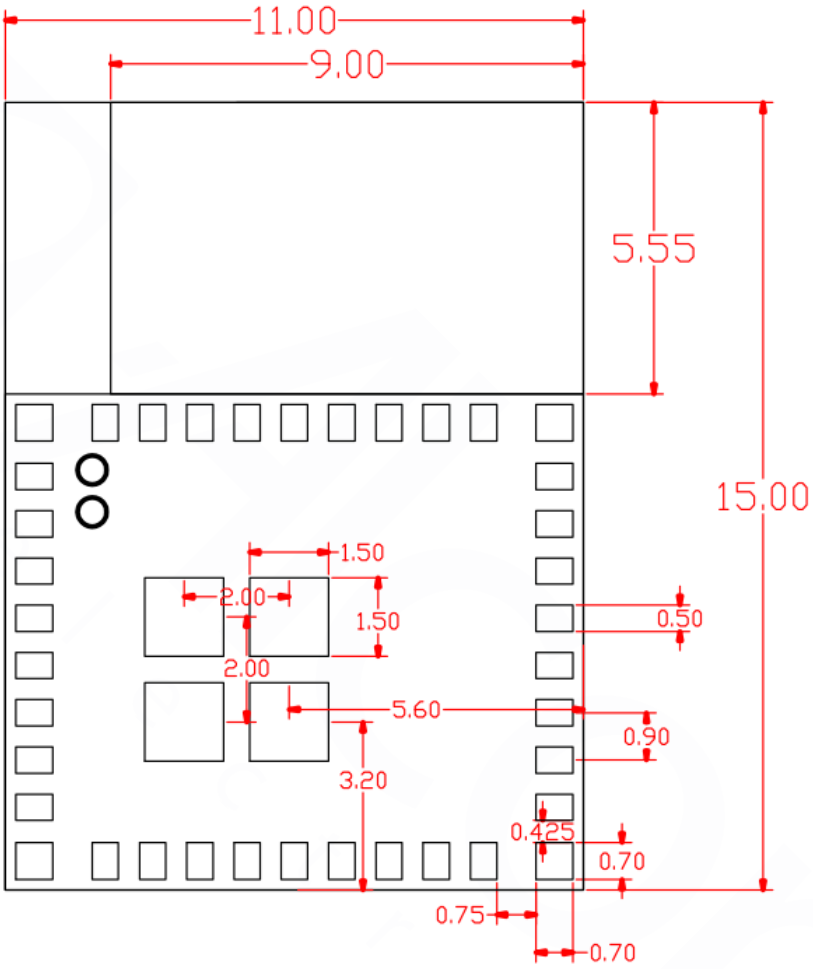


Figure 12 *– Module Mechanical Outline (BOTTOM View)*

Note:

1> Pad tolerance as ±30μm

2> Unit: mm

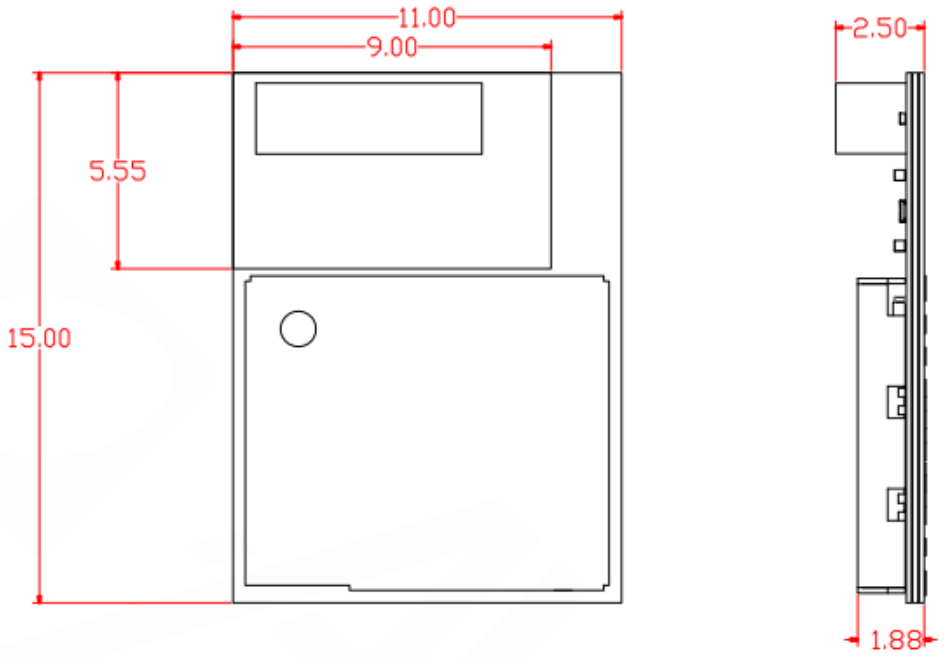


Figure 13 *– Module Mechanical Outline (TOP and Side View)*

Note:

Unit: mm

6.2. Ordering Information

Order Number	Package
WB2072-00	LGA-42

6.3. Package Marking

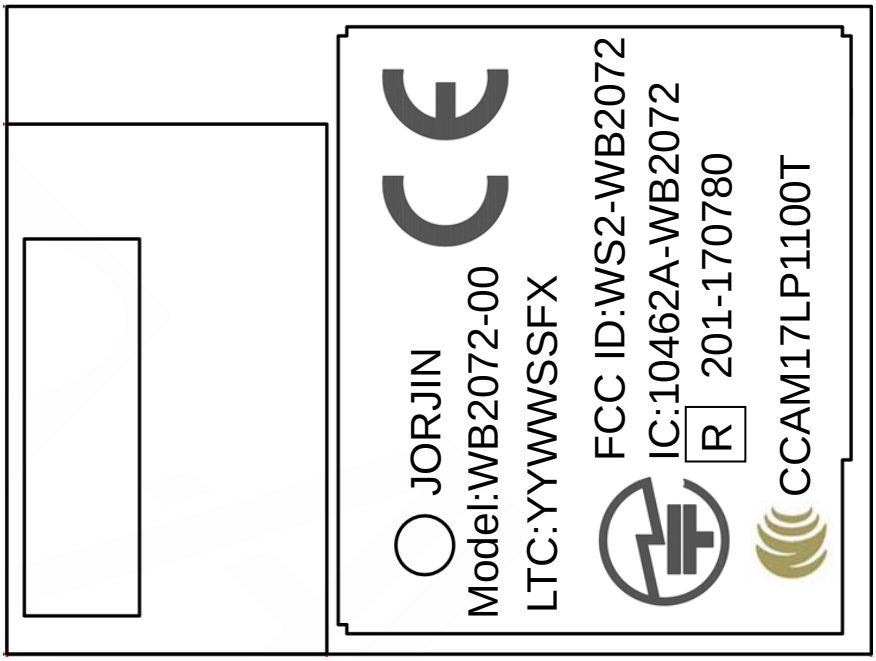


Figure 14 *–shielding case information*

Marking	Description
JORJIN	Brand name
WB2072-00	Model name
YYWWSSFX	Lot Trace Code: YYWWSSFX YY= Digit of the year, ex: 2017=17 WW= Week (01~52) SS= Serial number from 01~98 match to MFG's lot number, or 99 to repair control code F= Reverse for internal use X = A for Module version
WS2-WB2072	FCC ID
10462A-WB2072	Canada IC ID
	TELEC compliance mark, and ID
	CE compliance mark
	NCC compliance mark, and ID

7. SMT AND BAKING RECOMMENDATION

7.1. Baking Recommendation

- Baking condition：

  - Follow MSL Level 4 to do baking process.

  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be

  a) Mounted within 72 hours of factory conditions <30°C/60% RH, or

  b) Stored at <10% RH.

  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%

  - If baking is required, Devices may be baked for 8 hrs. at 125 °C.

7.2. SMT Recommendation

- Recommended Reflow profile：

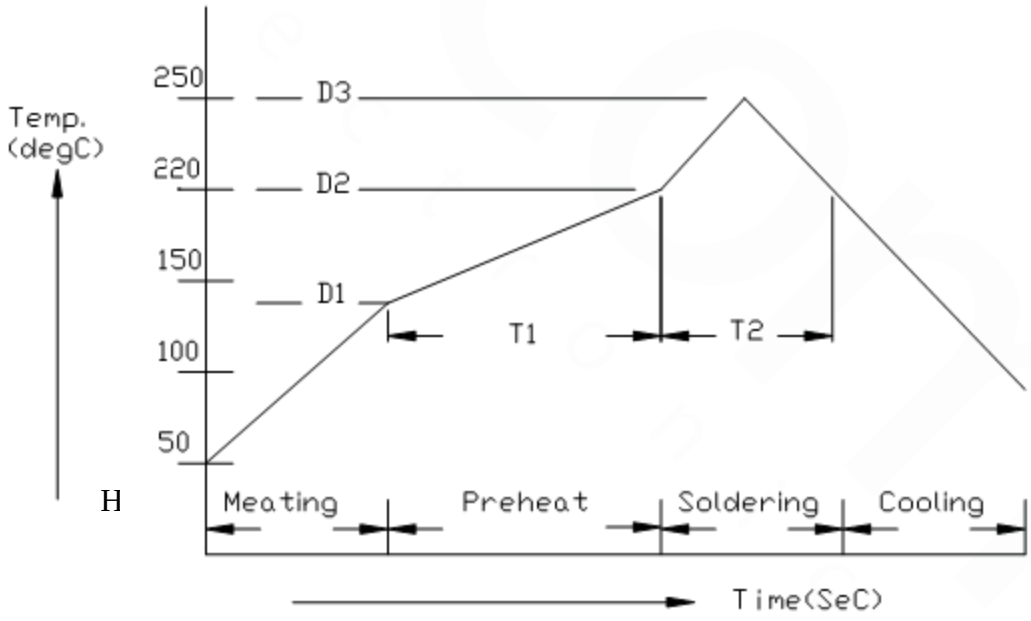


Figure 15 *– Reflow profile*

No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

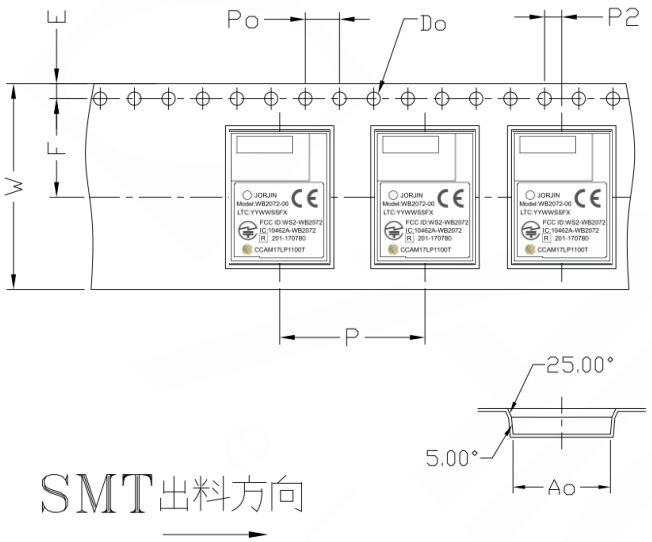
Note: (1) Reflow soldering is recommended two times maximum.

(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

- **Stencil thickness**： 0.1~ 0.13 mm (Recommended)
- **Soldering paste (without Pb)**： Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

8. TAPE REEL INFROMATION

8.1. Cover / Carrier Tape Dimension



ITEM	DIM	ALTERNATE
W	$24.00^{+0.30}_{-0.30}$	
E	$1.75^{+0.10}_{-0.10}$	
F	$11.50^{+0.10}_{-0.10}$	
P	$16.00^{+0.10}_{-0.10}$	
Po	$4.00^{+0.10}_{-0.10}$	
P2	$2.00^{+0.10}_{-0.10}$	
Do	$\phi 1.50^{+0.10}_{-0.00}$	
T	$0.35^{+0.05}_{-0.05}$	
Ao	$11.40^{+0.10}_{-0.10}$	
Bo	$15.40^{+0.10}_{-0.10}$	
Ko	$3.00^{+0.10}_{-0.10}$	

Packing Qty	Dry Bag	Inner Box	Outer Box
1200 EA / Reel	1 Reel (1200 EA)	1 Dry Bag (1200 EA)	4 Inner Box (4800 EA)

Inner Box Size : 352mm x 352mm x 56mm

Outer Box Size : 354mm x 362mm x 250mm

9. REGULATORY INFORMATION

TBD

10. HISTORY CHANGE

Revision	Date	Description
Draft 1.0	2020.07.08	Draft version released.
Draft 1.1	2020.08.11	Update parameter values
Draft 2.0	2020.11.12	Re-edit
Draft 2.0	2020.11.13	Update Figure 1 – Module block diagram
R01	2020.12.16	Official version released