HOLTEK

HT74153
6.0V / 2.0A / 1.2MHz Synchronous Step-Down Converter

Features

- Wide input range of V_{IN} from 2.5V to 6.0V
- Output voltage range from 0.6V to V_{DD}
- Internal low on-resistance switches
  - High-Side $R_{DS(ON)}$ 100mΩ
  - Low-Side $R_{DS(ON)}$ 100mΩ
- 100% duty cycle operation
- Switching frequency: 1.2MHz
- PFM mode operation when no load/light load conditions
- Output voltage power good indicator when V_{OUT}=0.95×$V_{OUT(TARGET)}$ (8SOP-EP)
- Low IC surface temperature in short circuit protection
- Protection features
  - V_{DD} under voltage lock-out
  - Cycle-by-Cycle over current protection
  - Thermal shutdown protection
  - Output short-circuit protection
  - Output over-voltage protection
- Package types: 8-pin SOP-EP and 5-pin SOT23

Applications

- Single Li-Battery applications and small motor driver applications
- Rechargeable AA batteries
- Laser demarcation device
- Portable toy
- 5V USB/Adaptor power source
- 3.3V DC source

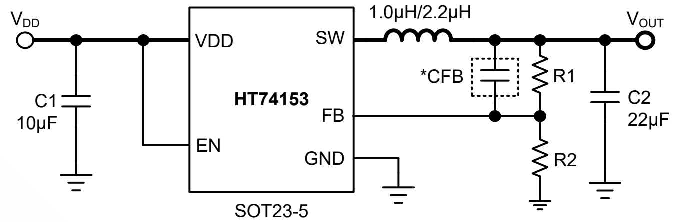
General Description

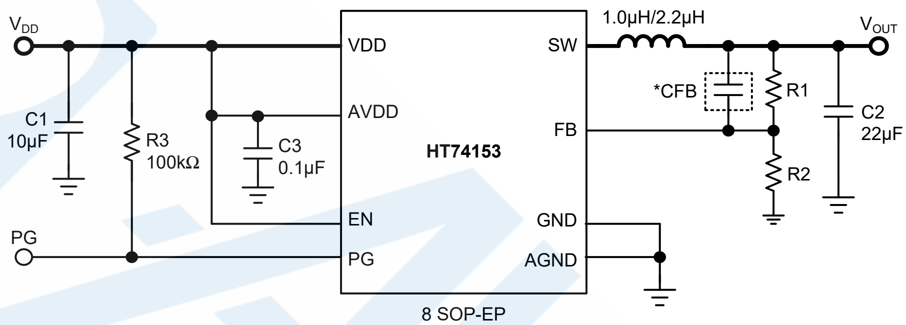
The HT74153 is a high efficiency synchronous step-down converter capable of delivering 2A output current. It can operate over a wide input voltage range from 2.5V to 6.0V and integrates 100mΩ low on-resistance main and rectified switches to minimize the conduction losses. Up to 1.2MHz switching frequency in PWM allows to use the small surface mount inductors and capacitors in applications.

The automatically PWM/PFM mode switching is useful to drive up to 2A load current and also decrease its standby current in no load condition. The Hysteretic PFM mode extends the battery life by reducing the quiescent current during the system standby. In the shutdown mode, the device turns off and consumes only 0.1µA input current.

The HT74153 also provides 100% duty cycle operation. When the input supply voltage decreases toward the targeted output voltage, the High-Side MOSFET will always turn on and the output voltage tracks the input voltage, which can extend the battery life.

Typical Application Circuit



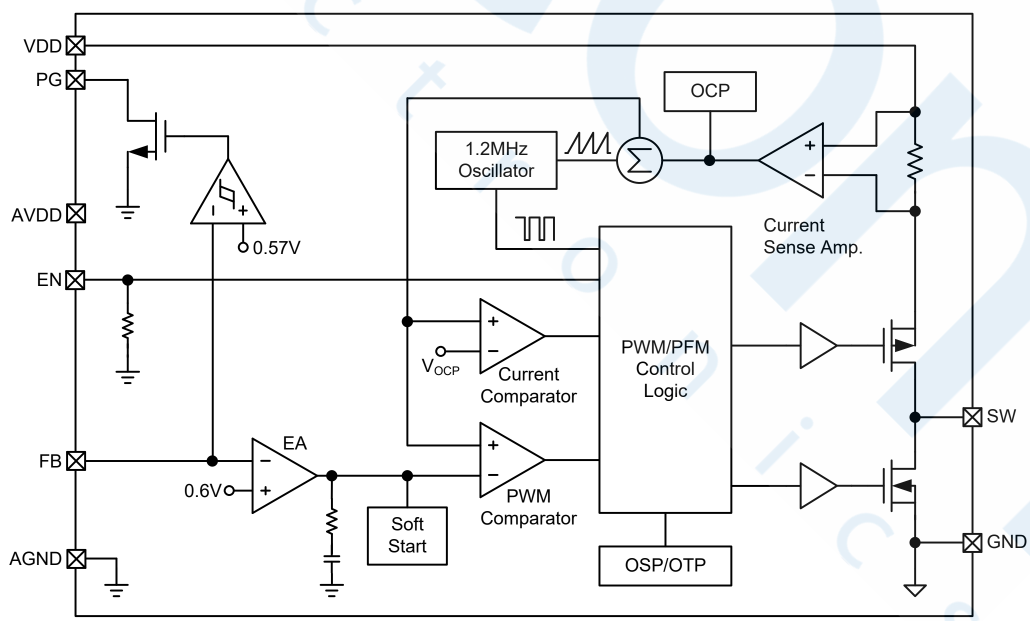


Note: *CFB option is recommended to refer the "Application Information-Load Transient Compensation Design" chapter.

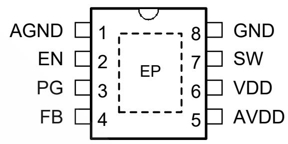
Selection Table

Part No.	Package	Marking
HT74153	8SOP-EP	HT74153
	SOT23-5	4153

Block Diagram

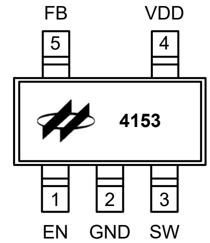


Pin Assignment



HT74153
8 SOP-EP-A

SOT23-5



Pin Description

Pin Name	Pin No.		Type	Description
	8SOP-EP	SOT23-5		
AGND	1	—	G	Analog ground pin
EN	2	1	I	Chip enable pin. High Active. Internally connect a 1MΩ pull down resistor
PG	3	—	O	Output power good indicate pin. Connect a 100kΩ pull up resistor to VDD
FB	4	5	I	Output voltage feedback pin. Set output voltage via resistor dividers R1 and R2
AVDD	5	—	P	Analog input pin. Connect a 0.1μF ceramic capacitor to GND at least
VDD	6	4	P	Power input pin. Connect a 10μF ceramic capacitor to GND at least
SW	7	3	O	Switching node. Connect to power inductor
GND	8	2	G	Power ground pin
EP	—	—	G	Exposed pad. Connect to AGND

Absolute Maximum Ratings

Parameter		Value	Unit
VDD, AVDD		-0.3 ~ +6.4	V
SW		-0.3 ~ (V_{DD}+0.3)	V
EN, PG, FB		-0.3 ~ +6.4	V
Operating Temperature Range		-40 ~ +85	°C
Output Current		Thermal Limits	—
Maximum Junction Temperature		+150	°C
Storage Temperature Range		-60 ~ +150	°C
Lead Temperature (Soldering 10sec)		+300	°C
ESD Susceptibility	Human Body Model	4000	V
	Machine Model	200	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	8SOP-EP	125	°C/W
	SOT23-5	220	

Recommended Operating Range

Parameter	Value	Unit
V_{DD}, AV_{DD}	2.5 ~ 6.0	V
$I_{OUT(MAX)}$	2	A

Note that Absolute Maximum Ratings indicate limitations beyond which damage to the device may occur. Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits.

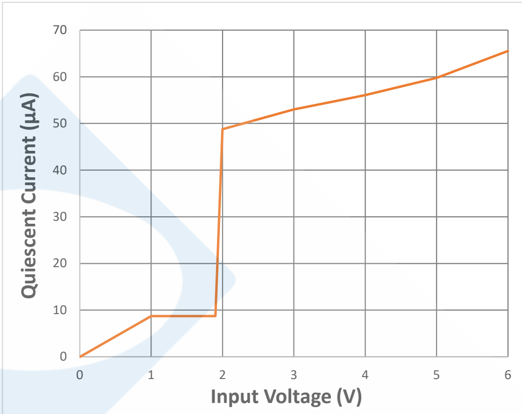
Electrical Characteristics

V_{DD}=AV_{DD}=3.6V, Ta=25°C, unless otherwise specified

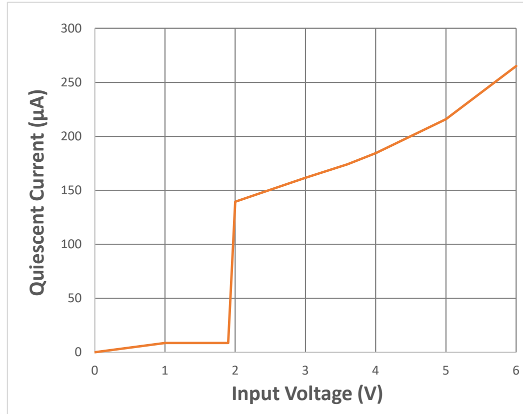
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage						
V_{DD}	Input Voltage	V_{DD}=AV_{DD}	2.5	—	6.0	V
I_{DD}	Input Supply Current	I_{AVDD}+I_{VDD}, PWM, V_{FB}=0.58V	—	170	210	μA
		I_{AVDD}+I_{VDD}, PFM, V_{FB}=0.62V	—	50	70	
I_{OFF}	Shutdown Current	I_{AVDD}+I_{VDD}, V_{AVDD}=V_{VDD}=5V, V_{EN}=0V	—	0.1	0.5	μA
Buck Converter						
V_{OUT}	Output Voltage	—	0.6	—	V_{DD}	V
f_{SW}	Switching Frequency	V_{FB}=0.58V	960	1200	1440	kHz
$T_{ON(min)}$	Minimum ON-Time	—	—	100	—	ns
$R_{DS(on)\_P}$	PMOS Switch-ON Resistance	—	—	100	—	mΩ
$R_{DS(on)\_N}$	NMOS Switch-ON Resistance	—	—	100	—	mΩ
I_{LEAK}	SW Leakage Current	V_{EN}=0V, V_{SW}=0V to V_{DD}. Measure I_{SW}	–	0.1	1.0	μA
V_{FB}	Feedback Voltage	2.5V≤V_{DD}≤6V	591	600	609	mV
I_{FB}	FB Leakage Current	V_{FB}=5V	—	—	0.1	μA
V_{IH}	EN High Voltage Threshold	2.5V≤V_{DD}≤6V	1.2	—	—	V
V_{IL}	EN Low Voltage Threshold	2.5V≤V_{DD}≤6V	—	—	0.4	V
R_{PD_EN}	EN Pull Down Resistor	—	—	1	—	MΩ
Protections						
V_{UVLO+}	Input Supply Turn ON Level	UVLO+	—	—	2.1	V
V_{UVLO-}	Input Supply Turn OFF Level	UVLO−	1.6	—	—	V
I_{OCP}	Over Current Protection Threshold	—	—	3.2	—	A
V_{OSP}	Output Short-Circuit Threshold	Measure FB	—	300	—	mV
T_{OSP}	OSP Repeat Time	—	—	21	—	ms
T_{SHD}	Thermal Shutdown Threshold	OTP	—	150	—	°C
T_{HYS}	Thermal Shutdown Hysteresis	—	—	15	—	°C
Others						
R_{PG}	PG Threshold	Measure FB, V_{FB_PG}/V_{FB}	—	95	—	%
$V_{PG(OL)}$	PG Sink Capability	V_{FB}=0.5V. Source 1mA to PG, measure PG	—	—	0.4	V
Tss	Soft Start Time	—	—	0.7	—	ms
V_{FB_OVP}	Prevent Output Overshoot	—	640	660	680	mV

Typical Performance Characteristics

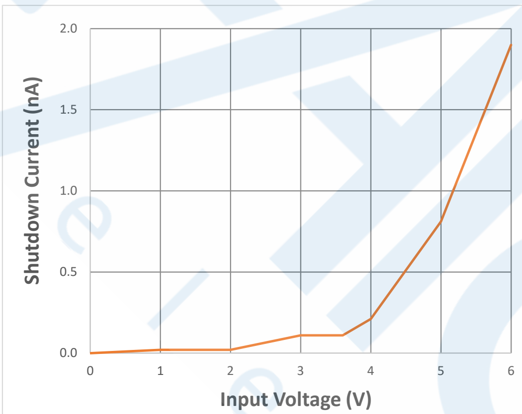
V_{DD}=AV_{DD}=3.6V, Ta=25°C, unless otherwise noted



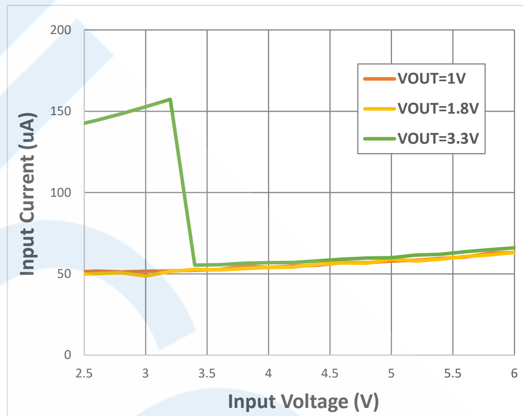
PFM Quiescent Current vs. Input Voltage



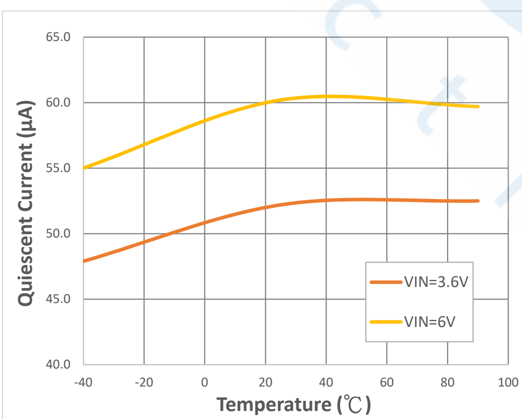
PWM Quiescent Current vs. Input Voltage



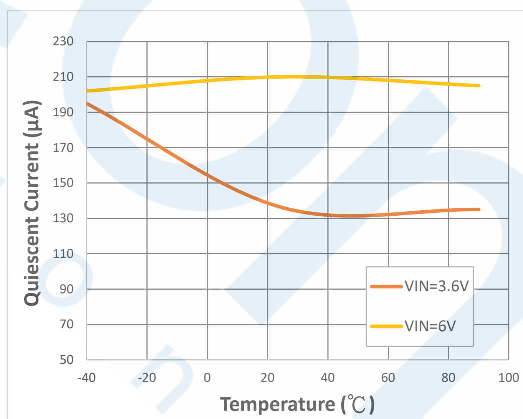
Shutdown Current vs. Input Voltage



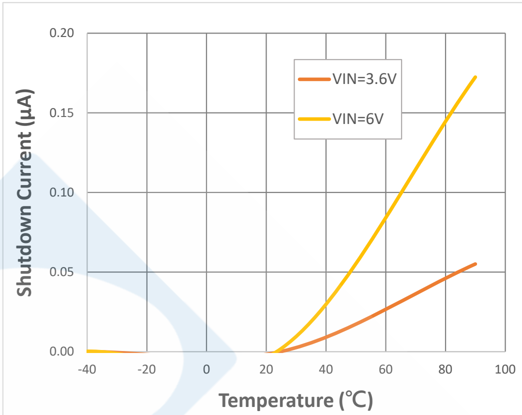
No Load Current vs. Input Voltage



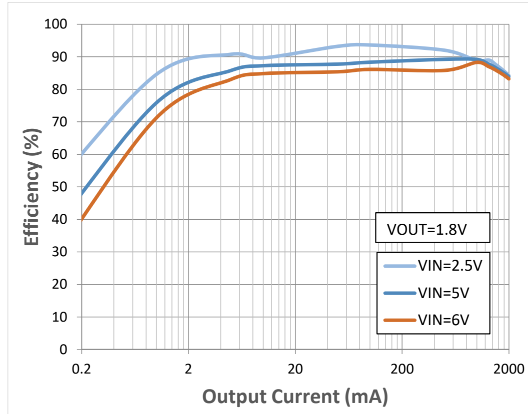
PFM Quiescent Current vs. Temperature



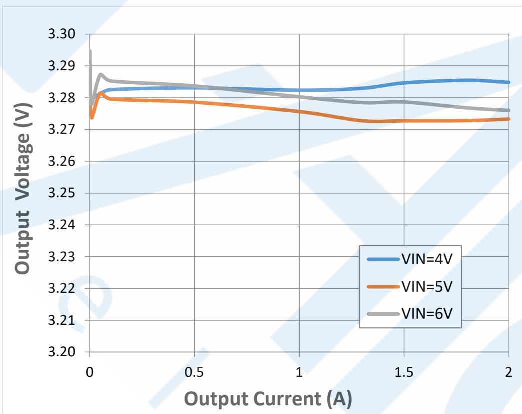
PWM Quiescent Current vs. Temperature



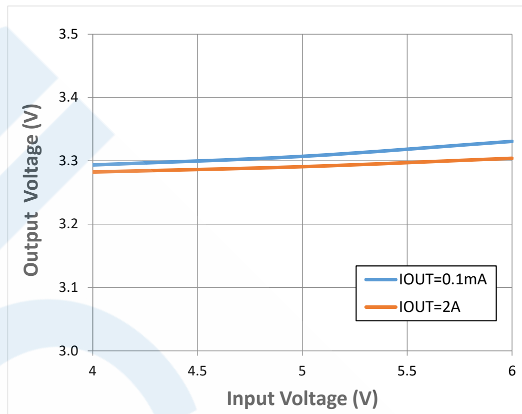
Shutdown Current vs. Temperature



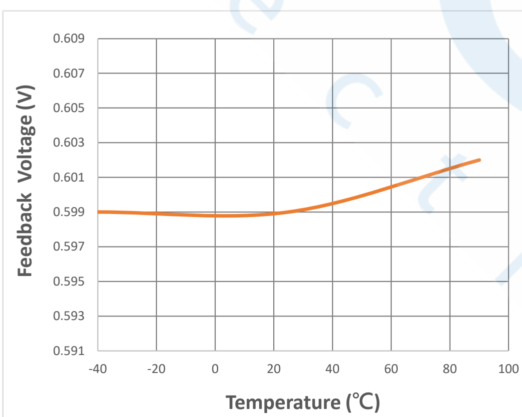
Efficiency vs. Load



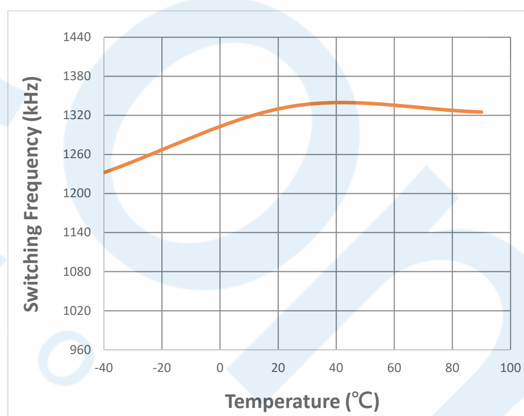
Load Regulation



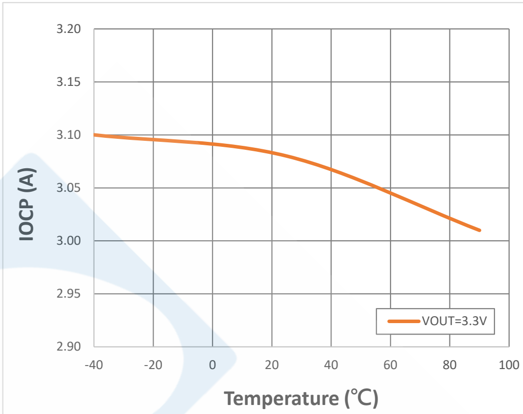
Line Regulation



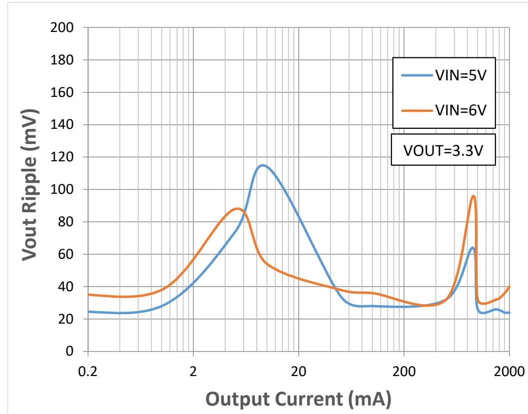
Feedback Voltage vs. Temperature



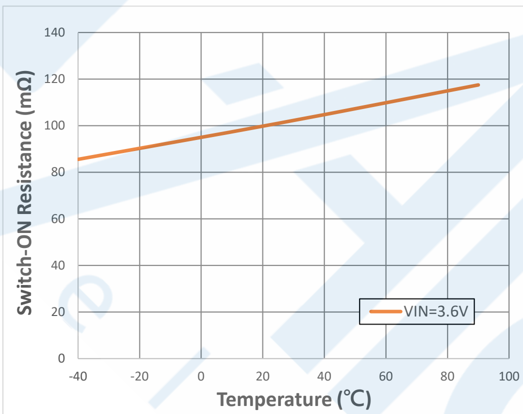
f_{SW} vs. Temperature



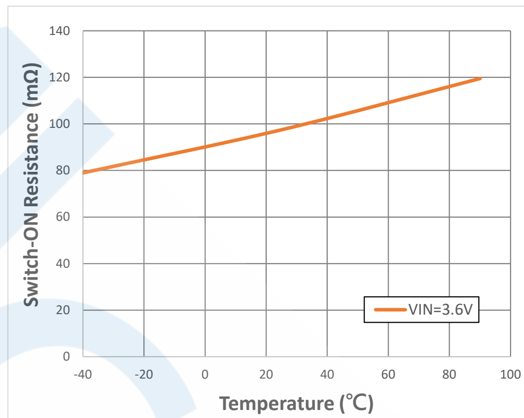
I_{ocp} vs. Temperature



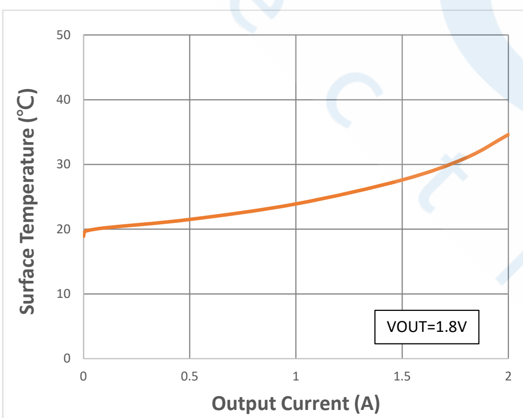
V_{OUT} Ripple



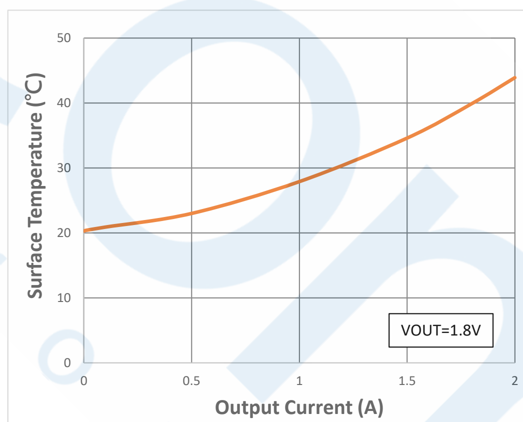
PMOS Switch-ON Resistance vs. Temperature



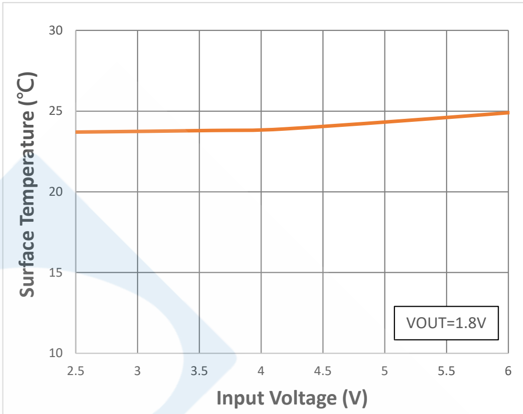
NMOS Switch-ON Resistance vs. Temperature



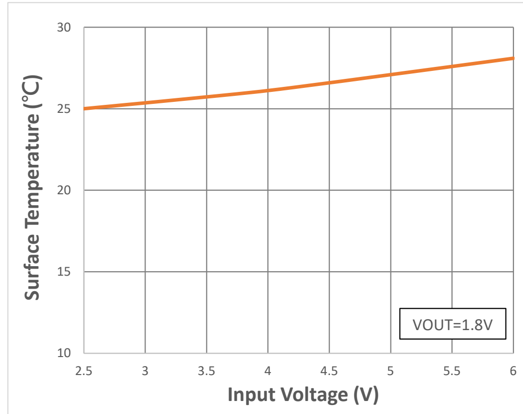
Surface Temperature vs. Output Current (8SOP-EP)



Surface Temperature vs. Output Current (SOT23-5)



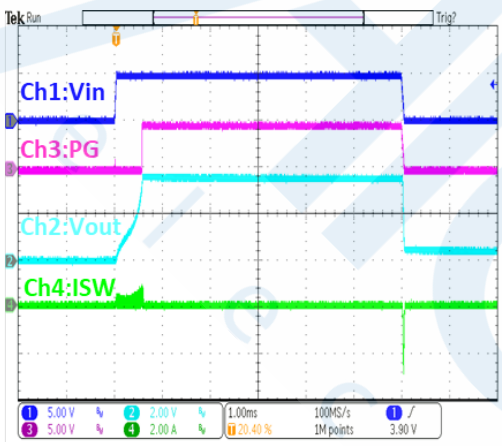
Output Short
Surface Temperature vs. Input Voltage (8SOP-EP)



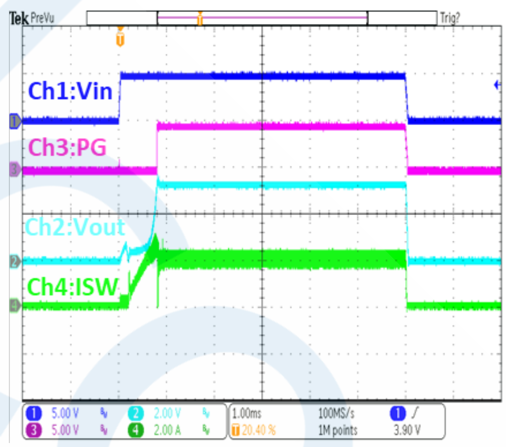
Output Short
Surface Temperature vs. Input Voltage (SOT23-5)

Typical Performance Characteristics (Continued)

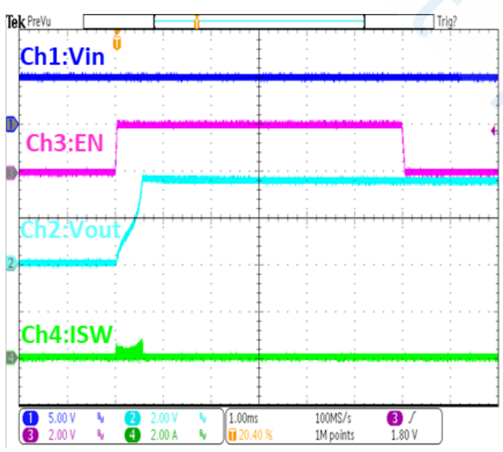
V_{DD}=AV_{DD}=5V, V_{OUT}=3.3V, L=1μH, C_{IN}=10μF+0.1μF, and Ta=25°C, unless otherwise noted



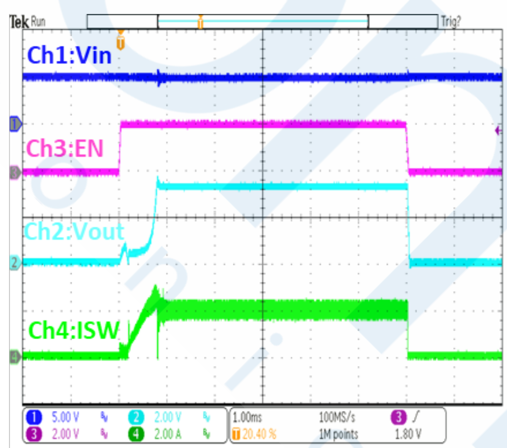
Power On/Off (No Load)



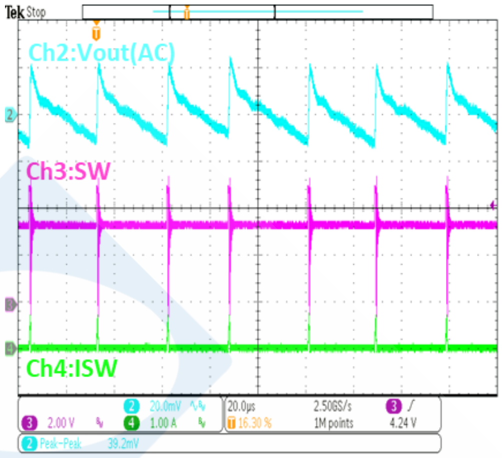
Power On/Off (I_{OUT}=2A)



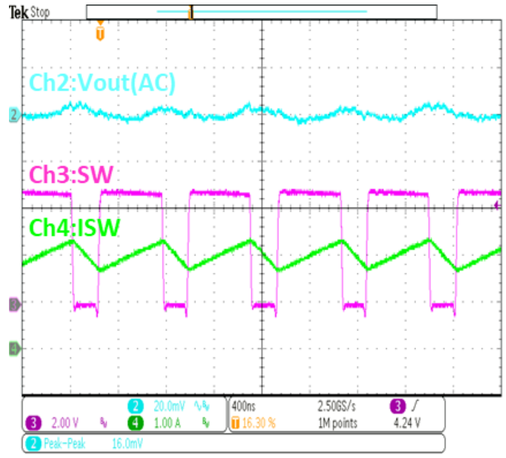
Chip Enable/Disable (No Load)



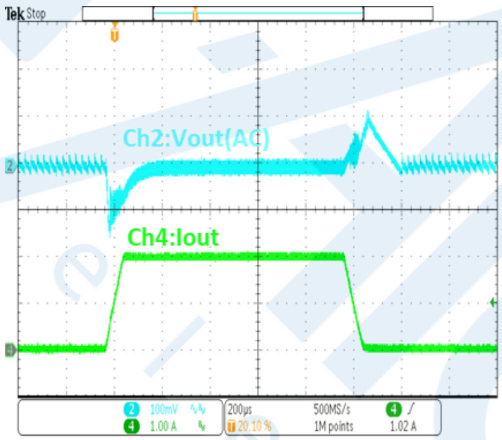
Chip Enable/Disable (I_{OUT}=2A)



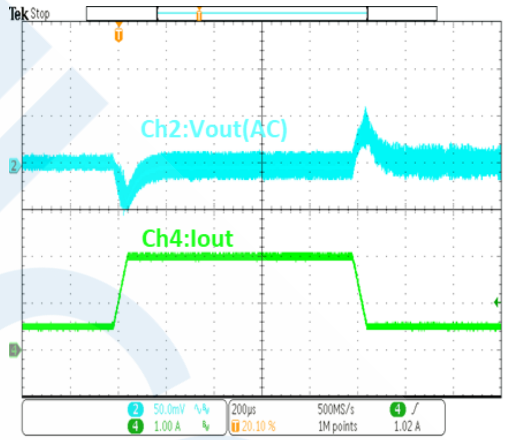
Output Ripple (I_{OUT}=10mA)



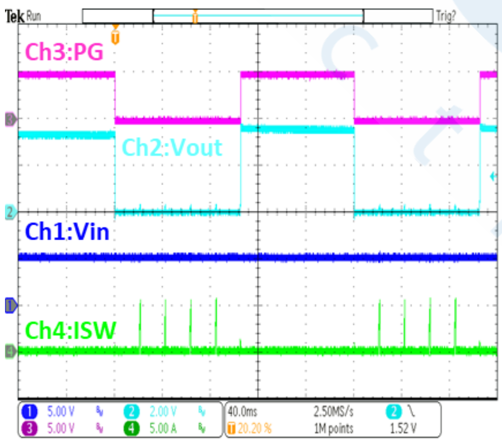
Output Ripple (I_{OUT}=2A)



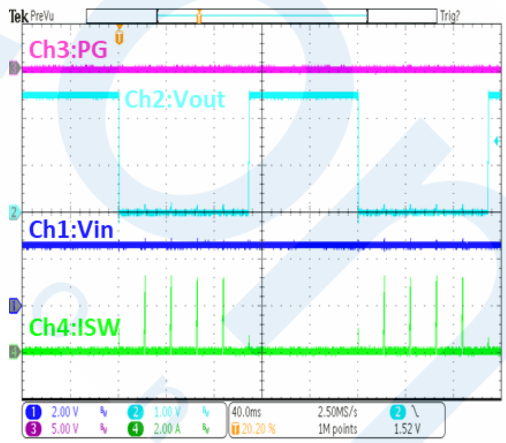
Load Transient (I_{OUT}=1mA↔2A, C_{FB}=47pF)



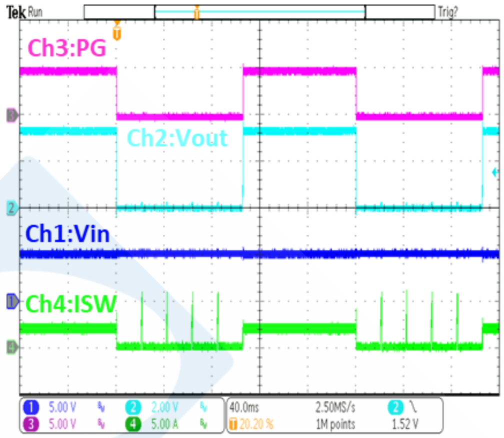
Load Transient (I_{OUT}=0.5A↔2A, C_{FB}=47pF)



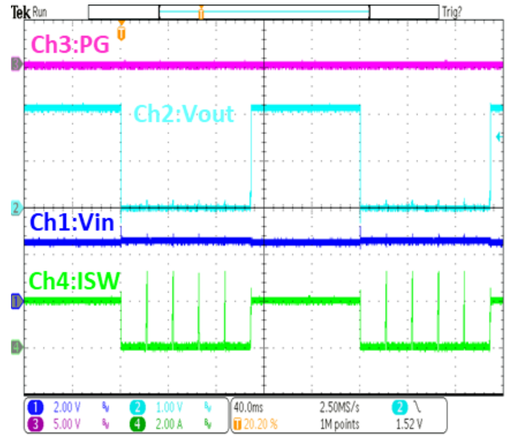
Output Short-Circuit Protection/Recover (V_{IN}=5V)



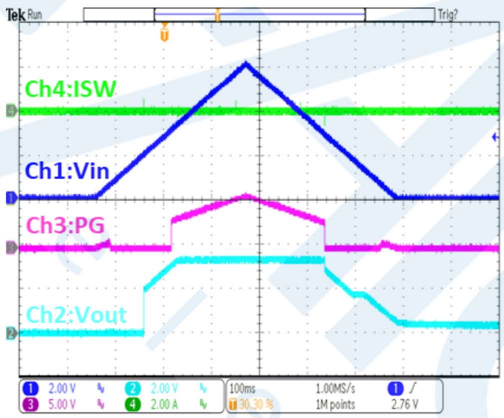
Output Short-Circuit Protection/Recover (V_{IN}=2.5V)



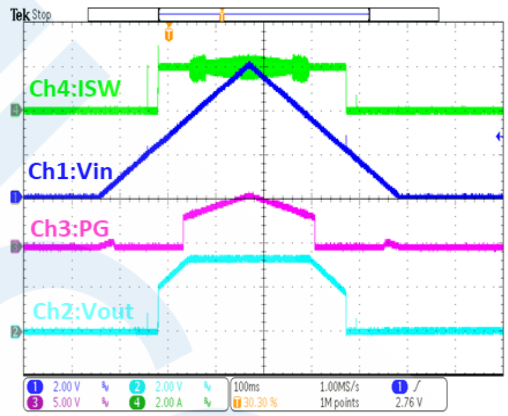
Output Short-Circuit Protection/Recover
(V_{IN}=5V, I_{OUT}=2A)



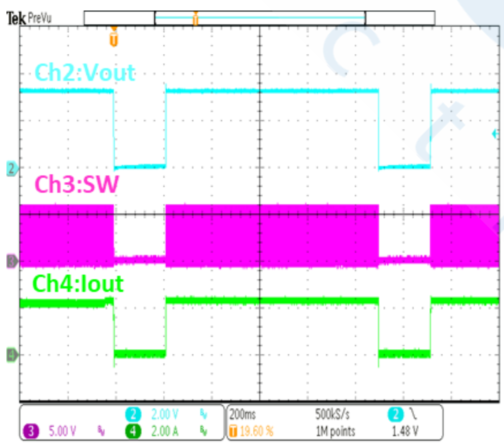
Output Short-Circuit Protection/Recover
(V_{IN}=2.5V, I_{OUT}=2A)



100% Duty Cycle Operation/Recover (No Load)



100% Duty Cycle Operation/Recover (I_{OUT}=2A)



Thermal Shutdown/Recover

Functional Description

PWM/PFM Control Operation

Depends on the output current requirement, the HT74153 realizes 3 kinds of operation modes: PWM Mode, PFM Mode and Shutdown Mode. When the light load current, the device operates in the PFM mode to reduce the input current consumption and improve the efficiency. The heavier load current drives the HT74153 enters the PWM mode automatically to keep the high efficiency and better transient response. In the Shutdown mode, the HT74153 turns off all devices to offer down to 0.1μA input current consumption.

100% Duty Cycle Operation

When the input supply voltage decreases toward the targeted output voltage, the duty cycle increases to 100% to extend the battery life, and the output voltage tracks the input voltage minus the voltage drop cross the internal High-Side MOSFET and inductor. In this condition, the PG signal is pulled low because the V_{OUT} drops to 95%.

Start-up/Soft Start

The soft start function is realized 0.7ms that smooth the output voltage and prevent the large input inrush current via controlled-charging an internal soft start capacitor during power start-up. The soft start is only activated when EN pin goes from low to high after $V_{IN} \geq 2.1V$ (V_{UVLO+}). During the soft start procedure, the OSP detection is ignored. The start-up time depends on the output capacitance and demand load current during power start-up. Note that the temperature T_j should be less than (T_{SDH}-T_{HYS}) during power start-up.

Output Voltage Setting

The external resistor divider sets the output voltage, for details see the Application Circuit. The feedback resistor, R1, also sets the feedback loop bandwidth with the internal compensation capacitor. R2 is calculated in equation below and recommended less than 200kΩ.

$$R2=R1/[(V_{OUT}/0.6V)-1] \quad (\Omega)$$

Power Good Indicator

The open-drain type output requires a pull-up resistor on the PG pin. When the output voltage is rising, the PG pin is driven down internally in soft start, shutdown periods and released until the FB voltage exceeds 95% of nominal regulation target voltage, i.e. 0.57V. In addition, there's a debounce time around 80μs after the FB voltage drops to 0.57V in order to prevent the misoperation.

Under Voltage Lock-Out Protection (UVLO)

The HT74153 implements the input Under Voltage Lock-Out (UVLO) function to prevent the misoperation during power on procedure. When the input voltage exceeds V_{UVLO+}, the converter starts operating. On the contrary, when the input voltage falls below V_{UVLO-}, the converter shuts off the output. The hysteresis voltage is designed to prevent the noise-caused reset.

Over Current Protection (OCP)

The HT74153 has a 3.2A (I_{OCP}) peak current for monitoring the internal High-Side switch (P-type MOSFET). When the OCP threshold is detected, the internal High-Side switch is turned off and the internal Low-Side switch (N-type MOSFET) is turned on until next cycle. It is used to protect the external power inductor to exceed its saturation current. When the OCP function occurs, the input peak current is limited and the output voltage is decreased.

Output Short Circuit Protection (OSP)

When the FB voltage is drop below 300mV, the HT74153 enters the output short-circuit protection (OSP) mode. In the OSP mode, the HT74153 enters the hiccup mode, disables both High/Low-Side MOSFETs and discharges the internal soft-start capacitor. After T_{OSP} rest to avoid the heating accumulation, the HT74153 reacts the soft-start procedure until the output short-circuit phenomenon ceases.

Over-Voltage Protection (OVP)

The HT74153 has an over-voltage protection function when the V_{FB} is over 660mV (V_{FB_OVP}). When the HT74153 enters the over-voltage protection function, both the high/low-side MOSFETs are disable. Until the V_{FB} is lower than V_{FB_OVP} in next cycle, the HT74153 exits the protection and the MOSFETs start to operate.

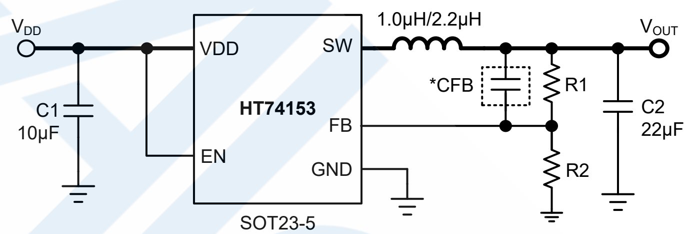
Thermal Shutdown (OTP)

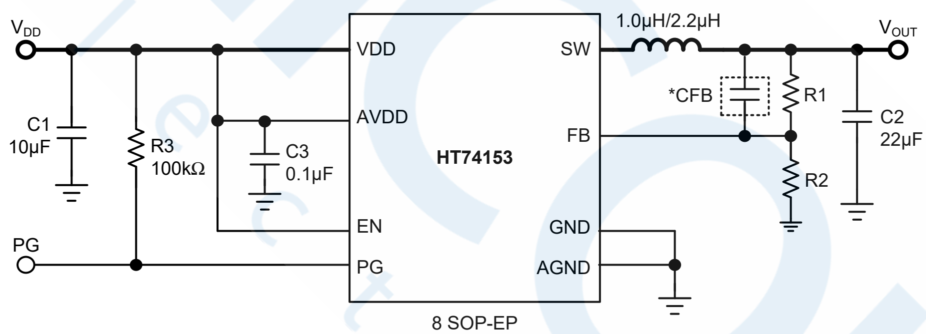
If the die temperature exceeds the internal limit threshold, T_{SHD}, the device will turn off all power MOSFETs until the temperature decreases to a specific level less than the recovery temperature, T_{HYS}.

Protection Type	Trigger Condition	V_{OUT}&PG	Recovery Condition
Under Voltage Lockout (UVLO)	V_{IN} is lower than V_{UVLO-}	V_{OUT} is 0V	V_{IN} is higher than V_{UVLO+}
		PG is LOW	
Over Current Protection (OCP)	I_L rises to I_{OCP}	V_{OUT} drop depends on duty cycle	I_L is lower than I_{OCP} in next cycle
		PG is LOW when V_{OUT} is lower 95% over 80μs	
Output Short Circuit Protection (OSP)	V_{FB} drops to V_{OSP}	V_{OUT} is 0V	V_{FB} is higher than V_{OSP} after T_{OSP}+T_{SS}
		PG is LOW when OSP is over 80μs	
Over Voltage Protection (OVP)	V_{FB} is over V_{FB_OVP}	Peak V_{OUT} is 110% V_{OUT}	V_{FB} is lower than V_{FB_OVP} in next cycle
		PG is HIGH	
Over Temperature Protection (OTP)	Tj is over T_{SHD}	V_{OUT} drops to 0V	Tj decreases to T_{HYS}
		PG is LOW when OTP is over 80μs	

List of Protection Function

Component Selection Guide





Recommended Component Values

Reference	Value	Description	Part Number	Manufacturer
C1	10μF	Capacitor, Ceramic, 10μF,10V, X7R, 0805	LMK212B7106KG-TD	Taiyo Yuden
C2	22μF	Capacitor, Ceramic, 22μF, 25V, X5R, 0805	GRM21BR61E226ME44L	Murata
C3	0.1μF	Capacitor, Ceramic, 0.1μF, 50V, X5R, 0603	0603B104K500CT	Walsin
*CFB	47pF	Capacitor, Ceramic, 47pF, 50V, NPO, 0603	GRM1885C1H470JA01D	Murata
L1	1.0μH	Inductor, 7.1mΩ, I_{Rate}=14.1A, 7.1mm×6.5mm×3mm	SPM6530T-1R0M120	TDK
	2.2μH	Inductor, 17.3mΩ, I_{Rate}=8.4A, 7.1mm×6.5mm×3mm	SPM6530T-2R2M	TDK
R3	100kΩ	Resistor, Chip, 1%, 0603		

V_{OUT} (V)	Package	R1 (kΩ)	R2 (kΩ)
1.8		400 (±1%)	200 (±1%)
2.5		630 (±1%)	200 (±1%)
2.7	SMD 0603	700 (±1%)	200 (±1%)
3.0		800 (±1%)	200 (±1%)
3.3		900 (±1%)	200 (±1%)

Note: 1. V_{OUT}=0.6V×(R1+R2)/R2.

2. *CFB option is recommended to refer the "Application Information-Load Transient Compensation Design" chapter.

Power Inductor

Use an inductor with a DC current rating at least 25% percent higher than the maximum load current for most applications. The DC resistance of the inductor is a key parameter for the efficiency. Concerned efficiency, the inductor's DC resistance should be less than 200mΩ. For most application, the inductor value can be calculated from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{ripple} \times f_{SW}}$$

A higher value of ripple current reduces the inductance value, but increases the conductance loss, core loss, and current stress for the inductor and switch devices. A suggest choice is for the inductor ripple current to be 30% of the maximum load current.

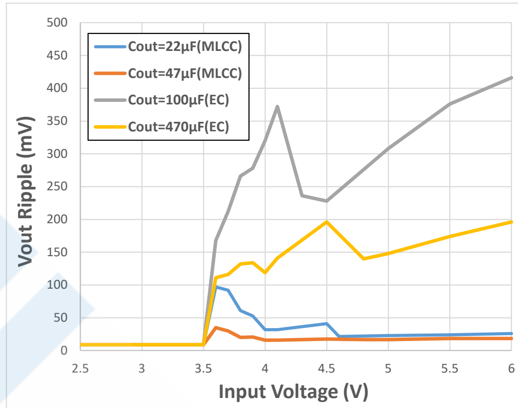
Input Capacitor

A low ESR ceramic capacitor, C_{IN}, is needed between the VIN pin and GND pin. Use ceramic capacitors with X5R or X7R dielectrics for their low ESRs and small temperature coefficients. For most applications, above 10µF capacitor will sufficient.

Output Capacitor

The selection of C_{OUT} is driven by the maximum allowable output voltage ripple. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR characteristics. The capacitor value is good starting point with an ESR or 0.1Ω or less and should be over 22µF.

The selection of COUT is driven by the maximum allowable output voltage ripple. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR characteristics. The capacitor value is good starting point with an ESR or 0.1Ω or less and capacitance should be in the range of 10µF to 470µF. It is neccecery to use MLCC in low output voltage ripple application. Only ceramics have the extremely low ESR that is needed to. The comparison of low ESR and non-low ESR is shown in Fig.1.



Application Information

Interference Consideration

If the external interference or PCB noise is too high in the application environment, causing output voltage too high, it is recommended that the FB resistor set as 1/10 of the recommended value table, it is also recommended a large ground plane to improve PCB noise and long-term reliability. C3, R1, R2 loop as close as possible to the HT74153.

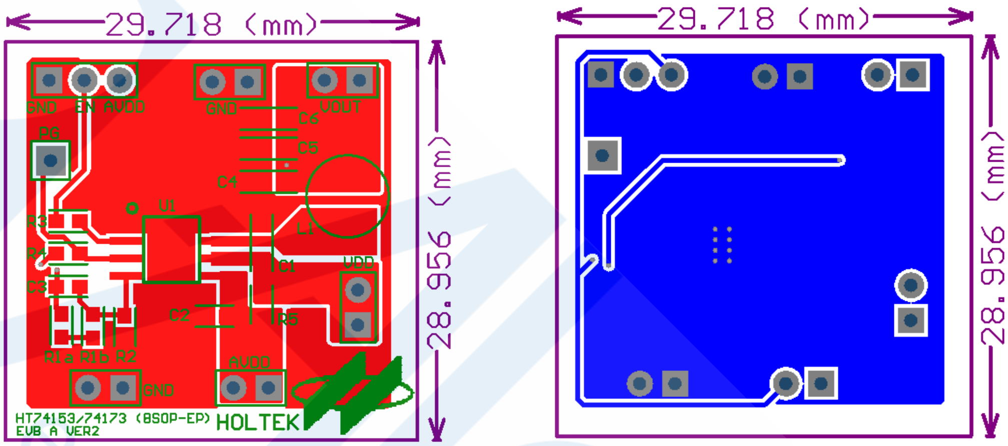
Load Transient Compensation Design

The HT74153 utilizes current-mode control to regulate the output voltage. When a load step occurs, PFM/PWM control logic takes several cycles to respond to a step in load current, causing output voltage rapid drop. Thus, adding a 47pF capacitor CFB will improve output voltage drop when load transient occurs.

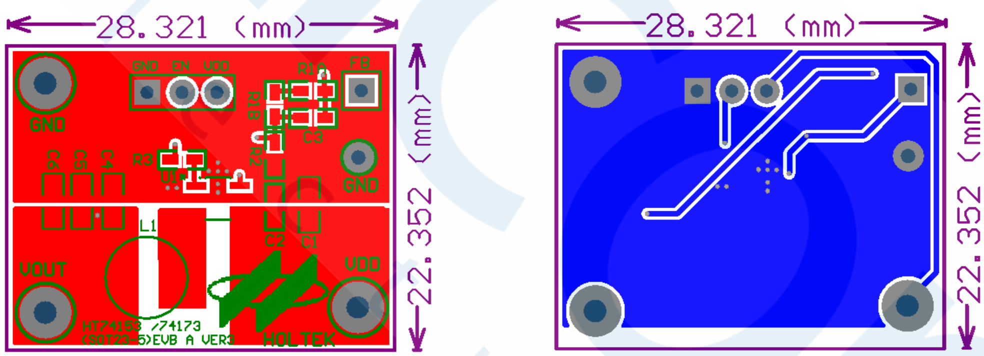
Layout Consideration Guide

To achieve the best efficiency and to reduce the conducted noise, there are some important points to note regarding the PCB layout.

1. The input/output capacitors and the inductor should be placed as close as possible to the IC.
2. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the FB pin as possible, but should not be close to the SW nodes to avoid noise interference.
3. L1 should be placed as close to the IC as possible. Minimize the noise from the switch node.
4. Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.



8SOP-EP PCB Layout Example



SOT23-5 PCB Layout Example

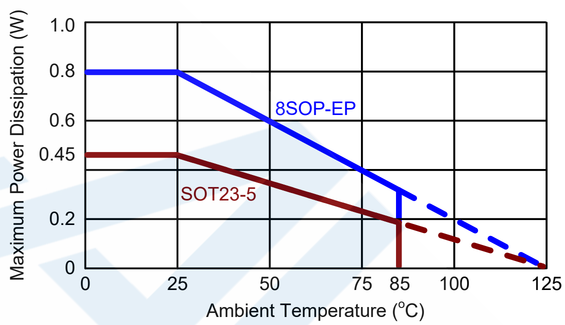
Thermal Considerations

The maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of the surrounding airflow and the allowed difference between the junction and ambient temperatures. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_a) / \theta_{JA} \quad (W)$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_a is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance of IC package (125°C/W for 8-pin SOP-EP).

For maximum operating rating conditions, the maximum junction temperature is 150°C. However, it's recommended that the maximum junction temperature does not exceed 125°C in normal operation to keep high reliability. The derating curve of maximum power dissipation is as follows:



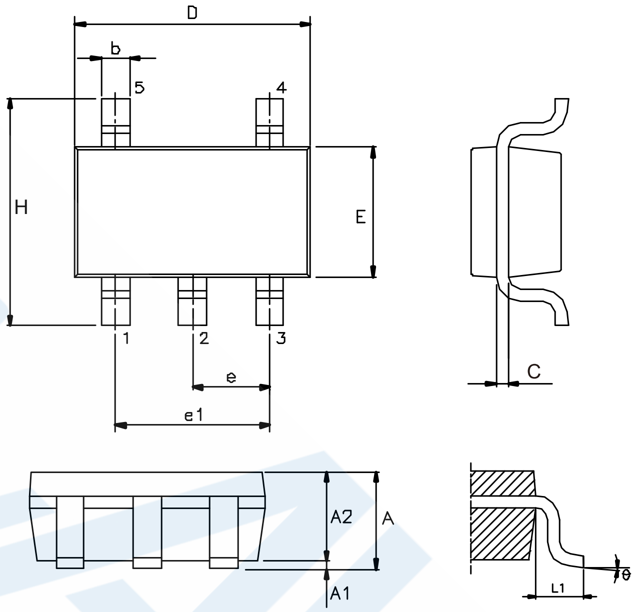
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

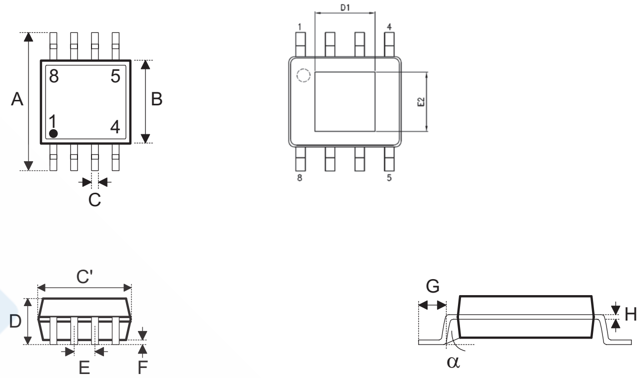
5-pin SOT23 Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.057
A1	—	—	0.006
A2	0.035	0.045	0.051
b	0.012	—	0.020
C	0.003	—	0.009
D	—	0.114 BSC	—
E	—	0.063 BSC	—
e	—	0.037 BSC	—
e1	—	0.075 BSC	—
H	—	0.110 BSC	—
L1	—	0.024 BSC	—
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.45
A1	—	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
C	0.08	—	0.22
D	—	2.90 BSC	—
E	—	1.60 BSC	—
e	—	0.95 BSC	—
e1	—	1.90 BSC	—
H	—	2.80 BSC	—
L1	—	0.60 BSC	—
θ	0°	—	8°

8-pin SOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C′	—	0.193 BSC	—
D	—	—	0.069
D1	0.059	—	—
E	—	0.050 BSC	—
E2	0.039	—	—
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C′	—	4.90 BSC	—
D	—	—	1.75
D1	1.50	—	—
E	—	1.27 BSC	—
E2	1.00	—	—
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°