V6/22

HT32F65540G Datasheet

32-Bit Arm® Cortex®-M0+ BLDC Microcontroller with 3-channel 48 V Half-bridge Gate-Driver, up to 64 KB Flash and 8 KB SRAM with 1 MSPS ADC, CMP, OPA, USART, UART, SPI, I^{2}C, MCTM, GPTM, SCTM, BFTM, CRC, LSTM, WDT, DIV and PDMA

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1 General Description

The Holtek HT32F65540G device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The device operates at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides 64 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, ADC, OPA, CMP, I^{2}C, USART, UART, SPI, MCTM, GPTM, SCTM, BFTM, CRC-16/32, LSTM, WDT, PDMA, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The device also includes a gate-driver for 3-phase motor driving applications. The gate-driver has several internal protection functions and provides an integrated 5 V low quiescent current LDO which can provide power supply for internal and external circuits.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as electric scooters, kitchen ventilators, ceiling fans, dust-free room fan filter units, other various fans and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- 64 KB on-chip Flash memory for instruction/data and options storage
- 8 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator to obtain maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions, pre-fetch buffer and branch cache for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming / page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-Out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 5.0 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include High Speed Internal RC oscillator (HSI), High Speed External crystal oscillator (HSE), Low Speed Internal RC oscillator (LSI), Phase Lock Loop (PLL), HSE clock monitor, clock prescaler, clock multiplexer, APB clock divider and gating circuitry. The clocks of AHB, APB and Cortex®-M0+ are derived from system clock (CK_SYS) which can come from HSI, HSE, LSI or system PLL. Watchdog Timer (WDT) and Low Speed Timer (LSTM) use the LSI as their clock source.

Power Management Control Unit – PWRCU

- V_{DD} power supply: 2.5 V to 5.5 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} and V_{CORE} power domains
- Two power saving modes: Sleep and Deep-Sleep modes

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides two types of power saving modes which are the Sleep and Deep-Sleep modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

Gate-Driver

- Wide power supply range: V_{CC} = 6 V ~ 40 V
- Maximum motor sustainable voltage up to 48 V
- 3-channel half-bridge driver: Drives 3 high-side and 3 low-side N-type MOSFETs
- Integrated 5 V LDO regulator (V_{REG}) with 50mA output drive current
- Integrated gate-driver power supplies:
  - High-side bootstrap driving: supports up to 50 kHz PWM operation
  - Low-side driving: 12 V linear regulator (V_{12P})
- Integrated 120ns fixed dead time control
- High-side and low-side gate-driver control
  - High-side: High active (INHx)
  - Low-side: Low active ($\overline{\text{INLx}}$)
- Protection features
  - V_{CC} Under Voltage Lock-Out (VCC_UVLO)
  - V_{BSTx} Under Voltage Lock-Out (VBST_UVLO)
  - V_{12P} Under Voltage Lock-Out (V12P_UVLO)
  - V_{REG} Under Voltage Lock-Out (VREG_UVLO)
  - Over Temperature Protection (OTP)

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 7 external analog input channels for each ADC

Two 12-bit multi-channel Analog to Digital Converter are integrated in the device. There are multiplexed channels, which include 7 external channels on which the external analog signal can be supplied and 4 internal channels. If the input voltage is required to remain within a specific threshold window, the Analog Watchdog function will monitor and detect the signal. An interrupt will then be generated to inform the device that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot, continuous and discontinuous conversion mode.

Operational Amplifier – OPA

- Rail-to-rail operational amplifier
- Fixed dedicated I/O pins
- Internal output paths to A/D converter or comparator

Two Operational Amplifiers (OPA0~OPA1) are implemented within the device.

Comparator – CMP

- Three Rail-to-rail comparators
- Each comparator has configurable negative inputs used for flexible voltage selection
  - Dedicated I/O pin
  - Internal voltage reference provided by 6-bit scaler
- Programmable hysteresis
- Programmable response speed and consumption
- Comparator output can be output to I/O or to multiple timer or ADC trigger inputs
- 6-bit scaler can be configurable to dedicated I/O for voltage reference
- Comparator n inverting input can be from CMP0N, CMPnN or CVREF
- Interrupt generation capability with wakeup from Sleep or Deep Sleep mode through the EXTI controller

Three general purpose comparators (CMP) are implemented within the device. They can be configured either as standalone comparators or combined with the different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or waking up the MCU from the Sleep or Deep Sleep mode through EXTI wakeup event management unit.

I/O Ports – GPIO

- Up to 26 GPIOs
- Port A, B, C are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 26 General Purpose I/O pins, GPIO for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Break input signals to assert the timer output signals in reset state or in a known state

The Motor Control Timer Module, MCTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes which include input signal pulse width measurement, output waveform generation for signals such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder and Pulse/Direction Mode
- Master/Slave mode controller

The General-Purpose Timer Module, GPTM, consists of one 16-bit up / down-counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM also supports an Encoder Interface using a quadrature decoder with two inputs.

Single-Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single-Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

Basic Function Timer – BFTM

- 32-bit compare match up-counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shots or generate repetitive interrupts. The BFTM can operate in two modes, repetitive and one shot modes. In the repetitive mode, the counter will restart at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provide reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuitry that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Low Speed Timer – LSTM

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up control

The Low Speed Timer, LSTM, circuitry includes the APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. The LSTM circuits are located in the V_{CORE} power domain. When the device enters the power-saving mode, the LSTM counter is used as a wakeup timer to let the system resume from the power saving mode.

Inter-Integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I^2C module is an internal circuit allowing communication with an external I^2C interface which is an industry standard two-wire serial interface used for connection to external hardware. These two serial lines are known as a serial data line SDA, and a serial clock line SCL. The I^2C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation registers are used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I^2C module also has an arbitration detection and clock synchronization function to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to ($f_{PCLK}/2$) MHz for the master mode and ($f_{PCLK}/3$) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line SCK, and the slave select line SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive the data bits, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to (f_{PCLK}/16) MHz for Asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes an 8-level transmitter FIFO, (TX_FIFO) and an 8-level receiver FIFO (RX_FIFO). The software can detect a USART error status by reading USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation done in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports Linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger sources:
  ADC, SPI, USART, UART, I²C, MCTM, GPTM, SCTM and software request

The Peripheral Direct Memory Access circuitry, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and requires a software triggered start signal by controlling the "START" bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

Package and Operation Temperature

- 48-pin LQFP-EP package
- Operation temperature range: -40 °C to 105 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F65540G
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		8
Timers	MCTM	1
	GPTM	1
	SCTM	4
	BFTM	2
	WDT	1
	LSTM	1
Communication	USART	1
	UART	1
	SPI	1
	I^2C	1
PDMA		6 channels
Hardware Divider		1
CRC-16/32		1
EXTI		16
12-bit ADC		2
Number of channels		7 channels
Comparator		3
Operational Amplifier		2
GPIO		Up to 26
CPU frequency		Up to 60 MHz
Power supply (V_{CC})		6 V ~ 40 V
Operating voltage (V_{DD})		2.5 V ~ 5.5 V
5 V LDO output driving current		50 mA
Operating temperature		-40 °C ~ 105 °C
Package		48-pin LQFP-EP

Block Diagram

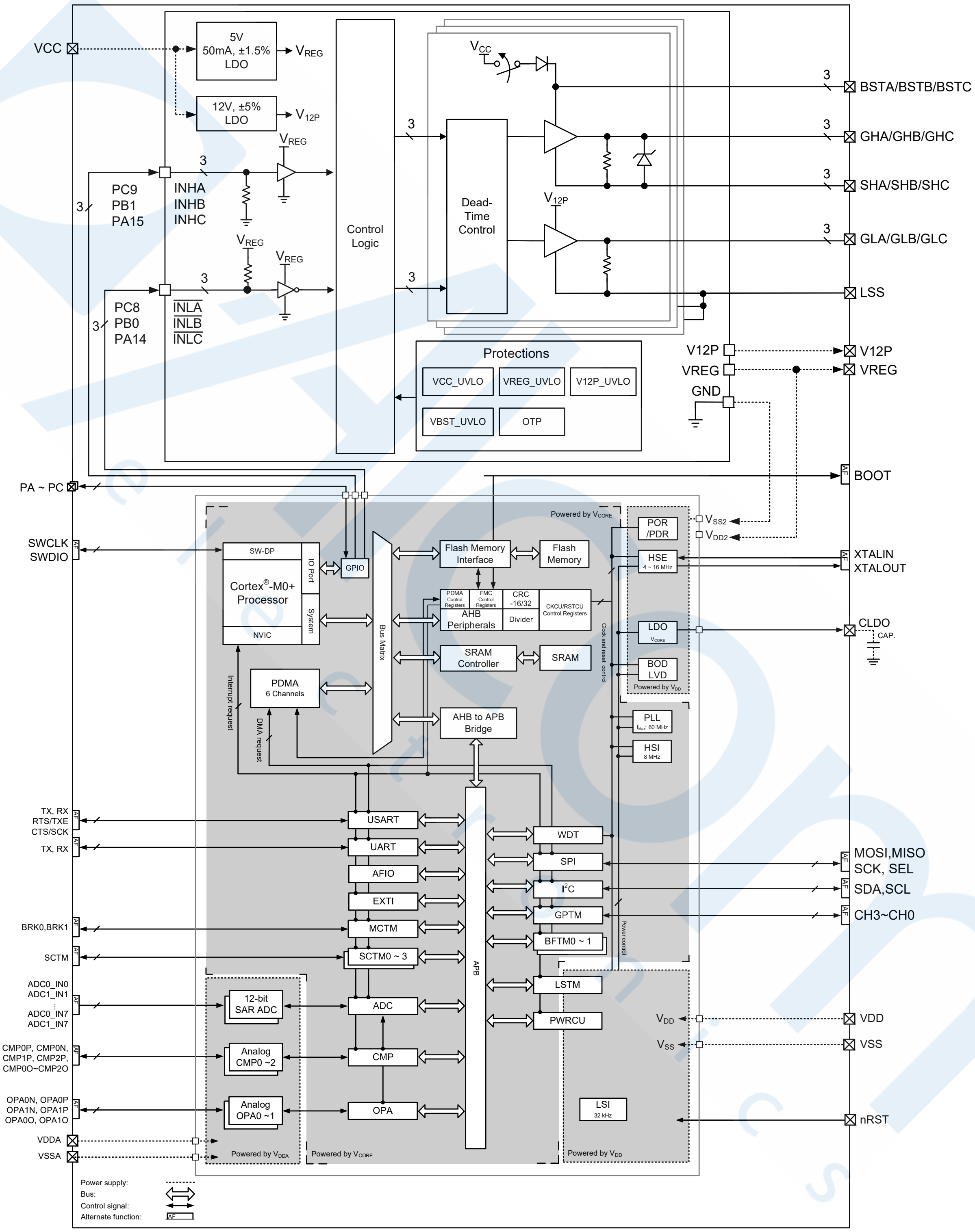


Figure 1. Block Diagram

Memory Map

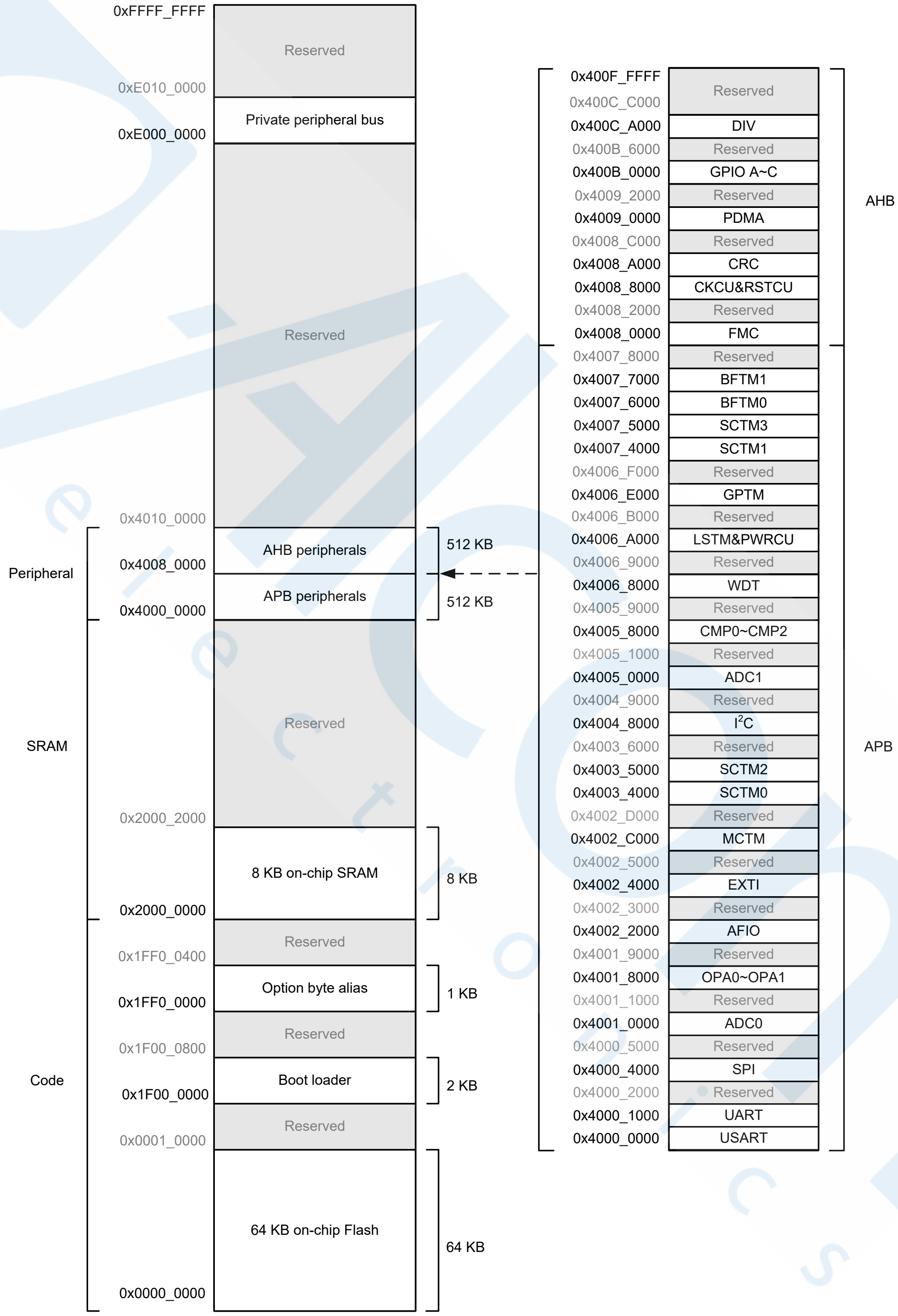


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC0	
0x4001_1000	0x4001_7FFF	Reserved	
0x4001_8000	0x4001_8FFF	OPA0 ~ OPA1	
0x4001_9000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4004_FFFF	Reserved	
0x4005_0000	0x4005_0FFF	ADC1	
0x4005_1000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	CMP0 ~ CMP2	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	LSTM&PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU&RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

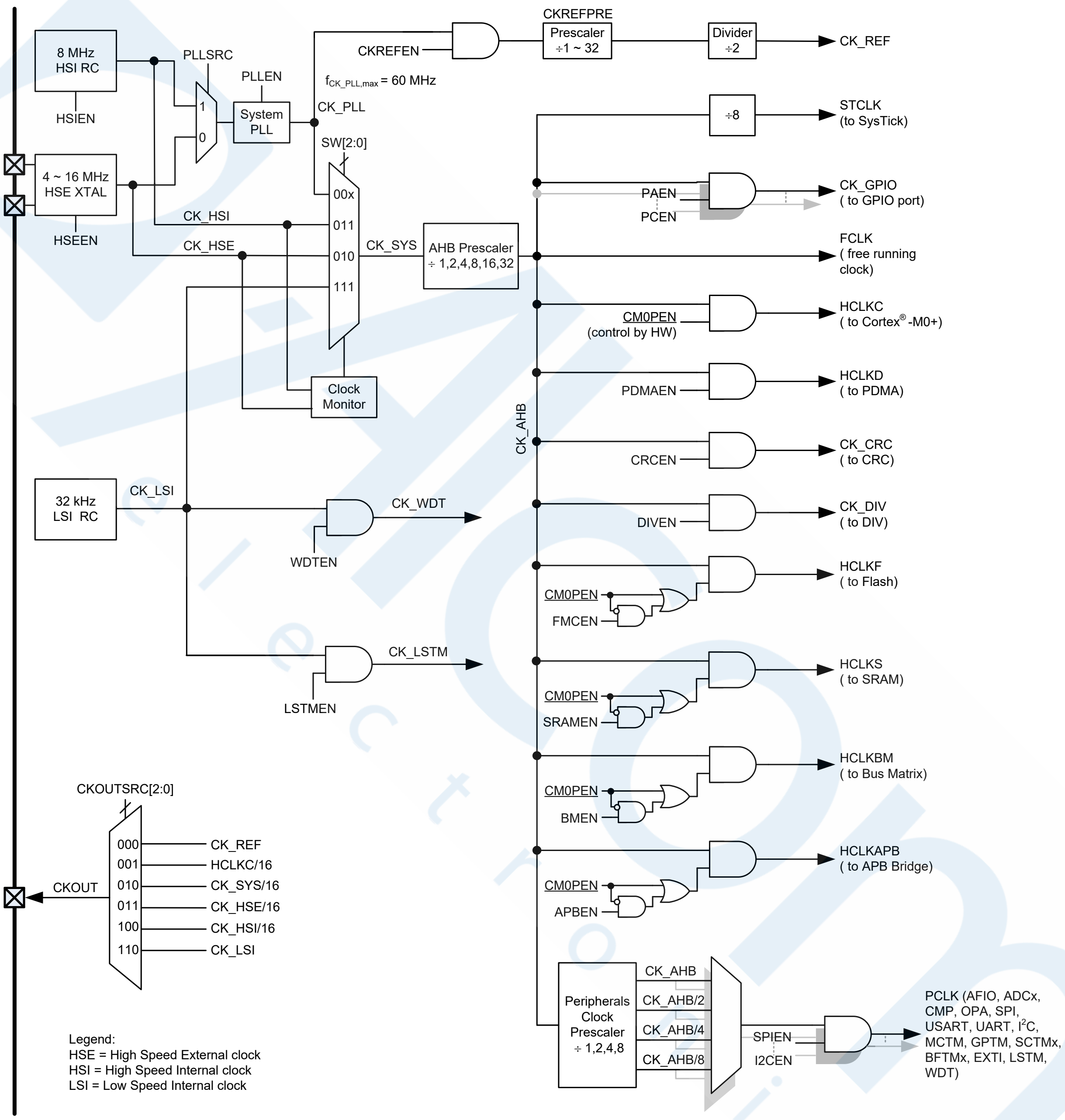


Figure 3. Clock Structure

4 Gate-Driver

The device includes a 3-channel gate-driver, which can be used for external high-side and low-side N-channel MOSFET driving. It includes a 5 V LDO, a 12 V LDO, 3-channel high-side and low-side gate-driver circuits. The gate-driver also has five protection functions, which are Power Supply Input Under Voltage Lock-Out, 5 V LDO Output Under Voltage Lock-Out, 12 V LDO Output Under Voltage Lock-Out, Bootstrap Output Under Voltage Lock-Out and Over Temperature Protection, to avoid abnormal output situations.

The input signals of INHx and $\overline{\text{INLx}}$ are input to the control logic which will determine the high-side and low-side gate-driver outputs. The INHx has an internal pull-down resistor and the $\overline{\text{INLx}}$ has an internal pull-up resistor. Additionally, there is a fixed dead time insertion when switching between the high-side and low-side gate driving to avoid short-circuit between V_{CC} and ground.

The gate-driver output voltage will vary with the power supply when V_{CC} is less than 13 V. When V_{CC} is greater than 13 V, the gate-driver output will be clamped to 12 V, providing a 0.7 A peak source current and a 1 A peak sink current. Either high-side and low-side gate has an internal hold-off resistor in order to avoid misconduction of external power MOSFET due to interference when the power is off.

The gate-driver also has integrated bootstrap diodes for bootstrap circuit implementation, allowing reduced system component requirements.

5 V Voltage Regulator

The integrated 5 V LDO can supply power for both internal and external circuits, with a output current over 50mA. The LDO will act as a fully turned on switch when the power supply V_{CC} is less than 5 V, in which condition its output voltage is almost equal to the power supply if there is no load.

12 V Voltage Regulator

The integrated 12 V LDO, which supplies power for the low-side gate-drivers, cannot be used as power supply for external circuits.

Bootstrap Circuit Operation

The gate-driver uses 3 sets of bootstrap circuits as floating power supplies to power the high-side gate-driver circuits.

Each set of bootstrap circuit is composed of an external bootstrap capacitor, C_B, and an internal bootstrap diode, D_{BOOT}. The charging current path of the bootstrap capacitor in common applications is shown in Figure 4. The bootstrap capacitor is charged after the low-side power MOSFET is turned on. After the gate-driver is enabled, an input command of INHx = $\overline{\text{INLx}}$ = 'L' should be arranged before switching to the high-side power MOSFET for the first time, so that the low-side power MOSFET will be turned on for a period of time to charge the bootstrap capacitor. As shown in Figure 5, the high-side gate-driver output could not be controlled by inputs until the bootstrap capacitor has been charged exceeding the bootstrap under voltage lock-out threshold, V_{BST_UVLO+}. It is recommended to charge the bootstrap capacitor to the steady-state voltage of V1 before proceeding. The equation for estimating the charging time t_{BST} of the bootstrap capacitor is as follows:

$$t_{BST}\ (ms) > 0.3 + 1.1 \times C_B\ (\mu F) \div 2.2$$

Where C_B is the bootstrap capacitance. The larger the capacitance, the longer it will take to charge. For example, the charging time t_{BST} should be at least 1.5 ms for a capacitance of 2.2 µF. After the charging is completed, the bootstrap voltage will reach the steady-state voltage V1, as shown in Figure 5. When the power supply V_{CC} is less than or equal to 13 V, V1 will change along with V_{CC}. Then V1 will be clamped to a fixed value of 12 V once V_{CC} is larger than 13 V. V1 is calculated as follows:

$$V1 = 12\ V \quad \text{when } V_{CC} > 13\ V$$

$$V1 = V_{CC} - 1.5\ V \quad \text{when } V_{CC} \leq 13\ V$$

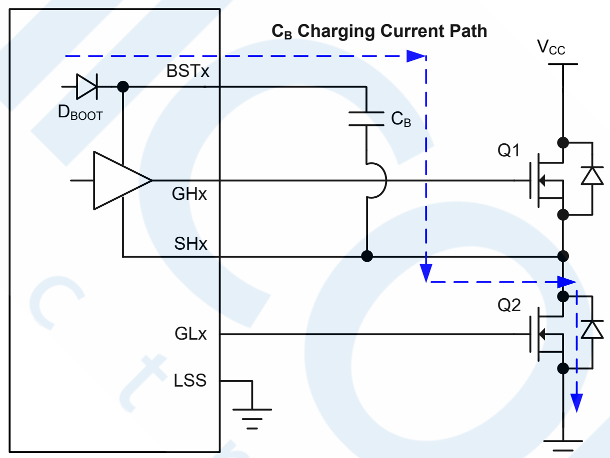
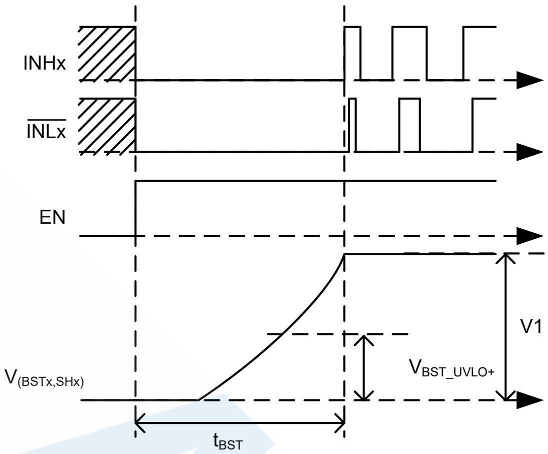


Figure 4. Bootstrap Capacitor (C_B) Charging Current Path



Note: "EN" in the figure is the gate-driver enable signal. After power on, EN is fixed high.

Figure 5. Bootstrap Capacitor Charging Time (t_{BST})

The charge stored in the bootstrap capacitor, C_B, is discharged during the high-side gate-driver output and the internal bootstrap diode, D_{BOOT}, is used to avoid current backflow, as shown in Figure 6. When discharging, pay attention to whether the bootstrap capacitance value is sufficient. If the bootstrap capacitance value is too small, it will affect the high-side gate driving capability. Refer to the "Component Selections" chapter for the bootstrap capacitance recommendation.

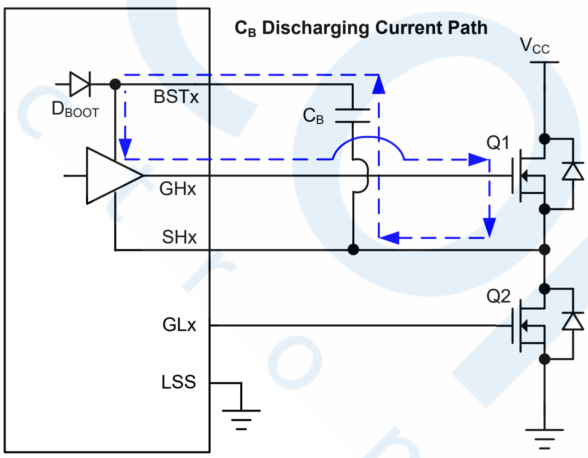


Figure 6. Bootstrap Capacitor (C_B) Discharging Current Path

Gate-Driver Control Logic

As a gate-driver for driving high-side and low-side N-channel MOSFETs, the control signals are input from INHx, $\overline{\text{INLx}}$. Usually a 6-wire input control method is used, where the dead time width is determined by the control signals but has a minimum value equal to the fixed dead time designed in the device.

Pay attention to whether the fixed dead time is sufficient when switching between the high-side and low-side power MOSFETs so that the power supply V_{CC} will not be short-circuited to the ground.

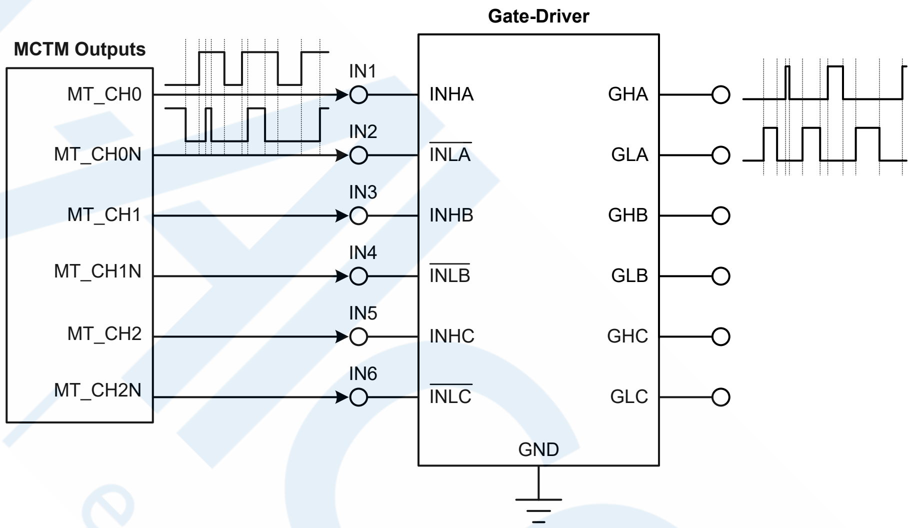


Figure 7. 6-Wire Control

Both high-side and low-side gate-driver outputs are controlled by the INHx and $\overline{\text{INLx}}$ input signals. For example, the on/off true table of the external N-channel power MOSFETs is shown as follows.

Table 3. Gate-Driver Operation Truth Table

EN (2)	INHx	$\overline{\text{INLx}}$	GHx-to-SHx	GLx-to-LSS	External H/S (1) Power MOSFET	External L/S (1) Power MOSFET
0	X	X	L	L	OFF	OFF
1	0	0	L	H	OFF	ON
1	0	1	L	L	OFF	OFF
1	1	0	L	L	OFF	OFF
1	1	1	H	L	ON	OFF

Note: 1. H/S indicates High-Side, L/S indicates Low-Side.
2. EN is always "1" after the gate-driver is powered up.

Protection Function Operation

When the device operates in an abnormal situation, such as a power supply input under voltage lock-out, bootstrap output under voltage lock-out, 12 V LDO output under voltage lock-out, 5 V LDO output under voltage lock-out or over temperature condition has occurred, it will activate the corresponding protection mechanism to turn off the affected N-channel power MOSFET. The protection mechanisms are summarized below.

Table 4. Protection Function Conditions

Protection	Protection Entry Condition	Protection Reaction				Release Condition
		V_{12P}	GHx-to-SHx	GLx-to-LSS	Bootstrap Function	
VCC_UVLO	$V_{CC} < V_{CC\_UVLO-}$	0V	L	L	Disable	$V_{CC} \geq V_{CC\_UVLO+}$
VBST_UVLO	$V_{(BSTx,SHx)} < V_{BST\_UVLO-}$	—	L	—	Keep Active	$V_{(BSTx,SHx)} \geq V_{BST\_UVLO+}$
V12P_UVLO	$V_{12P} < V_{12P\_UVLO-}$	—	—	L	Disable	$V_{12P} \geq V_{12P\_UVLO+}$
VREG_UVLO	$V_{REG} < V_{REG\_UVLO-}$	—	L	L	Disable	$V_{REG} \geq V_{REG\_UVLO+}$
OTP	$T_j > T_{SHD}$	—	L	L	Disable	$T_j \leq T_{REC}$

Power Supply Input Under Voltage Lock-Out – VCC_UVLO

This integrated protection function is to avoid unstable gate-driver output when the power supply voltage falls to a certain low level. During V_{CC} power-on period, both high-side and low-side power MOSFETs are turned off before the power supply voltage reaching the threshold V_{CC_UVLO+}. When the power supply voltage is greater than V_{CC_UVLO+}, the gate-driver outputs are determined by the input signals. If the power supply voltage falls below the under voltage lock-out threshold V_{CC_UVLO-}, both high and low-side power MOSFETs will remain off.

Bootstrap Output Under Voltage Lock-Out – VBST_UVLO

This integrated protection function is to avoid that when the bootstrap capacitor is insufficiently charged, the output voltage of the high-side gate-driver will be insufficient making the high-side power MOSFET fully turned on. When the bootstrap output voltage is larger than the threshold V_{BST_UVLO+}, the high-side gate-driver output is determined by the input signals. If the bootstrap output voltage falls below the under voltage lock-out threshold V_{BST_UVLO-}, the high-side power MOSFET will remain off.

12 V LDO Output Under Voltage Lock-Out – V12P_UVLO

When the internal 12 V LDO output voltage, V_{12P}, is too low, the integrated 12 V LDO output under voltage lock-out function will be activated to avoid that the output voltage of the low-side gate-driver is insufficient making the low-side power MOSFET fully turned on. After V_{12P} exceeds the threshold V_{12P_UVLO+}, the low-side gate-driver output is determined by the input signals. If V_{12P} is less than the under voltage lock-out threshold V_{12P_UVLO-}, the low-side power MOSFET will remain off.

5 V LDO Output Under Voltage Lock-Out – VREG_UVLO

When the internal 5 V LDO output voltage, V_{REG}, is too low, the integrated 5 V LDO output under voltage lock-out function will be activated to avoid unstable signals input from the external controller. After V_{REG} exceeds the threshold V_{REG_UVLO+}, the gate-driver output is determined by the input signals. If V_{REG} is less than the under voltage lock-out threshold V_{REG_UVLO-}, both high and low-side power MOSFETs will remain off.

Over Temperature Protection – OTP

If the internal junction temperature of the gate-driver exceeds the limit threshold T_{SHD}, the high-side and low-side power MOSFETs will be turned off until the junction temperature drops below the recovery temperature level, T_{REC}, at which the gate-driver output is determined by the input signals.

Component Selections

Gate Resistor Circuit

The main function of the gate resistors, R_{G1}, R_{G2}, R_{G3} and R_{G4}, is to reduce the vibration of U, V, W output voltages and reduce the EMI noise generation. Adjusting R_{G1} and R_{G3} controls the on time of the high-side and low-side switches, adjusting R_{G2} and R_{G4} controls the off time of the high-side and low-side switches. The gate resistors are optional and can be used according to the requirements.

It is recommended to select the gate resistance value according to the desired gate voltage rising time (t_r) or falling time (t_f), which are shown in the figure below. R_{G1}, R_{G2}, R_{G3} and R_{G4}, if used, are recommended to have a typical value of 10 Ω ~ 200 Ω. It is recommended to use a 1N4148 switch diode for both D_{G1} and D_{G2}.

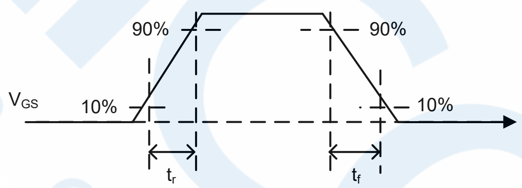


Figure 8. Gate Voltage (V_{GS}) Rising Time (t_r) and Falling Time (t_f)

Bootstrap Capacitor

The power stored in the bootstrap capacitor, C_B, services as a floating power supply for the high-side gate-driver circuit. Generally speaking, the bootstrap capacitance value is recommended to be more than 50 times the input power capacitance value of the high-side power MOSFET, and is recommended to be at least 2.2 μF.

Current Sensing Resistors

The current sensing resistors, R_{S1}, R_{S2} and R_{S3}, turn the current flowing through them into a voltage for the controller to detect. The current sensing resistors are optional and can be used according to the requirements. It is recommended that the current sensing resistors be used when the cross voltage is less than 0.5 V.

Pay attention to the power that the current sensing resistor can withstand, P_{RS}, which is calculated by $P_{RS} = R_S \times I_{RMS}^2$, where R_S is the resistance value, I_{RMS} is the effective value of the current flowing through the resistor. The package of the current sensing resistor should be selected based on the power calculated above.

Gate-Driver Supply Capacitor

The power supply regulator capacitor, C1, can reduce input voltage fluctuation. It is recommended to use at least a 4.7 μF capacitor.

Power Supply Bypass Capacitor

When the board power supply is mains, the power supply bypass capacitor, C5, can filter out the high-frequency noise input from the power supply. It is recommended to use a 0.1 μF capacitor. This capacitor is optional and can be used according to the requirements.

Power Supply Input Series Resistor

In order to keep the junction temperature of the gate-driver within the operating range and maintain a stable output, it is necessary to distribute the power dissipation of the gate-driver through the power supply series resistor, R1, so that the total power dissipation P_D would not exceed the maximum power dissipation $P_{D(MAX)}$. This resistor is optional and can be used or not according to needs. Usually, when the power dissipation P_D of the gate-driver exceeds the maximum allowable power dissipation $P_{D(MAX)}$, over temperature protection will occur. it is recommended to use a 150 Ω resistor for R1 and a package that can withstand at least 0.5 W for the resistor.

RC Snubbers

In order to prevent the 3-channel U, V, W output voltages from vibrating too much and to reduce EMI, an RC snubber circuit composed of R_{SN} and C_{SN} can be used to reduce the peak value and frequency of the vibration. R_{SN} and C_{SN} should be designed based on the actual board parasitic inductance and parasitic resistance. The capacitor and resistor are optional and can be used according to requirements.

Motor Supply Capacitor

The motor power supply capacitor, C4, can absorb the current that is fed back to the V_{CC} power supply when the motor is running, and can also provide a transient power for motor to compensate for the power response speed or the influence of external wire length. It is recommended to use at least a 22 μF capacitor.

12 V LDO Output Capacitor

The 12 V LDO output regulator capacitor, C2, can reduce the voltage ripple of the 12 V LDO output. It is recommended to use at least a 2.2 μF capacitor.

5 V LDO Output Capacitor

The 5 V LDO output regulator capacitor, C3, can reduce the voltage ripple of the 5 V LDO output. It is recommended to use at least a 2.2 μF capacitor.

Voltage Clamp Circuit

In order to prevent IC damage or malfunction when a large negative SHx transient occurs, a voltage clamp circuit can be used to reduce the negative SHx spike. It is recommended to use a 2.2 Ω resistor, R_{SH}, and 1N5819 schottky diode, D_{SH}.

5 Pin Assignment

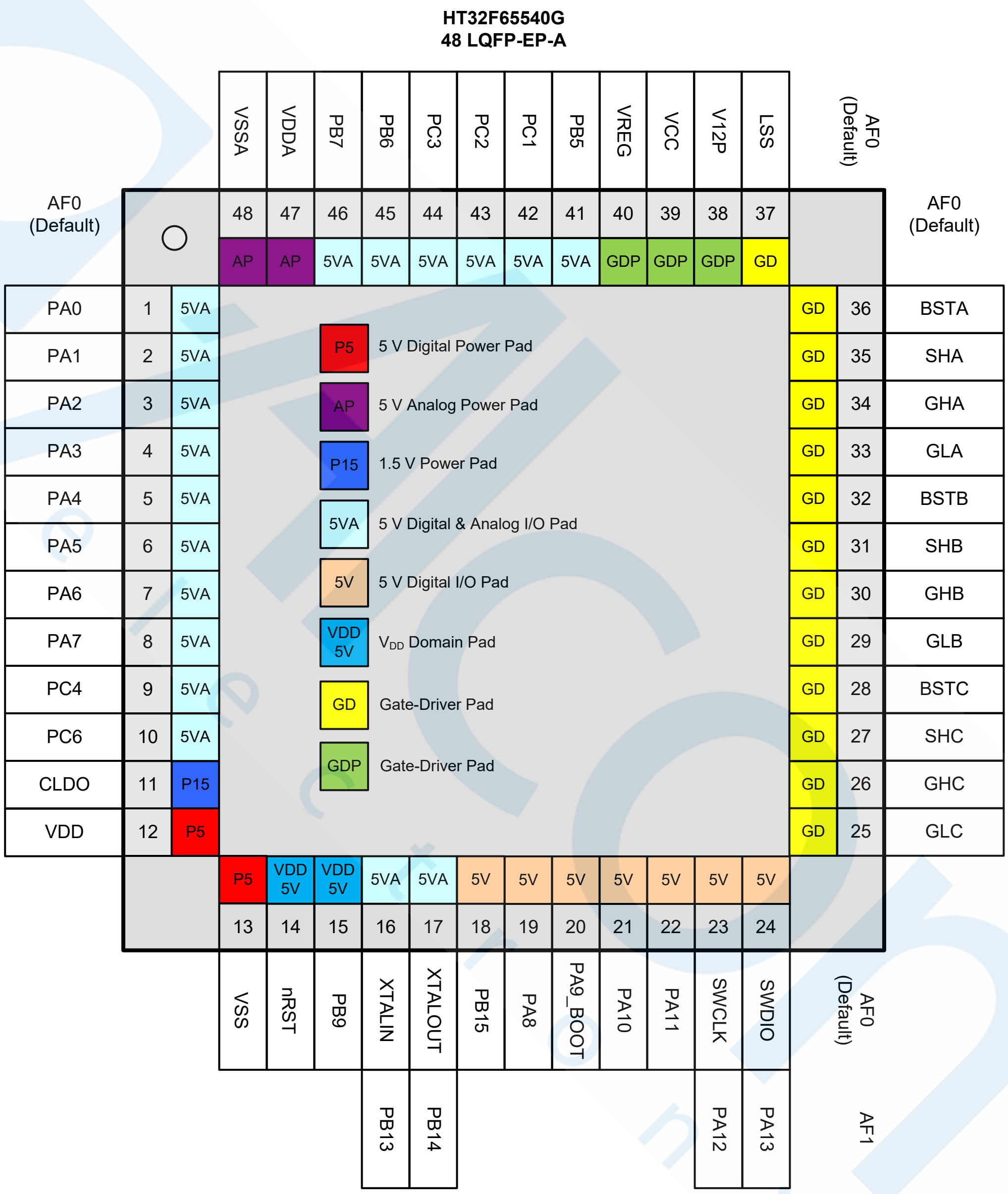


Figure 9. 48-pin LQFP-EP Pin Assignment

Table 5. Pin Alternate Function

Package	Alternate Function Mapping															
	AF0	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**	**AF8**	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
48 LQFP-EP	**System Default**	**GPIO**	**ADC0**	**ADC1**	**GPTM /MCTM**	**SPI**	**USART /UART**	**I^2C**	**CMP /OPA**	**N/A**	**N/A**	**N/A**	**N/A**	**SCTM**	**N/A**	**System Other**
1	PA0		ADC0_IN5	ADC1_IN1										SCTM0		
2	PA1		ADC0_IN6	ADC1_IN2			USR_RX							SCTM1		
3	PA2		ADC0_IN7	ADC1_IN3	MT_BRK0	SPI_SCK										
4	PA3			ADC1_IN4	MT_BRK1	SPI_SEL	USR_TX		CMP0O							
5	PA4			ADC1_IN5		SPI_MISO	UR_TX	I2C_SCL	CMP1O					SCTM2		
6	PA5			ADC1_IN6		SPI_MOSI	UR_RX	I2C_SDA	CMP2O					SCTM3		
7	PA6			ADC1_IN7					CMP0P							
8	PA7				GT_CH0	SPI_SEL			CMP0N							
9	PC4				GT_CH1		USR_RTS		CMP1P							
10	PC6				GT_CH3	SPI_MOSI	UR_TX		CMP2P							
11	CLDO															
12	VDD															
13	VSS															
14	nRST															
15	PB9					SPI_SCK	USR_RTS	I2C_SCL						SCTM1		
16	XTALIN	PB13														
17	XTALOUT	PB14														
18	PB15				MT_BRK0	SPI_MOSI	USR_CTS	I2C_SDA						SCTM2		
19	PA8				GT_CH0		USR_RX									
20	PA9_BOOT				GT_CH3		USR_TX									CKOUT
21	PA10				GT_CH1		USR_RTS	I2C_SCL						SCTM1		
22	PA11				GT_CH2		USR_CTS	I2C_SDA						SCTM2		
23	SWCLK	PA12														
24	SWDIO	PA13														
25	GLC															
26	GHC															
27	SHC															
28	BSTC															
29	GLB															
30	GHB															
31	SHB															
32	BSTB															
33	GLA															
34	GHA															
35	SHA															
36	BSTA															
37	LSS															
38	V12P															
39	VCC															
40	VREG															
41	PB5					SPI_SEL			OPA0O							
42	PC1					SPI_ SCK			OPA0N					SCTM0		
43	PC2		ADC0_IN0			SPI_MOSI			OPA0P					SCTM1		
44	PC3		ADC0_IN1			SPI_MISO			OPA1O							
45	PB6		ADC0_IN2		MT_BRK0			I2C_SCL	OPA1N					SCTM2		
46	PB7		ADC0_IN3		MT_BRK1			I2C_SDA	OPA1P							
47	VDDA															
48	VSSA															

Table 6. Pin Description

Pin Number 48LQFP-EP	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description Default function (AF0)
1	PA0	AI/O	5V	4/8/12/16 mA	PA0
2	PA1	AI/O	5V	4/8/12/16 mA	PA1
3	PA2	AI/O	5V	4/8/12/16 mA	PA2
4	PA3	AI/O	5V	4/8/12/16 mA	PA3
5	PA4	AI/O	5V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode
6	PA5	AI/O	5V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode
7	PA6	AI/O	5V	4/8/12/16 mA	PA6
8	PA7	AI/O	5V	4/8/12/16 mA	PA7
9	PC4	AI/O	5V	4/8/12/16 mA	PC4
10	PC6	AI/O	5V	4/8/12/16 mA	PC6
11	CLDO	P	—	—	Core power LDO V_{CORE} output A 2.2μF capacitor must be connected as close as possible between this pin and VSS
12	VDD	P	—	—	Digital voltage input
13	VSS	P	—	—	Ground reference
14	nRST(3)	I	5V_PU	—	External reset pin
15	PB9(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
16	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
17	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
18	PB15	I/O	5V	4/8/12/16 mA	PB15
19	PA8	I/O	5V	4/8/12/16 mA	PA8
20	PA9	I/O	5V_PU	4/8/12/16 mA	PA9_BOOT
21	PA10	I/O	5V	4/8/12/16 mA	PA10
22	PA11	I/O	5V	4/8/12/16 mA	PA11
23	PA12	I/O	5V_PU	4/8/12/16 mA	SWCLK
24	PA13	I/O	5V_PU	4/8/12/16 mA	SWDIO
25	GLC	O	—	—	Low-side gate drive phase C
26	GHC	O	—	—	High-side gate drive phase C
27	SHC	I	—	—	High-side source connection phase C
28	BSTC	O	—	—	Bootstrap output phase C
29	GLB	O	—	—	Low-side gate drive phase B
30	GHB	O	—	—	High-side gate drive phase B
31	SHB	I	—	—	High-side source connection phase B
32	BSTB	O	—	—	Bootstrap output phase B
33	GLA	O	—	—	Low-side gate drive phase A
34	GHA	O	—	—	High-side gate drive phase A
35	SHA	I	—	—	High-side source connection phase A
36	BSTA	O	—	—	Bootstrap output phase A
37	LSS	I	—	—	Low-side source connection for phase A, B and C. Connect to ground of power stage.

Pin Number 48LQFP-EP	Pin Name	Type[(1)]	I/O Structure[(2)]	Output Driving	Description Default function (AF0)
38	V12P	O	—	—	Supplied from VCC. Regulated 12 V output (V12P only supplies power to the device internal circuit)
39	VCC	P	—	—	VCC power supply input
40	VREG	O	—	—	Supplied from VCC. Regulated 5 V output. Always active
41	PB5	AI/O	5V	4/8/12/16 mA	PB5
42	PC1	AI/O	5V	4/8/12/16 mA	PC1
43	PC2	AI/O	5V	4/8/12/16 mA	PC2
44	PC3	AI/O	5V	4/8/12/16 mA	PC3
45	PB6	AI/O	5V	4/8/12/16 mA	PB6
46	PB7	AI/O	5V	4/8/12/16 mA	PB7
47	VDDA	P	—	—	Analog voltage for ADC and Comparator
48	VSSA	P	—	—	Ground reference for ADC and Comparator

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. The EP which means the thermally enhanced Exposed Pad on the packages must be connected to ground.

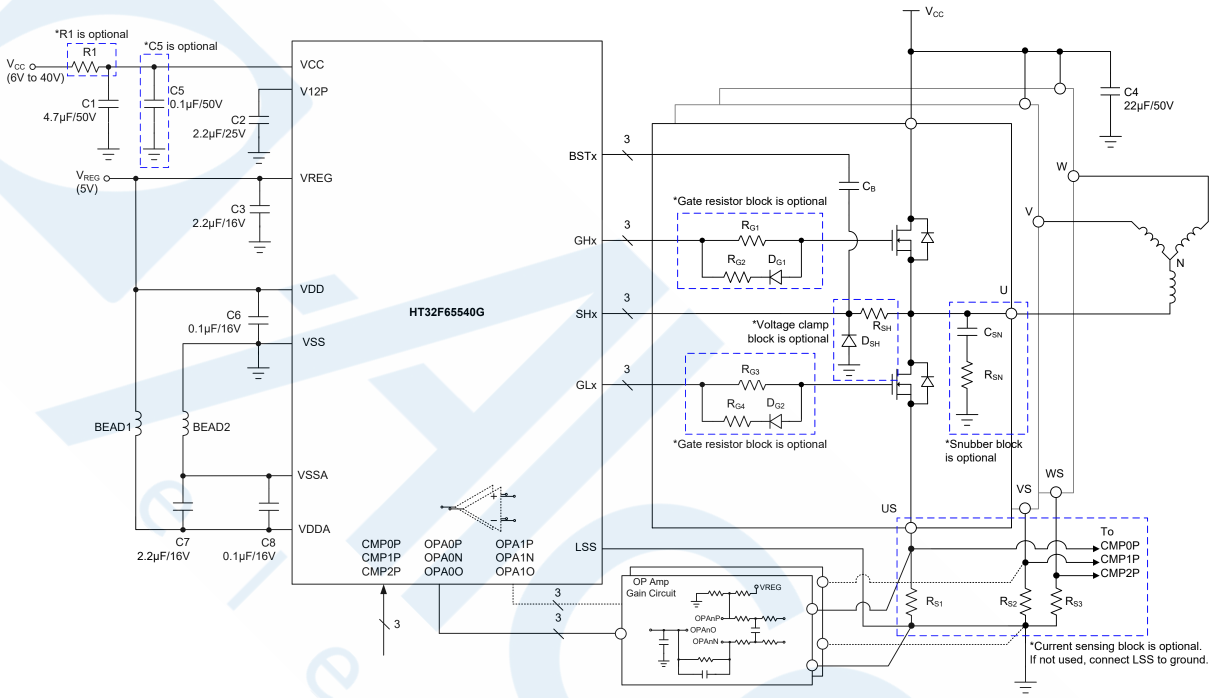
Internal Connection Signal Lines

The MCU generated signals such as the MCTM channel outputs have been internally connected to the gate-driver inputs for control purpose. The connections are listed in the following table and the related control registers should be configured correctly using application program.

Table 7. Internal Connection Signal Lines

MCU Signal Name	Connected Gate-Driver Signal Name	Description
PC9 / MT_CH0 (MCTM)	INHA	Control input for high-side gate drive phase A, high active. The MCU AFIO setting should be AF4 to select the MCTM pin function.
PC8 / MT_CH0N (MCTM)	$\overline{\text{INLA}}$	Control input for low-side gate drive phase A, low active. The MCU AFIO setting should be AF4 to select the MCTM pin function.
PB1/ MT_CH1 (MCTM)	INHB	Control input for high-side gate drive phase B, high active. The MCU AFIO setting should be AF4 to select the MCTM pin function.
PB0 / MT_CH1N (MCTM)	$\overline{\text{INLB}}$	Control input for low-side gate drive phase B, low active. The MCU AFIO setting should be AF4 to select the MCTM pin function.
PA15 / MT_CH2 (MCTM)	INHC	Control input for high-side gate drive phase C, high active. The MCU AFIO setting should be AF4 to select the MCTM pin function.
PA14 / MT_CH2N (MCTM)	$\overline{\text{INLC}}$	Control input for low-side gate drive phase C, low active. The MCU AFIO setting should be AF4 to select the MCTM pin function.

6 Application Circuits



Note: 1. V12P only supplies power to the device internal circuit.

2. When verification, the load can use a 5Ω resistor in series with a 1mH inductor.

Figure 10. Typical Application Circuit – 2-Shunt Current Sensing

7 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Parameter		Value	Unit
V_{CC}		6 to 48	V
V_{DD}, V_{DDA}		(V_{SS} - 0.3) to (V_{SS} + 5.5)	V
SHx		-2 (<1μs) to 48	V
BSTx, GHx		-0.3 to 60	V
$V_{(GHx, SHx)}$, $V_{(BSTx, SHx)}$		-0.3 to 20	V
V12P, GLx		-0.3 to 20	V
VREG, INHx, $\overline{\text{INLx}}$		-0.3 to 7.0	V
Ambient Operating Temperature Range		-40 to 105	°C
Storage Temperature Range		-60 to 150	°C
Maximum Junction Temperature		125	°C
Electrostatic Discharge Voltage	Human Body Model	±4000	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	48LQFP-EP	50	°C/W

Recommended DC Operating Conditions

Table 9. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	—	6	—	40	V
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
V_{DDA}	Analog Operating Voltage	—	2.5	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 10. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 35 mA and voltage variation = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 11. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	16.76	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	7.54	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	13.9	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	7.69	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	6.56	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	3.44	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	2.69	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	1.43	—	mA
		V_{DD} = 5.0 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals enabled	—	34.6	—	μA
		V_{DD} = 5.0 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals disabled	—	29.6	—	μA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Sleep Mode)	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	11.22	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	1.19	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	7.63	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	0.94	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	4.16	—	mA
I_{DD}	Supply Current (Sleep Mode)	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	0.73	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	1.72	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	0.35	—	mA
	Supply Current (Deep-Sleep Mode)	V_{DD} = 5.0 V, all clock off (HSE/HSI), LDO in low power mode, LSI on, LSTM on	—	25	—	µA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSI means 32 kHz low speed internal oscillator.
3. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 12. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 105 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})		2.09	2.2	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 13. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown-Out Detection	After factory-trimmed V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	—	—	ms
I_{DDLVD}	Operation Current [3]	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 14. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	2.5	—	5.5	V
f_{HSE}	HSE Frequency	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	—	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	160	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 15. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 105 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5.0 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 5.0 V, T_A = 25 °C	-2	—	+2	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -20 °C ~ 85 °C	-3	—	+3	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = 85 °C ~ 105 °C	-3.5	—	+3.5	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ -20 °C	-5	—	+3.5	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	μA
	Power Down Current		—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 8 MHz	—	—	10	μs

Table 16. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	2.5	—	5.5	V
f_{LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 105 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 5.0 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V, T_A = 25 °C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V, T_A = 25 °C	—	—	100	μs

System PLL Characteristics

Table 17. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 18. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 105 °C	10	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 105 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 105 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 105 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 105 °C	10	—	—	ms

I/O Port Characteristics

Table 19. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O; $V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin; $V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	
I_{IH}	High Level Input Current	5.0 V I/O; $V_I = V_{DD,}$ On-chip pull-down resister disabled	—	—	3	μA
		Reset pin; $V_I = V_{DD,}$ On-chip pull-down resister disabled	—	—	3	
V_{IL}	Low Level Input Voltage	5.0 V I/O	-0.5	—	V_{DD} × 0.35	V
		Reset pin	-0.5	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	5.0 V I/O	V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin	V_{DD} × 0.65	—	V_{DD} + 0.5	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O	—	0.12 × V_{DD}	—	mV
		Reset pin	—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.4 V	4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.4 V	8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.4 V	12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.4 V	16	—	—	mA
		V_{DD} Domain I/O drive @ V_{DD} = 5.0 V, V_{OL} = 0.4 V, PB9	4	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	4	—	—	mA
		5.0 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	8	—	—	mA
		5.0 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	12	—	—	mA
		5.0 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	16	—	—	mA
		V_{DD} Domain I/O drive @ V_{DD} = 5.0 V, $V_{OH} = V_{DD}$ - 0.4 V, PB9	—	—	2	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA	—	—	0.4	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA	—	—	0.4	
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA	—	—	0.4	
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA	—	—	0.4	
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA	V_{DD} - 0.4	—	—	
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	5.0 V I/O, V_{DD} = 5.0 V	—	60	—	kΩ
R_{PD}	Internal Pull-down Resistor	5.0 V I/O, V_{DD} = 5.0 V	—	60	—	kΩ

ADC Characteristics

Table 20. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	A/D Converter Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 5.0 V	—	0.85	1	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	µA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	MHz
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Time	—	—	—	1	µs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±2	±5	LSB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DNL	Differential Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, 3.5/f_{ADC}. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

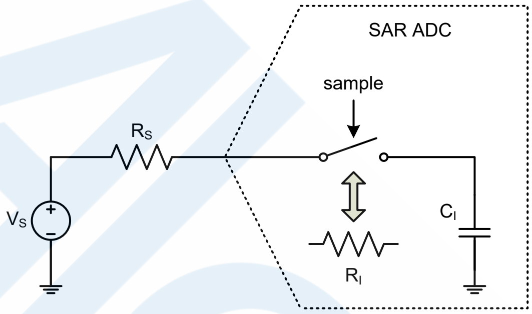


Figure 11. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Comparator Characteristics

Table 21. Comparator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating Voltage	Comparator mode	2.5	5.0	5.5	V
V_{IN}	Input Common Mode Voltage Range	CP or CN	V_{SSA}	—	V_{DDA}	V
V_{IOS}	Input Offset Voltage[1]	T_A = 25 °C	-15	—	15	mV
V_{HYS}	Input Hysteresis V_{DDA} = 5.0 V	No hysteresis, CMPHM [1:0] = 00	—	0	—	mV
V_{HYS}	Input Hysteresis V_{DDA} = 5.0 V	Low hysteresis, CMPHM [1:0] = 01	—	50	—	mV
V_{HYS}	Input Hysteresis V_{DDA} = 5.0 V	Middle hysteresis, CMPHM [1:0] = 10	—	100	—	mV
V_{HYS}	Input Hysteresis V_{DDA} = 5.0 V	High hysteresis, CMPHM [1:0] = 11	—	150	—	mV
t_{RT}	Response Time Input Overdrive = ±100 mV	High Speed Mode, $V_{DDA} \ge 3.6$ V	—	50	100	ns
t_{RT}	Response Time Input Overdrive = ±100 mV	High Speed Mode, $V_{DDA} < 3.6$ V	—	100	250	ns
t_{RT}	Response Time Input Overdrive = ±100 mV	Low Speed Mode	—	2	5	μs
I_{CMP}	Current Consumption V_{DDA} = 5.0 V	High Speed Mode	—	180	—	μA
I_{CMP}	Current Consumption V_{DDA} = 5.0 V	Low Speed Mode	—	50	—	μA
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid	—	—	50	μs
I_{CMP_DN}	Power Down Supply Current	CMPEN = 0 CVREN = 0 CVROE = 0	—	—	0.1	μA
Comparator Voltage Reference (CVR)						
V_{CVR}	Output Range	—	V_{SSA}	—	V_{DDA}	V
N_{Bits}	CVR Scaler Resolution	—	—	6	—	bits
t_{CVRST}	Settling Time	CVR Scaler Setting Time from CVRVAL[5:0] = “000000” to “111111”	—	—	100	μs
I_{CVR}	Current Consumption V_{DDA} = 5.0 V	CVREN = 1, CVROE = 0	—	100	—	μA
I_{CVR}	Current Consumption V_{DDA} = 5.0 V	CVREN = 1, CVROE = 1	—	125	150	μA

Note: Data based on characterization results only, not tested in production.

Operational Amplifier Characteristics

Table 22. Operational Amplifier Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	OPA mode	2.5	5.0	5.5	V
I_{OPA_DN}	Power Down Current	—	—	—	0.1	μA
V_{OPOS}	Input Offset Voltage	Without calibration	-15	—	15	mV
V_{CM}	Common Mode Voltage Range	—	V_{SS}+0.2	—	V_{DD}-0.2	V
V_{OR}	Maximum output voltage range	—	V_{SS}+0.2	—	V_{DD}-0.2	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Current Dissipation	—	—	800	—	μA
PSRR	Power Supply Rejection Ratio	—	—	80	—	dB
CMRR	Common Mode Rejection Ratio	V_{CM} = 0 ~ V_{DD}	—	80	—	dB
SR	Slew Rate+, Slew Rate-	R_L = 100 kΩ, C_L = 100 pF	6	—	—	V/μs
GBW	Gain Band Width	R_L = 100 kΩ, C_L = 100 pF	—	6	—	MHz
A_{OL}	Open Loop Gain	R_L = 100 kΩ, C_L = 100 pF	60	80	—	dB
PM	Phase Margin	R_L = 100 kΩ, C_L = 100 pF	50	60	—	

MCTM/GPTM/SCTM Characteristics

Table 23. MCTM/GPTM/SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for MCTM, GPTM and SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

Gate-Driver Characteristics

Table 24. Gate-Driver Characteristics

V_{CC} = 24 V, C1 = 4.7 μF, C2 = 2.2 μF, C3 = 2.2 μF, C4 = 22 μF,
C_B = 2.2 μF and T_A = 25˚C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply / Regulators						
V_{CC}	Supply Voltage	—	6	—	40	V
I_{CC}	Supply Standby Current	I_{LOAD} = 0 mA (SHx = GND)	—	300	400	μA
V_{REG}	VREG Output Voltage	I_{LOAD} = 1 mA	4.925	5.0	5.075	V
I_{LOAD} (1)	VREG Output Current	V_{CC} = 6 V ~ 40 V (without thermal limited)	50	—	—	mA
ΔV_{REG}	VREG Load Regulation	I_{LOAD} = 0 mA ~ 30 mA	—	15	—	mV
$\frac{\Delta V_{REG}}{\Delta V_{CC} \times V_{REG}}$	VREG Linear Regulation	V_{CC} rises from 6 V to 40 V	—	0.1	0.2	%/V
$\frac{\Delta V_{REG}}{\Delta T_A \times V_{REG}}$	VREG Temperature Coefficient	I_{LOAD} = 1 mA, T_A = -40 ˚C ~ 105 ˚C	—	±100	—	ppm/˚C
PSRR	VREG Power Supply Rejection Ratio	I_{LOAD} = 30 mA	—	60	—	dB
Noise	VREG Output Noise	I_{LOAD} = 30 mA, BW = 10 kHz ~ 100 kHz	—	50	—	μV_{RMS}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Bootstrap						
I_{BST}	Current Consumption from BST	INHx = '1' and $\overline{INLx}$ = '1'	—	80	100	μA
I_{BSTC}	Bootstrap Charging Current	INHx = '0' and $\overline{INLx}$ = '1' (SHx = GND)	—	25	—	mA
Gate-Driver (GHx, SHx, GLx)						
V_{GSH}	High-Side V_{GS} Gate Drive – $V_{(GHx,SHx)}$	V_{CC} = 6 V ~ 13 V, f_{PWM} = 25 kHz	V_{CC}-2	V_{CC}-1.5	—	V
		V_{CC} = 13 V ~ 40 V, f_{PWM} = 25 kHz	11	12	13	V
V_{GSL}	Low-Side V_{GS} Gate Drive – $V_{(GLx,LSS)}$	V_{CC} = 6 V ~ 13 V	V_{CC}-1	V_{CC}-0.5	—	V
		V_{CC} = 13 V ~ 40 V	11	12	—	V
I_{DRVP}	High-Side and Low-Side Gate Peak Source Current	R_{DRV} = open, C_{GS} = 200 nF	—	700	—	mA
I_{DRVN}	High-Side and Low-Side Gate Peak Sink Current	R_{DRV} = open, C_{GS} = 200 nF	—	1000	—	mA
t_{DEAD}	Dead Time	—	—	120	200	ns
t_{DEAD_MIS}	Dead Time Mismatch	Dead time difference between rising and falling edges	—	50	—	ns
t_{PD}	Propagation Delay	INHx to GHx and $\overline{INLx}$ to GLx transition (No connected capacitor with GHx / GLx)	—	40	200	ns
t_{PD_MIS}	High-Side / Low-Side Propagation Delay Mismatch	Propagation delay difference between different phases or different sides	—	20	—	ns
t_{ON_MIN}	Minimum Input Pulse Width(2)	—	—	—	150	ns
R_{OFF1}	Low-Side Gate Hold-off Resistor	GLx to LSS	—	200	—	kΩ
R_{OFF2}	High-Side Gate Hold-off Resistor	GHx to SHx	—	400	—	kΩ
Protections						
V_{CC_UVLO+}	V_{CC} Turn On Level	V_{CC} rises	—	5.5	6	V
V_{CC_UVLO-}	V_{CC} Turn Off Level	V_{CC} falls	4.5	5.0	—	V
V_{REG_UVLO+}	V_{REG} Turn On Level	V_{REG} rises	—	—	4.0	V
V_{REG_UVLO-}	V_{REG} Turn Off Level	V_{REG} falls	3.0	—	—	V
V_{12P_UVLO+}	V_{12P} Turn On Level	V_{12P} rises, $\overline{INLx}$ = '0'	—	5.5	6	V
V_{12P_UVLO-}	V_{12P} Turn Off Level	V_{12P} falls, $\overline{INLx}$ = '0'	4.2	5.0	—	V
V_{BST_UVLO+}	$V_{(BSTx,SHx)}$ Turn On Level	$V_{(BSTx,SHx)}$ rises, INHx = '1'	—	3.7	4.2	V
V_{BST_UVLO-}	$V_{(BSTx,SHx)}$ Turn Off Level	$V_{(BSTx,SHx)}$ falls, INHx = '1'	2.2	2.6	—	V
T_{SHD}	Thermal Shutdown Threshold	—	—	160	—	°C
T_{REC}	Thermal Recovery Threshold	—	—	120	—	°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Control Logic						
V_{IL}	Input Logic Low Voltage	INHx, $\overline{INLx}$	—	—	0.8	V
V_{IH}	Input Logic High Voltage	INHx, $\overline{INLx}$	2.0	—	—	V
R_{PD}	Input Logic Pull-down Resistor	INHx	—	100	—	kΩ
R_{PU}	Input Logic Pull-up Resistor	$\overline{INLx}$	—	100	—	kΩ

Note: 1. Output current standard: the output voltage might keep a 2% voltage drop compared to the original output voltage for a 1mA load current.
2. When the INHx or $\overline{INLx}$ input signal pulse width is less than t_{ON_MIN}, the output may malfunction.

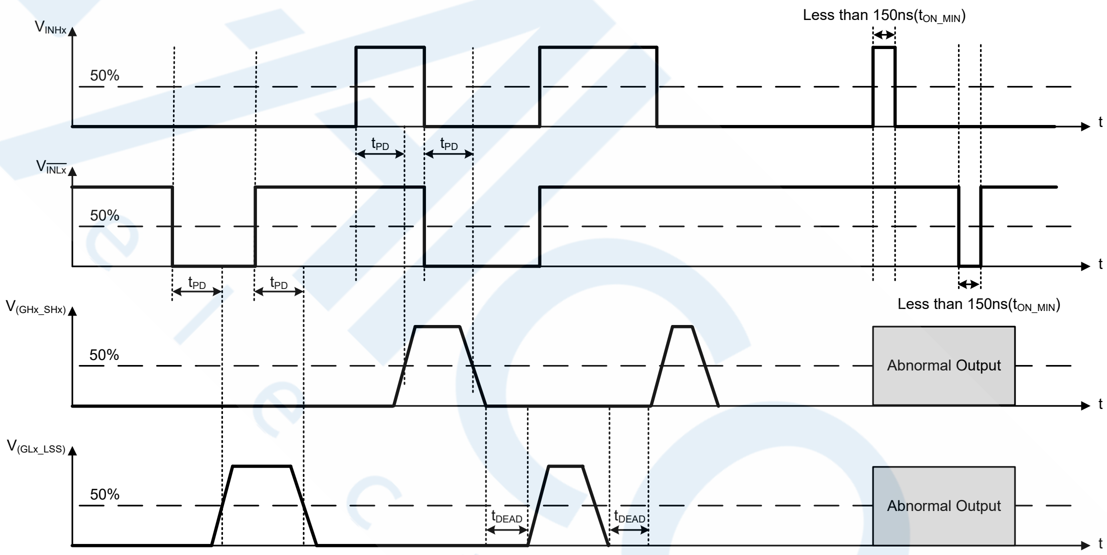


Figure 12. Gate Drive Timing Diagram

I²C Characteristics

Table 25. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time	0	—	0	—	0	—	ns
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: SEQFILTER = 01 and COMBFILTEREN = 0 that COMB_filter is disabled.

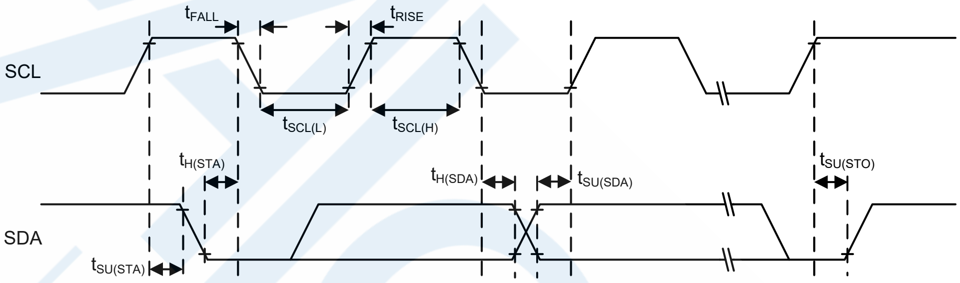


Figure 13. I²C Timing Diagram

SPI Characteristics

Table 26. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

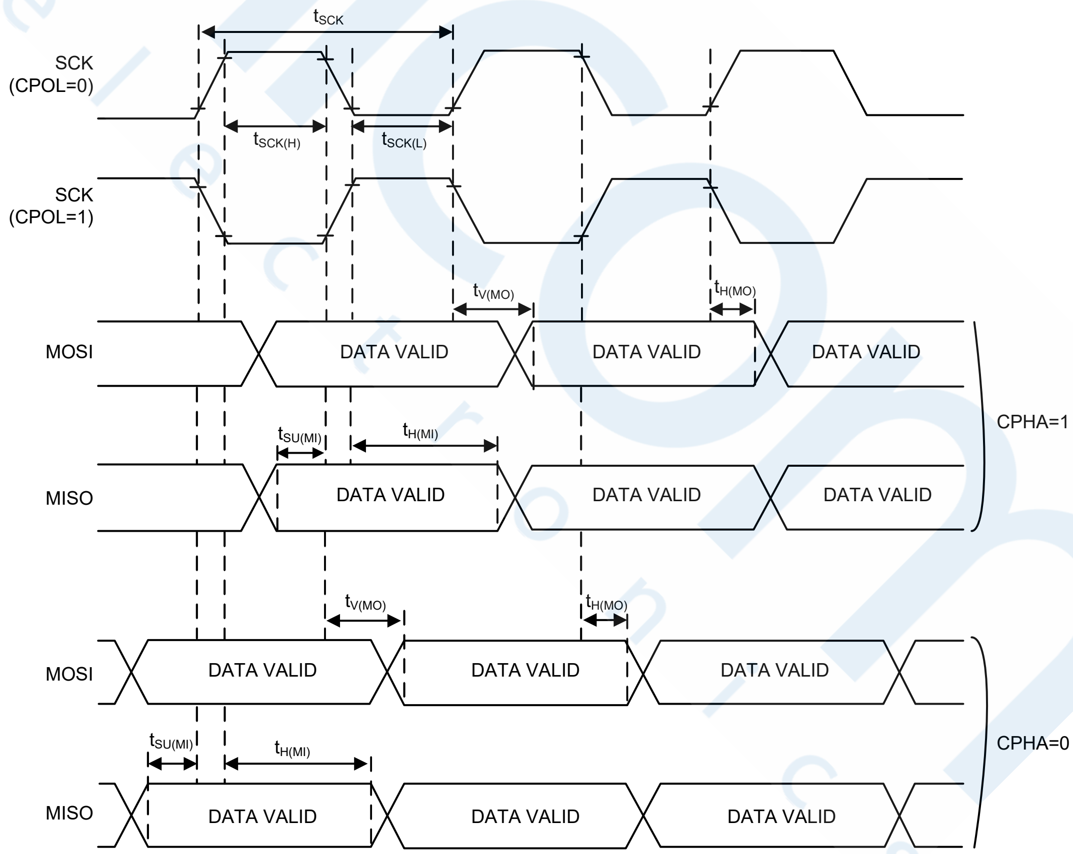


Figure 14. SPI Timing Diagram – SPI Master Mode

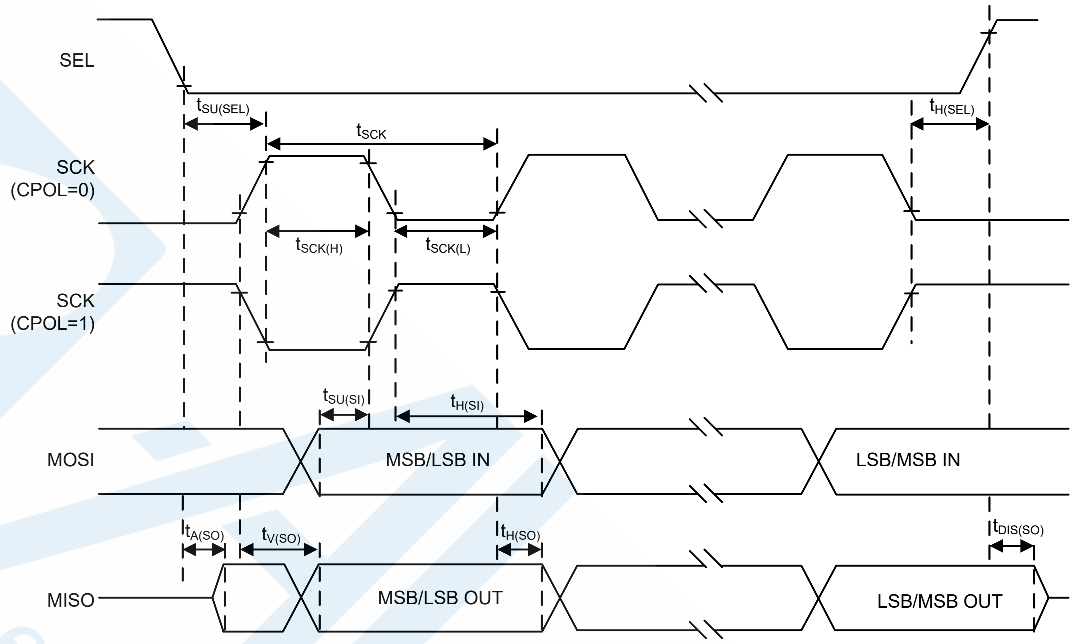


Figure 15. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

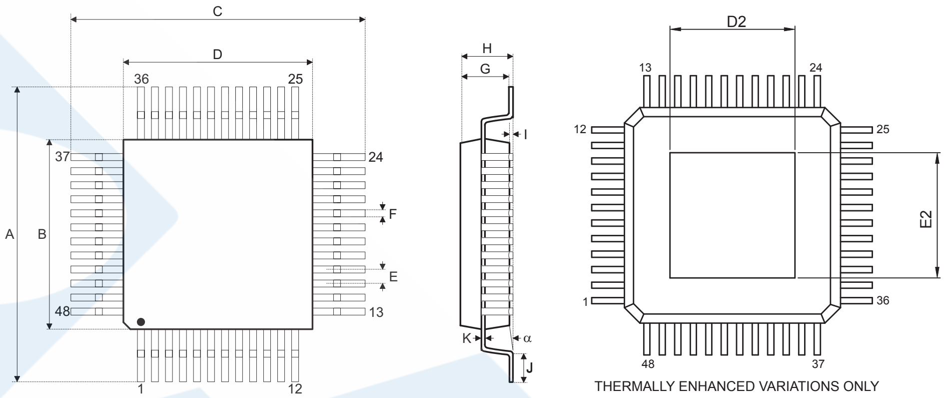
8 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

48-pin LQFP-EP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
D2	0.079	—	—
E	—	0.020 BSC	—
E2	0.079	—	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
D2	2.00	—	—
E	—	0.50 BSC	—
E2	2.00	—	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°