

## Features

- Highly integrated analog circuits for demodulation and decoding
- Operating voltage range: 2.3V~5.5V
- Ultra low power consumption, typical communication distance up to 10cm depending on antenna size
- Supports ISO/IEC 14443 TypeA/TypeB protocols
- Supports ISO 14443 A, B high transfer speed of 106kbit/s, 212kbit/s, 424kbit/s and 848kbit/s
- Supports MFIN/MFOUT
- Supported host interfaces
  - ♦ SPI interface up to 10Mbit/s
  - ♦ I<sup>2</sup>C interface up to 400kbit/s
  - ♦ Serial UART up to 1228.8kbit/s
- FIFO buffer for 64-byte transmission and reception
- Flexible interrupt modes
- Programmable timer
- 3 power saving modes: hardware power-down, software power-down and transmitter power-down
- Internal temperature sensor automatically stops RF transmission in high chip temperature situations
- Multiple independent power supplies to avoid mutual interference between blocks and improve the operation stability
- CRC coprocessor to implement CRC and parity function
- Internal oscillator for connection to a 27.12MHz quartz crystal
- Programmable I/O pins
- Supports Low Power Card Detection (LPCD) function
- Package type: 32-pin QFN

## Applications

- Security access control / locks
- Toys
- Handheld NFC readers
- Contactless payment systems

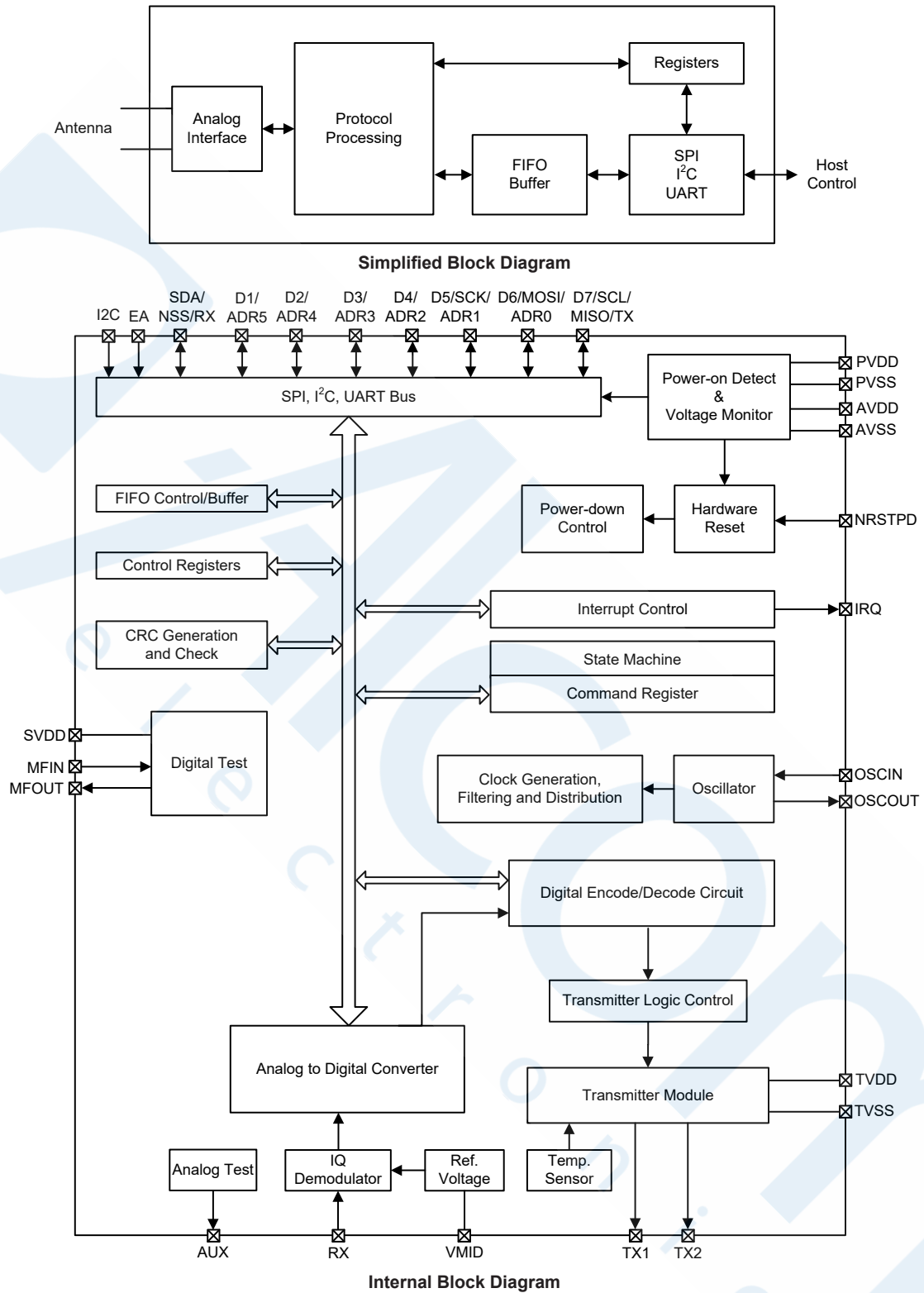
## General Description

The BC45B4522 is a highly integrated reader IC for use in contactless communication at 13.56MHz. This NFC reader supports ISO/IEC 14443 A, ISO/IEC 14443B and Crypto\_M modes. The internal transmitter is able to drive the reader antenna to communicate with ISO/IEC 14443 A, ISO/IEC1444B, Crypto\_M cards and transponders without requiring additional active circuitry. The receiver block provides a robust and efficient implementation to demodulate and decode signals from ISO/IEC 14443 A, ISO/IEC1444B, Crypto\_M cards and transponders. The digital block manages the complete ISO/IEC 14443 A framing detection and error detection including parity and CRC check.

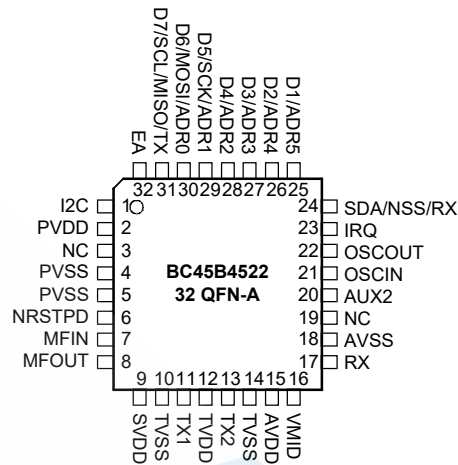
The BC45B4522 supports all protocol layers for ISO/IEC 14443 A and ISO/IEC 14443 B communications. It supports contactless communication with higher baud rates and the bidirectional transmission speeds is up to 848kbit/s. The device provides several host interfaces including the Serial Peripheral Interface(SPI), serial UART and I<sup>2</sup>C bus.

## Block Diagram

The analog interface is used to handle the modulation and demodulation of analog signals, and then cooperate with the host to manage the communication protocol requirements. The FIFO buffer ensures fast and convenient data transfer between the host and the contactless interface. Various host interfaces are provided to meet different customer requirements.



## Pin Assignment



## Pin Description

| Pin No. | Pin Name     | Pin Type | Description  |
|---------|--------------|----------|--|
| 1       | I2C          | I        | I <sup>2</sup> C interface enable                          |
| 2       | PVDD         | PWR      | Pin and digital positive power supply                      |
| 3       | NC           | —        | Not connected  |
| 4       | PVSS         | G        | Pin and digital negative power supply, ground              |
| 5       | PVSS         | G        | Pin and digital negative power supply, ground              |
| 6       | NRSTPD       | I        | Reset or power-down pin, low active                        |
| 7       | MFIN         | I        | Test signal input  |
| 8       | MFOUT        | O        | Test signal output   |
| 9       | SVDD         | PWR      | MFIN and MFOUT positive power supply                       |
| 10      | TVSS         | G        | Transmitter negative power supply, ground                  |
| 11      | TX1          | O        | Transmitter antenna pin 1                                  |
| 12      | TVDD         | PWR      | Transmitter positive power supply                          |
| 13      | TX2          | O        | Transmitter antenna pin 2                                  |
| 14      | TVSS         | G        | Transmitter negative power supply, ground                  |
| 15      | AVDD         | PWR      | Analog positive power supply                               |
| 16      | VMID         | PWR      | Internal reference voltage                                 |
| 17      | RX           | I        | Receiver antenna pin                                       |
| 18      | AVSS         | G        | Analog negative power supply, ground                       |
| 19      | NC           | —        | Not connected  |
| 20      | AUX2         | O        | Test pin   |
| 21      | OSCIN        | I        | 27.12MHz crystal input                                     |
| 22      | OSCOUT       | O        | 27.12MHz crystal output                                    |
| 23      | IRQ          | O        | Interrupt request output                                   |
| 24      | SDA/NSS/RX   | I/O      | I <sup>2</sup> C SDA; SPI NSS; UART RX                     |
| 25      | D1/ADR5      | I/O      | Programmable I/O; I <sup>2</sup> C address bit 5           |
| 26      | D2/ADR4      | I/O      | Programmable I/O; I <sup>2</sup> C address bit 4           |
| 27      | D3/ADR3      | I/O      | Programmable I/O; I <sup>2</sup> C address bit 3           |
| 28      | D4/ADR2      | I/O      | Programmable I/O; I <sup>2</sup> C address bit 2           |
| 29      | D5/SCK/ADR1  | I/O      | Programmable I/O; SPI SCK; I <sup>2</sup> C address bit 1  |
| 30      | D6/MOSI/ADR0 | I/O      | Programmable I/O; SPI MOSI; I <sup>2</sup> C address bit 0 |

| Pin No. | Pin Name       | Pin Type | Description   |
|---------|----------------|----------|---|
| 31      | D7/SCL/MISO/TX | I/O      | Programmable I/O; I <sup>2</sup> C SCL; SPI MISO; UART TX |
| 32      | EA             | I        | I <sup>2</sup> C address coding control                   |

Legend: 1. Pin Type: I=Input, O=Output, I/O=Input/Output, PWR=Power, G=Ground

2. MFIN and MFOUT are digital test pins. Leave the pins floating in product design.

## Electrical Characteristics

### Absolute Maximum Rating

| Symbol           | Parameter           | Conditions | Min. | Max. | Unit |
|------------------|---------------------|------------|------|------|------|
| AV <sub>DD</sub> | Analog Power Supply | —          | -0.5 | +6.0 | V    |
| PV <sub>DD</sub> | PVDD Power Supply   | —          | -0.5 | +6.0 | V    |
| TV <sub>DD</sub> | TVDD Power Supply   | —          | -0.5 | +6.0 | V    |
| SV <sub>DD</sub> | SVDD Power Supply   | —          | -0.5 | +6.0 | V    |

### Operating Condition

| Symbol           | Parameter                       | Conditions  | Min. | Typ. | Max. | Unit |
|------------------|---------------------------------|---|------|------|------|------|
| AV <sub>DD</sub> | Analog Power Supply             | PV <sub>SS</sub> =AV <sub>SS</sub> =TV <sub>SS</sub> =0V,<br>PV <sub>DD</sub> ≤SV <sub>DD</sub> ≤AV <sub>DD</sub> ≤TV <sub>DD</sub> | 2.3  | 3.3  | 5.5  | V    |
| TV <sub>DD</sub> | Transmitter Power Supply        |   | 2.3  | 3.3  | 5.5  | V    |
| SV <sub>DD</sub> | MFIN and MFOUT Pin Power Supply |   | 2.3  | 3.3  | 5.5  | V    |
| PV <sub>DD</sub> | Pin and Digital Power Supply    |   | 2.0  | 3.3  | 5.5  | V    |
| T <sub>a</sub>   | Operating Temperature           | —   | -40  | —    | +105 | °C   |

Note: Recommended power supply condition: PV<sub>DD</sub>≤SV<sub>DD</sub>≤AV<sub>DD</sub>≤TV<sub>DD</sub>. The performance of other power supply conditions are not guaranteed.

### Power Consumption Characteristics

| Symbol                      | Parameter                           | Conditions   | Min. | Typ. | Max. | Unit |
|-----------------------------|-------------------------------------|--|------|------|------|------|
| <b>3.3V Characteristics</b> |                                     |  |      |      |      |      |
| I <sub>HPD</sub>            | Hardware Power-down Current         | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =3.3V,<br>NRSTPD=LOW  | —    | 0.02 | 1.00 | μA   |
| I <sub>SPD</sub>            | Software Power-down Current         | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =3.3V,<br>RF level detector on  | —    | 0.6  | 5.0  | μA   |
| I <sub>IDLE</sub>           | Idle Current                        | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =3.3V   | —    | 3.52 | 5.00 | mA   |
| I <sub>RX</sub>             | Receiving Current                   | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =3.3V   | —    | 6.5  | 10.0 | mA   |
| I <sub>PVDD</sub>           | Pin and Digital Supply Current      | PV <sub>DD</sub> =3.3V   | —    | 2.97 | 4.00 | mA   |
| I <sub>AVDD</sub>           | Analog Supply Current               | AV <sub>DD</sub> =3.3V, RcvOff=0   | —    | 2.98 | 6.00 | mA   |
|                             |                                     | AV <sub>DD</sub> =3.3V, RcvOff=1   | —    | 2.95 | 6.00 | mA   |
| I <sub>TVDD</sub>           | Transmitter Supply Current          | Continuous transmit carrier,<br>TV <sub>DD</sub> =3.3V   | —    | 60   | 160  | mA   |
| I <sub>LPD</sub>            | Low Power Card Detection Current    | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =3.3V,<br>Average current consumption in<br>LPD mode @ WUPeriod=500ms<br>& detect wave time=5.9μs | —    | 1.5  | 10.0 | μA   |
| V <sub>Ripple</sub>         | Power Supply Ripple Rejection       | —  | —    | —    | 400  | mV   |
| V <sub>Noise</sub>          | Power Supply Random Noise Rejection | —  | —    | —    | 1600 | mV   |
| T <sub>OSU</sub>            | Oscillator Start Up Time            | —  | —    | 300  | —    | μs   |

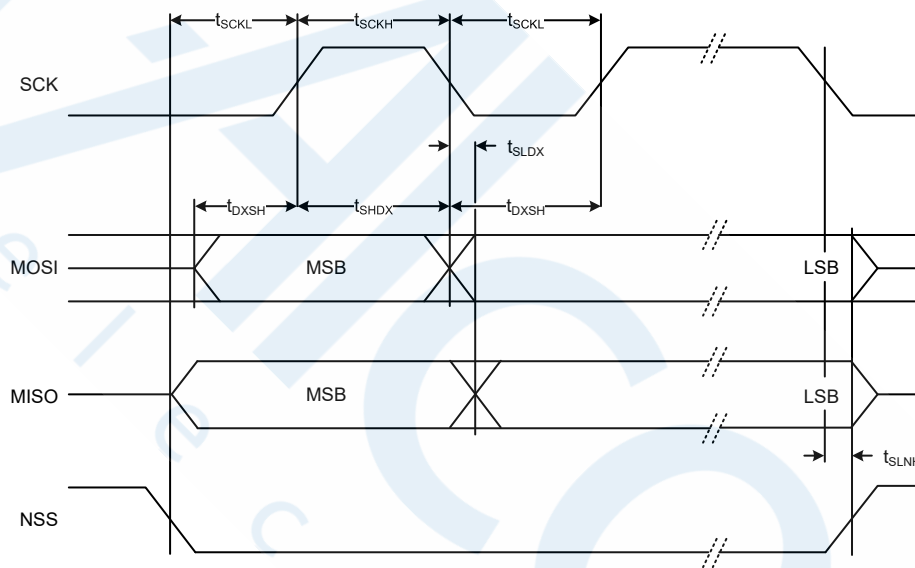
| Symbol                    | Parameter                           | Conditions  | Min. | Typ. | Max.  | Unit |
|---------------------------|-------------------------------------|---|------|------|-------|------|
| <b>5V Characteristics</b> |                                     |   |      |      |       |      |
| I <sub>HPD</sub>          | Hardware Power-down Current         | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =5V,<br>NRSTPD=LOW           | —    | 0.02 | 1.00  | μA   |
| I <sub>SPD</sub>          | Software Power-down Current         | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =5V,<br>RF level detector on | —    | 0.8  | 5.0   | μA   |
| I <sub>IDLE</sub>         | Idle Current                        | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =5V                          | —    | 3.52 | 5.00  | mA   |
| I <sub>RX</sub>           | Receiving Current                   | AV <sub>DD</sub> =TV <sub>DD</sub> =PV <sub>DD</sub> =SV <sub>DD</sub> =5V                          | —    | 6.55 | 10.00 | mA   |
| I <sub>PVDD</sub>         | Pin and Digital Supply Current      | PV <sub>DD</sub> =5V  | —    | 3.2  | 5.0   | mA   |
| I <sub>AVDD</sub>         | Analog Supply Current               | AV <sub>DD</sub> =5V, RcvOff=0  | —    | 3.1  | 6.0   | mA   |
|                           |                                     | AV <sub>DD</sub> =5V, RcvOff=1  | —    | 3.07 | 6.00  | mA   |
| I <sub>TVDD</sub>         | Transmitter Supply Current          | Continuous transmit carrier,<br>TV <sub>DD</sub> =5V  | —    | 90   | 230   | mA   |
| V <sub>Ripple</sub>       | Power Supply Ripple Rejection       | —   | —    | —    | 300   | mV   |
| V <sub>Noise</sub>        | Power Supply Random Noise Rejection | —   | —    | —    | 1600  | mV   |
| T <sub>OSU</sub>          | Oscillator Start Up Time            | —   | —    | 300  | —     | μs   |

**I/O Characteristics**

| Symbol  | Parameter                    | Conditions                                     | Min.                  | Typ.  | Max.                  | Unit |
|---|------------------------------|--|-----------------------|-------|-----------------------|------|
| <b>Pins I2C, EA, NRSTPD, MFIN, SDA/NSS/RX</b>   |                              |  |                       |       |                       |      |
| I <sub>LEAK</sub>   | Input Leakage Current        | —  | -1                    | —     | 1                     | μA   |
| V <sub>IH</sub>   | High Level Input Voltage     | —  | 0.7PV <sub>DD</sub>   | —     | —                     | V    |
| V <sub>IL</sub>   | Low Level Input Voltage      | —  | —                     | —     | 0.3PV <sub>DD</sub>   | V    |
| <b>Pins D1/ADR5, D2/ADR4, D3/ADR3, D4/ADR2, D5/SCK/ADR1, D6/MOSI/ADR0, D7/SCL/MISO/TX, MFOUT, IRQ</b> |                              |  |                       |       |                       |      |
| I <sub>LEAK</sub>   | Input Leakage Current        | Connected to VDD when in operation/idle state  | -1                    | —     | 1                     | μA   |
|   |                              | Connected to GND when in operation/idle state  | —                     | 13.5  | —                     | μA   |
|   |                              | Connected to 1.5V when in operation/idle state | —                     | 13    | —                     | μA   |
|   |                              | Left floating when in operation/idle state     | —                     | 0     | —                     | μA   |
| V <sub>IH</sub>   | High Level Input Voltage     | —  | 0.7PV <sub>DD</sub>   | —     | —                     | V    |
| V <sub>IL</sub>   | Low Level Input Voltage      | —  | —                     | —     | 0.3PV <sub>DD</sub>   | V    |
| V <sub>OH</sub>   | High Level Output Voltage    | —  | PV <sub>DD</sub> -0.4 | —     | PV <sub>DD</sub>      | V    |
| V <sub>OL</sub>   | Low Level Output Voltage     | —  | PV <sub>SS</sub>      | —     | PV <sub>SS</sub> +0.4 | V    |
| I <sub>OH</sub>   | High Level Output Current    | PV <sub>DD</sub> =3V                           | —                     | —     | 5                     | mA   |
| I <sub>OL</sub>   | Low Level Output Current     | PV <sub>DD</sub> =3V                           | —                     | —     | 14                    | mA   |
| <b>Pins OSCIN, OSCOUT Connection Requirements</b>   |                              |  |                       |       |                       |      |
| f <sub>xtal</sub>   | Crystal Frequency            | —  | —                     | 27.12 | —                     | MHz  |
|   | Frequency Tolerance          | —  | —                     | ±10   | ±20                   | ppm  |
| ESR   | Equivalent Series Resistance | —  | —                     | —     | 100                   | Ω    |
| C <sub>L</sub>  | Load Capacitance             | —  | —                     | 10    | —                     | pF   |
| P <sub>xtal</sub>   | Crystal Power Dissipation    | —  | —                     | 50    | 100                   | mW   |

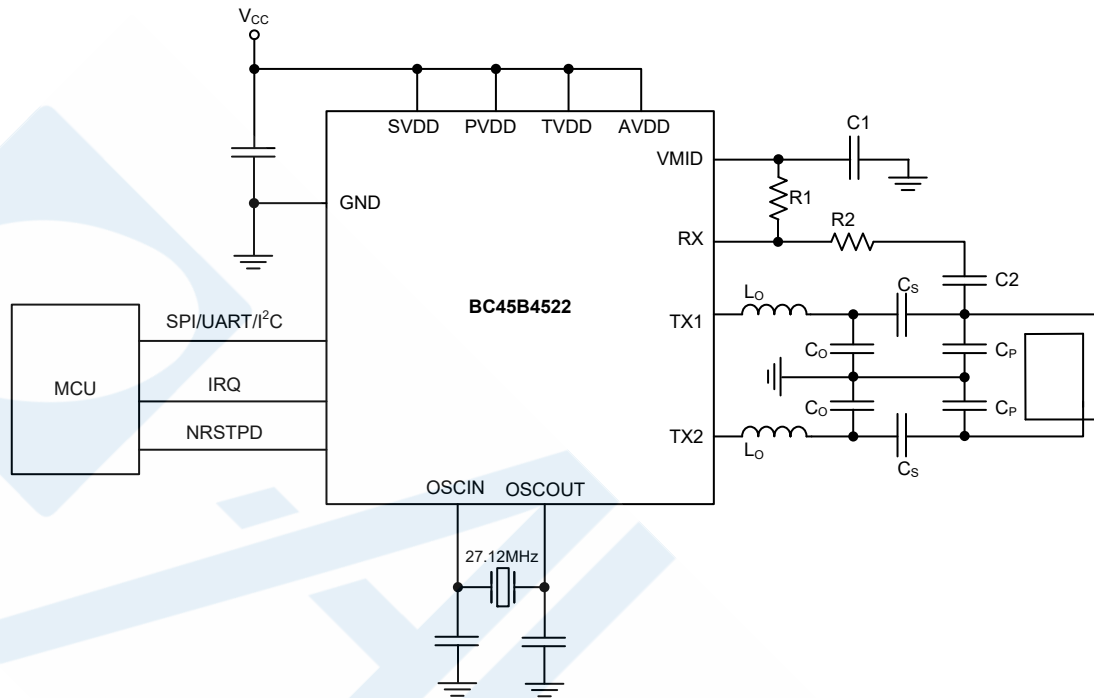
**SPI Characteristics**

| Symbol     | Parameter  | Conditions           | Min. | Typ. | Max. | Unit |
|------------|--|----------------------|------|------|------|------|
| $t_{SCKL}$ | Low Pulse Width                                  | Line SCK             | 50   | —    | —    | ns   |
| $t_{SCKH}$ | High Pulse Width                                 | Line SCK             | 50   | —    | —    | ns   |
| $t_{SHDX}$ | Time Interval from SCK High to Data Input Hold   | SCK to changing MOSI | 25   | —    | —    | ns   |
| $t_{DXSH}$ | Time Interval from Data Input to SCK High Set-up | Changing MOSI to SCK | 25   | —    | —    | ns   |
| $t_{SLDX}$ | Time Interval from SCK Low to Data Output Hold   | SCK to changing MISO | —    | —    | 25   | ns   |
| $t_{SLNH}$ | Time Interval from SCK Low to NSS High           | —                    | 25   | —    | —    | ns   |
| $t_{NHNL}$ | NSS High Time                                    | Before communication | 50   | —    | —    | ns   |
| $t_{DOD}$  | Data Out Delay                                   | —                    | —    | 20   | —    | ns   |
| $t_{DOHZ}$ | Time Interval from Data Out to High Impedance    | —                    | —    | 20   | —    | ns   |


**SPI Timing Diagram**

- Note: 1. The NSS signal must be low to be able to send several bytes in one data stream.  
 2. To send more than one data stream, the NSS line must be set high between data streams.

## Typical Application Circuit



## Communication Interfaces

### Overview

The BC45B4523 supports the SPI, I<sup>2</sup>C and serial UART interfaces. After reset, the device identifies the current host interface type automatically by checking the logic level on the pins. The following table lists the different connection configurations.

| Pin | Interface Type |      |                      |
|-----|----------------|------|----------------------|
|     | UART           | SPI  | I <sup>2</sup> C-bus |
| SDA | RX             | NSS  | SDA                  |
| I2C | 0              | 0    | 1                    |
| EA  | 0              | 1    | EA                   |
| D7  | TX             | MISO | SCL                  |
| D6  | —              | MOSI | ADR0                 |
| D5  | —              | SCK  | ADR1                 |
| D4  | —              | —    | ADR2                 |
| D3  | —              | —    | ADR3                 |
| D2  | —              | —    | ADR4                 |
| D1  | —              | —    | ADR5                 |

### SPI Interface

The contactless chip acts as a slave during SPI communication and uses an SPI clock signal (SCK) generated by the host. The interface can manage data speeds up to 10Mbit/s and is in accordance with the SPI standard.

Reading data from the device using the SPI interface requires to use the byte order shown in the following table. It is possible to read out up to n data bytes.

| Pin  | Byte 0    | Byte 1    | Byte 2    | ... | Byte n    | Byte n+1 |
|------|-----------|-----------|-----------|-----|-----------|----------|
| MOSI | Address 0 | Address 1 | Address 2 | ... | Address n | 00       |
| MISO | X         | Data 0    | Data 1    | ... | Data n-1  | Data n   |

**MISO and MOSI Byte Order – Read Data**

Note: 1. The first sent byte defines both mode and address.

2. X: don't care.
3. The MSB must be sent first.

Writing data to the device using the SPI interface requires to use the byte order shown in the following table. It is possible to write up to n data bytes.

| Pin  | Byte 0    | Byte 1 | Byte 2 | ... | Byte n   | Byte n+1 |
|------|-----------|--------|--------|-----|----------|----------|
| MOSI | Address 0 | Data 0 | Data 1 | ... | Data n-1 | Data n   |
| MISO | X         | X      | X      | ... | X        | X        |

**MISO and MOSI Byte Order – Write Data**

Note: 1. The first sent byte defines both mode and address.

2. X: don't care.
3. The MSB must be sent first.

The address byte must meet the following format, as shown in the table below.

- The MSB of the first byte defines the mode. To read data from the device, the MSB must be set to logic 1. To write data to the device, the MSB must be set to logic 0.
- Bit[6:1] defines the address.
- The LSB must be set to logic 0.

| Address (MOSI) | Bit7 (MSB) | Bit 6   | Bit 5   | Bit4    | Bit 3   | Bit 2   | Bit 1   | Bit 0 (LSB) |
|----------------|------------|---------|---------|---------|---------|---------|---------|-------------|
| Byte 0         | 1 or 0     | Address | Address | Address | Address | Address | Address | 0           |

**Address Byte**
**UART Interface**

The UART default transfer speed is 9.6kbit/s. To modify the transfer speed, the host controller must write a new value to the SerialSpeed register, where the BR\_T0[2:0] and BR\_T1[4:0] bits define the factors for setting the transfer speed. The host controller needs to first configure the register using a data rate of 9.6kbit/s, and then adjusts its data rate corresponding to the new register value.

The BR\_T0[2:0] and BR\_T1[4:0] settings are described below.

| BR_Tn        | Bit 0   | Bit 1    | Bit 2    | Bit 3    | Bit4     | Bit 5    | Bit6     | Bit 7    |
|--------------|---------|----------|----------|----------|----------|----------|----------|----------|
| BR_T0 factor | 1       | 1        | 2        | 4        | 8        | 16       | 32       | 64       |
| BR_T1 range  | 1 to 32 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 |

**BR\_T0 and BR\_T1 Settings**

Examples of different transfer speeds and the relevant register settings are given in the following table.

| Transfer Speed (kbit/s)    | 7.2   | 9.6  | 14.4  | 19.2 | 38.4 | 57.6  | 115.2 | 128   | 230.4 | 460.8 | 921.6 | 1228.8 |
|----------------------------|-------|------|-------|------|------|-------|-------|-------|-------|-------|-------|--------|
| SerialSpeed register value | FAh   | EBh  | DAh   | CBh  | ABh  | 9Ah   | 7Ah   | 74h   | 5Ah   | 3Ah   | 1Ch   | 15h    |
| Transfer speed accuracy    | -0.25 | 0.32 | -0.25 | 0.32 | 0.32 | -0.25 | -0.25 | -0.06 | -0.25 | -0.25 | 1.45  | 0.32   |

**Selectable UART Transfer Speeds**

Note: Transfer speeds exceeding 1228.8kbit/s are not supported.



The transfer speeds shown in the above table are calculated according to the following equations.

- If BR\_T0[2:0]=0

$$\text{Transfer Speed} = (27.12 \times 10^6) \div (\text{BR\_T0} + 1)$$

- If BR\_T0[2:0]>0

$$\text{Transfer Speed} = (27.12 \times 10^6) \div [(\text{BR\_T1} + 33) \div 2^{(\text{BR\_T0} - 1)}]$$

The UART frame format is given in this table. The LSB of the data and address bytes must be sent first. No parity bit is used during transmission.

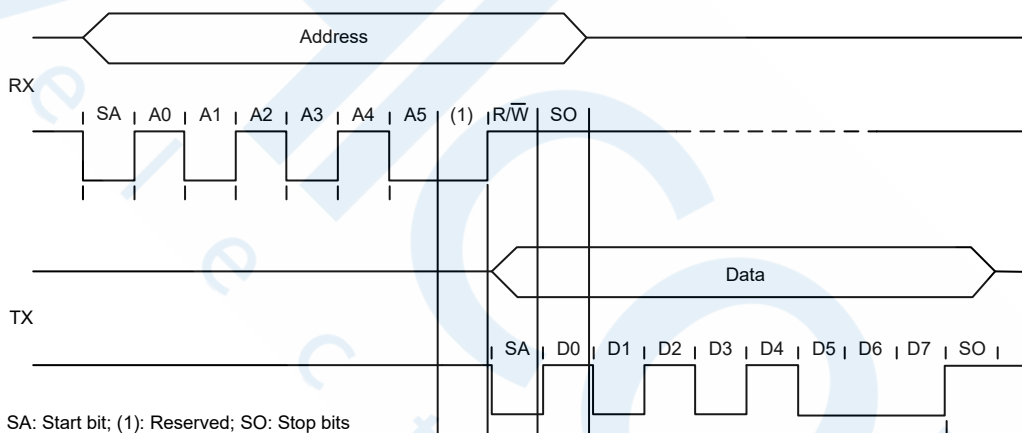
| Bit   | Length | Value |
|-------|--------|-------|
| Start | 1-bit  | 0     |
| Data  | 8-bit  | data  |
| Stop  | 1-bit  | 1     |

**UART Frame Format**

To read out data using the UART interface, the procedure shown in the following table must be used. The first sent byte defines both mode and address.

| Pin | Byte 0  | Byte 1 |
|-----|---------|--------|
| RX  | Address | —      |
| TX  | —       | Data 0 |

**Byte Order for Reading Data**

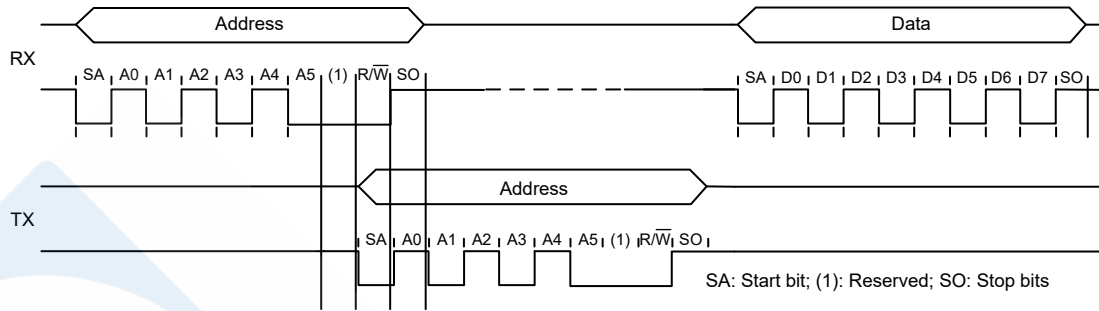


**Timing Diagram for Reading Data**

To write data using the UART interface, the procedure shown in the following table must be used. The first sent byte defines both mode and address.

| Pin | Byte 0    | Byte 1    |
|-----|-----------|-----------|
| RX  | Address 0 | Data 0    |
| TX  | —         | Address 0 |

**Byte Order for Writing Data**


**Timing Diagram for Writing Data**

The address byte must meet the following format, as shown in the table below.

- The MSB of the first byte defines the mode.
  - ♦ MSB=0 for write mode
  - ♦ MSB=1 for read mode
- Bit6 is reserved.
- Bit[5:0] defines the address.

| Bit7 (MSB) | Bit 6    | Bit 5   | Bit4    | Bit 3   | Bit 2   | Bit 1   | Bit 0 (LSB) |
|------------|----------|---------|---------|---------|---------|---------|-------------|
| 1 or 0     | Reserved | Address | Address | Address | Address | Address | Address     |

**Address Byte**

### I<sup>2</sup>C Interface

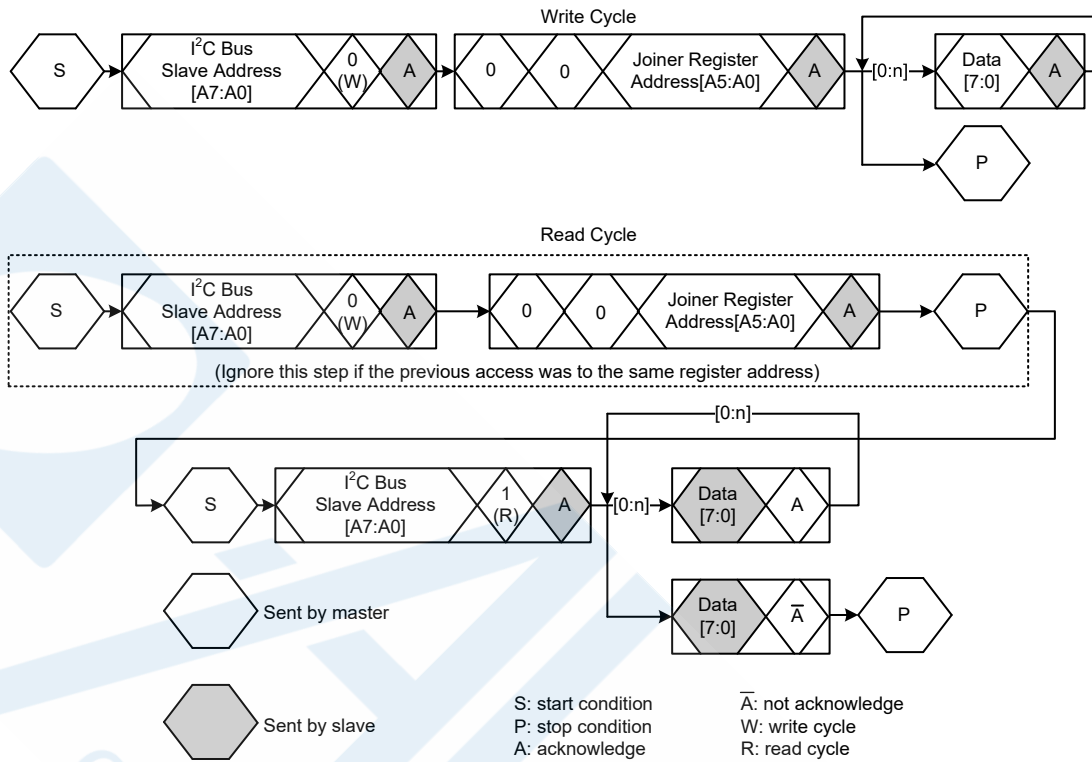
The contactless chip acts as a slave during I<sup>2</sup>C communication and the implemented interface is in accordance with the I<sup>2</sup>C standard. The data transfer speed is up to 400kbit/s.

To write data from the host controller using the I<sup>2</sup>C bus, the following procedure and format must be followed:

- The first byte indicates the device address in accordance with the I<sup>2</sup>C bus standard.
- The second byte indicates the register address, followed by up to n data bytes.
- The Read/Write bit is 0.

To read data from the contactless chip using the I<sup>2</sup>C bus, the following procedure and format must be followed:

- The first byte indicates the device address in accordance with the I<sup>2</sup>C bus standard.
- The second byte indicates the register address. No data bytes are added.
- The Read/Write bit is 0.
- After the write access, read access can be started. The host sends the device address. In response, the contactless chip sends the content of the accessed register to the host.
- The Read/Write bit is 1.



**Register Read and Write Access**

The address byte must meet the following format:

- 7-bit address setting.
  - ♦ If pin EA is set to 0, the higher 4 address bits are fixed at 0101b and the lower 3 bits (ADR0, ADR1, ADR2) can be freely configured by the user.
  - ♦ If pin EA is set to 1, ADR0 to ADR5 can be completely specified on the external pins by the user. ADR6 is always set to logic 0.
- The LSB defines the mode.
  - ♦ LSB=0, write data to the device.
  - ♦ LSB=1, read data from the device.

**MFIN and MFOUT Interface**

The BC45B4522 is divided into a digital circuit block and an analog circuit block. The digital block contains the state machine, encoder and decoder logic circuitry, etc. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured so that the interfacing signals can be routed to the MFIN and MFOUT pins. This configuration is implemented using the MFOutSel[3:0] and DriverSel[1:0] bits in the TxSel register and the UARTSel[1:0] bits in the RxSel register.

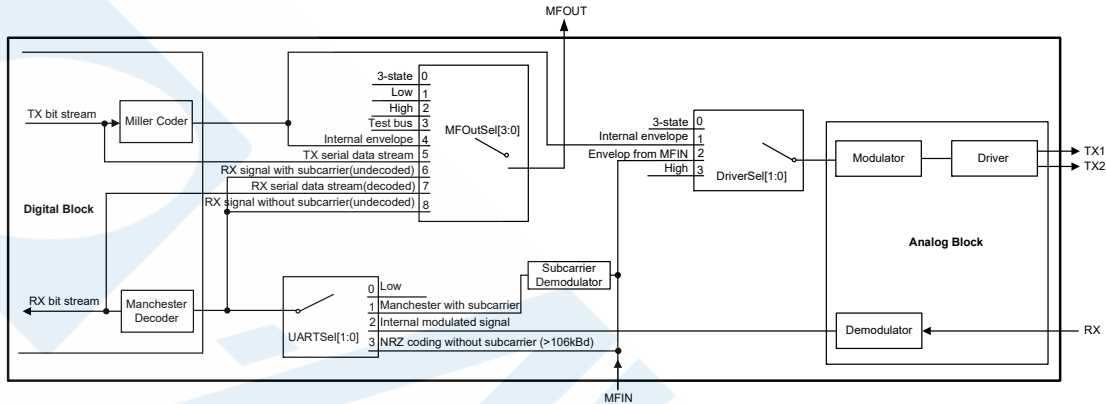
This topology allows some parts of the analog block to be connected to the digital block of another device.

The MFOutSel[3:0] bits in the TxSel register is used to measure ISO/IEC14443 A related signals. This is especially important during the design and test phases as it enables checking of the transmitted and received data.

Pins MFOUT and MFIN can find important use in active antenna applications. An external active antenna circuit can be connected to the BC45B4522's digital block. The MFOutSel[3:0] bits must be configured to 0100b so that the internal Miller encoded signal can be sent to the MFOUT pin. The UARTSel[1:0] bits must be configured to 01b so that a Manchester signal with subcarrier is received on the MFIN pin.

It is possible to connect a passive antenna to the TX1, TX2 and RX pins using an appropriate filter and matching circuitry, and simultaneously an active antenna to the MFIN and MFOUT pins. In this circuit configuration, two RF circuits can be driven by the same host processor.

Note that the MFIN and MFOUT pins have a dedicated power supply on pin SVDD with the ground on pin PVSS. When the MFIN pin is not used, it must be connected to either pin SVDD or pin PVSS. When the SVDD pin is not used, it must be connected to pin PVDD or any other power supply pin.



MFIN and MFOUT Signal Routing Diagram

## Functional Description

### CRC Coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the CRCPreset[1:0] setting in the Mode register.
- The CRC polynomial for the 16-bit CRC is  $X^{16} + X^{12} + X^5 + 1$ .
- The CRCResult\_H and CRCResult\_L registers indicate the CRC calculation result high byte and low byte respectively.
- The MSBFirst bit in the Mode register indicates that data will be loaded with the MSB first.

| Parameter           | Value   |
|---------------------|---|
| CRC register length | 16-bit CRC  |
| CRC algorithm       | Algorithm according to ISO/IEC 14443 A and ITU-T                                      |
| CRC preset value    | 0000h, 6363h, A671h or FFFFh depending on CRCPreset[1:0] setting in the Mode register |

### FIFO Buffer

The BC45B4522 contains an 8×64 FIFO buffer. It is used to cache the input and output data streams for communication between the host and the device internal state machine. It can manage up to 64 bytes of data streams without considering timing limitations.

### Accessing the FIFO Buffer

The FIFO buffer input and output data bus is connected to the FIFOData register. Writing to the FIFOData register will store one byte in the FIFO buffer and increase the internal FIFO buffer write pointer by 1. Reading from the FIFOData register will read the data stored in the pointed FIFO buffer and decrease the FIFO buffer read pointer by 1. The distance between the FIFO buffer write and read pointers can be obtained by reading the FIFOLevel register.

When the host controller sends a command, the BC45B4522 can access the FIFO buffer according to the command while the command is in progress. The FIFO buffer can continue to be used for input and output only when it is valid. The host controller must ensure that there are no unintentional accesses to the FIFO buffer.

### Controlling the FIFO Buffer

The FIFO buffer pointers can be reset by setting the FlushBuffer bit in the FIFOLevel register to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the BufferOvfl flag in the Error register is cleared to zero. In this situation, the stored bytes can no longer be accessible, allowing the FIFO buffer to store another 64 data bytes.

### FIFO Buffer State Information

The host device can obtain the following FIFO buffer state information:

- The number of data bytes stored in the FIFO buffer: FIFOLevel[6:0] bits in the FIFOLevel register
- FIFO buffer almost full warning: HiAlert bit in the Status1 register
- FIFO buffer almost empty warning: LoAlert bit in the Status1 register
- FIFO buffer overflow warning: BufferOvfl bit in the Error register, which can be cleared only by setting the FlushBuffer bit in the FIFOLevel register

The BC45B4522 can generate an interrupt signal when any one of the following conditions occurs:

- The LoAlertIEn bit in the ComIEn register is set to logic 1, it activates the IRQ pin when the LoAlert bit in the Status1 register changes to logic 1.
- The HiAlertIEn bit in the ComIEn register is set to logic 1, it activates the IRQ pin when the HiAlert bit in the Status1 register changes to logic 1.
- If the WaterLevel[5:0] value set in the WaterLevel register is greater than or equal to the remaining space in the FIFO buffer, the HiAlert bit is set to logic 1:

$$\text{HiAlert}=1 \text{ if } (64-\text{FIFOLength})\leq\text{WaterLevel}$$

- If the WaterLevel[5:0] value set in the WaterLevel register is greater than or equal to the used space in the FIFO buffer, the LoAlert bit is set to logic 1:

$$\text{LoAlert}=1 \text{ if } \text{FIFOLength}\leq\text{WaterLevel}$$

### Interrupt Request System

The BC45B4522 indicates various interrupt events by setting the IRq bit in the Status1 register or by activating the IRQ pin. The signal on the IRQ pin can be used to interrupt the host to use its interrupt handling capabilities. This greatly improves the efficiency of host software execution.

### Interrupt Source Overview

The following table lists the available interrupt flags, the corresponding interrupt source and the trigger condition for their activation.

The TimerIRq interrupt flag in the ComIrq register being set high indicates an interrupt generated by the timer. When the timer decreases from 1 to 0, this flag will be set high.

The TxIRq flag in the ComIrq register being set high indicates that the transmitter sending has finished. When the state changes from sending data to sending the end of the frame, the transmitter will automatically set the corresponding interrupt flag high. The CRC coprocessor will set the CRCIRq flag high in the DivIrq register after processing all the data in the FIFO buffer which is indicated by the CRCReady bit.

The RxIRq flag in the ComIrq register being set high indicates that the end of data reception has been detected.

The IdleIRq flag in the ComIrq register will be set high if a command execution has finished and the Command[3:0] field in the Command register has changed to the Idle state.

When the HiAlert bit is set to 1 and the HiAlertIRq flag in the ComIrq register is set to 1, it indicates that the remaining space in the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits. When the LoAlert bit is set to 1 and the LoAlertIRq flag in the ComIrq register is set to 1, it indicates that the used space in the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ErrIRq flag in the ComIrq register being set high indicates that an error has been detected during the contractless UART transmission and reception. This is indicated when any bit in the Error register is set to logic 1.

The TagDetIRq flag in the DivIrq register being set high indicates that in the LPCD mode an external contractless card has been detected.

| Intrrupt Flag | Interrupt Source  | Trigger Action  |
|---------------|-------------------|---|
| TimerIRq      | Timer             | The timer counts from 1 to 0                                |
| TxIRq         | Transmitter       | A data stream transmitting ends                             |
| CRCIRq        | CRC coprocessor   | All data in the FIFO buffer has been processed              |
| RxIRq         | Receiver          | A data stream receiving ends                                |
| IdleIRq       | ComIrq register   | Command execution ends                                      |
| HiAlertIRq    | FIFO buffer       | FIFO buffer is almost full                                  |
| LoAlertIRq    | FIFO buffer       | FIFO buffer is almost empty                                 |
| ErrIRq        | Contractless UART | An error is detected  |
| TagDetIRq     | LPCD trigger      | In the LPCD mode, a card enters the antenna effective range |

## Timer Unit

The BC45B4522 has a timer unit which can be used by the external host to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Time-out counter
- Watchdog counter
- Stopwatch
- Programmable one-shot trigger
- Periodic trigger

The timer unit can be used to measure the time interval between two events or to indicate the occurrence of a specified event after a certain period of time. The timer can be triggered by events explained in the following paragraphs. The timer unit does not affect any internal events, for example, a timer time-out event during data reception does not affect the automatic processing of this process. In addition, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 13.56MHz, which is obtained by dividing the frequency of a 27.12MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

The prescaler (TPrescaler) is a 12-bit counter, which is set using the TPrescaler\_Hi[3:0] bits in the TMode register and the TPrescaler\_Lo[7:0] bits in the TPrescaler register. The 16-bit reload value for the counter, TReloadVal, can be set between 0 and 65535 using the TReload\_H and TReload\_L registers. The current value of the timer is indicated in the TCouterVal\_H and TCouterVal\_L registers.

When the counter value reaches 0, an interrupt is automatically generated, which is indicated by the TimerIRq flag in the ComIrq register. If enabled, this interrupt signal can be indicated on the IRQ pin. The TimerIRq flag can be set and reset by the host. Depending on the configuration, the timer can stop at 0 or restart with the value set in the TReload\_H and TReload\_L registers.

The timer status is indicated by the TRunning bit in the Status1 register.

The timer can be started using the TStartNow bit in the Control register and stopped using the TStopNow bit in the same register.

To meet some specific protocol requirements, the timer can also be activated automatically by setting the TAuto bit

in the TMode register to logic 1.

The delay time of a timing process is set by the reload value plus one. The total delay time is calculated using the following equation:

$$t_d = (TPrescaler \times 2 + 1) \times (TReloadVal + 1) \div 13.56\text{MHz}$$

An example of calculating the total delay time is shown below, where TPrescaler=4095 and TReloadVal=65535:

$$39.59\text{s} = (4095 \times 2 + 1) \times (65535 + 1) \div 13.56\text{MHz}$$

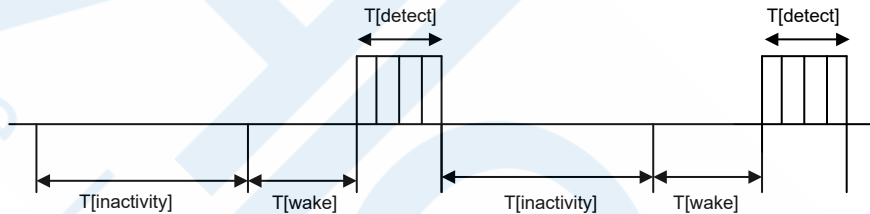
For example, a delay unit of 25μs requires 339 timer clock cycles to be counted and a TPrescaler value of 169. This configuration allows the timer to count every 25μs up to 65535 times.

### LPCD Unit

The LPCD is the abbreviation of Low Power external Card Detection. This function allows the device to detect whether an external contactless card is close to it with a very low standby power consumption. If an card has been detected, an interrupt can be output to inform the host MCU to enter the normal reader communication mode and implement data exchange with the card.

### LPCD Operating Principle

The LPCD mode is divided into three stages, T[inactivity](sleep period), T[wake](active period) and T[detect](detection period), corresponding to different actions, as shown below.



In the initial state, the chip detects the antenna field strength in the current field and automatically records it. When a card is within the effective range of the antenna, it will cause the antenna field strength to change beyond the Delta[3:0] value in the LPCD register, then the chip will automatically change to the reader state and trigger the TagDetIRq interrupt. The LPCD function related registers include the LPCD, WUPeriod and SwingsCnt.

The LPCD time parameters are described below:

- Sleep period:  $T[\text{inactivity}] = WUPeriod[7:0] \times 256 \times Tclk\_32k$
- Active period:  $T[\text{wake}] = 400\mu\text{s}$  (Typ.)
- Detection period:  $T[\text{detect}] = SwingsCnt[3:0] \times 16 \times 4 \times Tclk\_27M12$
- Card detection total time =  $(T[\text{inactivity}] + T[\text{wake}] + T[\text{detect}] \times (Skip[2:0] + 1))$

### TX Driver

The signals on the TX1 and TX2 pins are signals modulated by a 13.56MHz carrier, which can be used to directly drive an antenna with some passive components for matching and filtering.

The signals on the TX1 and TX2 pins can be configured using the TxControl register. The modulation index can be set by adjusting the impedance of the driver so as to adjust the output power, current consumption and operating distance. The impedance of the P driver is configured using the CWGsP and ModGsP registers. The impedance of the N driver is configured using the GsN register. The modulation index also depends on antenna design and tuning.

## Power Saving Modes

### Hardware Power-down

The hardware power-down mode is enabled when the NRSTPD pin is pulled low. This mode turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and their functionality is turned off (except pin NRSTPD). The output pins remain at either a high or low level.

### Software Power-down

The software power-down mode is entered immediately after the PowerDown bit in the Command register is set to logic 1. This mode turns off all internal current sinks including the oscillator buffer. However, the digital input buffers are not separated from the input pins and remain their functionality. The status of the digital output pins remains unchanged.

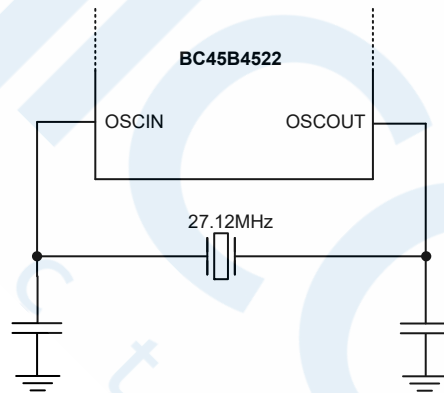
During the software power-down, all register values, FIFO buffer content and configuration remain unchanged.

After setting the PowerDown bit to logic 0, it takes 1024 clocks to exit the software power-down mode. Setting the PowerDown bit low does not immediately clear it. This bit is cleared automatically by the chip when the software power-down mode is exited.

### Transmitter Power-down

The transmitter power-down mode turns off the internal antenna drivers, thereby switching off the RF field. The transmitter power-down mode is entered by setting the TxRFEn bit in the TxControl register to 00b.

### Oscillator Circuit



Quartz Crystal Connection

The clock applied to the BC45B4522 provides a time basis for the encoder and decoder synchronized to the system. Therefore, the stability of the clock frequency is an important factor to ensure the good performance of the system. To achieve the best performance, clock jitter must be as minimized.



## Registers

### Register Bit Behavior

Depending on the functionality of the register, the access conditions of the registers are also different. The following table describes different access conditions for the registers.

| Abbreviation | Behavior   | Description  |
|--------------|------------|--|
| R/W          | Read/Write | These bits can be read and written by the host controller. Since they are used only for control, their contents are not affected by the internal state machine. For example, the ComIEEn register can be read and written by the host controller, but it can only be read by the internal state machine and cannot be changed by it. |
| D            | Dynamic    | These bits can be read and written by the host controller. They can also be written automatically by the internal state machine. For example, the Command register automatically changes the value of certain bits in it after command execution.  |
| W            | Write only | Reading these register bits always returns zero.   |
| R            | Read only  | These register bits are determined by the internal states only.  |
| Reserved     | —          | These register bits are reserved for future use and cannot be changed.   |

### Register Overview

To access the registers of pages 4–6, the PageSel register of page 3 should first be configured to the correct switch value before executing any operations to the registers in the corresponding page.

| Address<br>(Hex) | Register Name | Function  |
|------------------|---------------|---|
| <b>Page 0</b>    |               |   |
| 00h              | Reserved      | —   |
| 01h              | Command       | Start and stop command execution                    |
| 02h              | ComIEEn       | Interrupt request enable or disable control bits    |
| 03h              | DivIEEn       | Interrupt request enable or disable control bits    |
| 04h              | ComIrq        | Interrupt request bits                              |
| 05h              | DivIrq        | Interrupt request bits                              |
| 06h              | Error         | Error status of the last command executed           |
| 07h              | Status1       | Communication status bits                           |
| 08h              | Status2       | Receiver and transmitter status bits                |
| 09h              | FIFOData      | 64-byte FIFO buffer input/output                    |
| 0Ah              | FIFOLevel     | Number of bytes stored in the FIFO buffer           |
| 0Bh              | WaterLevel    | Level for FIFO buffer overflow and empty warning    |
| 0Ch              | Control       | Internal controller                                 |
| 0Dh              | BitFraming    | Adjustment for bit-oriented frames                  |
| 0Eh              | Coll          | Bit position of the first bit-collision detected    |
| <b>Page 1</b>    |               |   |
| 10h              | Reserved      | —   |
| 11h              | Mode          | General mode setting for transmitting and receiving |
| 12h              | TxMode        | Transmission data rate and frame format             |
| 13h              | RxMode        | Reception data rate and frame format                |
| 14h              | TxControl     | Antenna driver pins TX1 and TX2 control             |
| 15h              | TxASK         | Transmission modulation settings                    |
| 16h              | TxSel         | Antenna driver signal source selection              |
| 17h              | RxSel         | Internal receiver settings                          |
| 18h              | Reserved      | —   |
| 19h              | Demod         | Demodulation settings                               |

| Address<br>(Hex) | Register Name | Function   |
|------------------|---------------|--|
| 1Ch              | MFTx          | Transmission waiting time control  |
| 1Dh              | MfRx          | Parity function and high-pass bandwidth settings   |
| 1Eh              | TypeB         | ISO/IEC 14443 B control  |
| 1Fh              | SerialSpeed   | Serial UART data rate selection  |
| <b>Page 2</b>    |               |  |
| 20h              | Reserved      | —  |
| 21h              | CRCResult_H   | CRC result high byte   |
| 22h              | CRCResult_L   | CRC result low byte  |
| 23h              | Reserved      | —  |
| 24h              | ModWidth      | Modulation width control   |
| 25h              | Reserved      | —  |
| 26h              | RFCfg         | Receiver gain setting  |
| 27h              | GsN           | Controls the conductance of N driver output during non-modulation period and modulation period |
| 28h              | CWGsP         | Controls the conductance of P driver output during non-modulation period                       |
| 29h              | ModGsP        | Controls the conductance of P driver output during modulation period                           |
| 2Ah              | TMode         | Internal timer settings  |
| 2Bh              | TPrescaler    |  |
| 2Ch              | TReload_H     | 16-bit timer reload value high byte  |
| 2Dh              | TReload_L     | 16-bit timer reload value low byte   |
| 2Eh              | TCounterVal_H | 16-bit timer current value high byte   |
| 2Fh              | TCounterVal_L | 16-bit timer current value low byte  |
| <b>Page 3</b>    |               |  |
| 33h              | TestPinEn     | Programmable I/O (D1-D6) enable bits   |
| 34h              | TestPinValue  | Programmable I/O (D1-D6) control bits  |
| 37h              | PageSel       | Controls the register page switching   |
| <b>Page 4</b>    |               |  |
| 31h              | TestSel       | MFOUT output signal selection  |
| 32h              | DataPullID    | Pull-high control for MFIN and programmable I/O  |
| 33h              | RxAlgorithm0  | Demodulation algorithm adjustment  |
| 34h              | AGCCfg0       | Automatic gain control bits  |
| 35h              | AGCCfg1       | Automatic gain control bits  |
| 36h              | RxAlgorithm1  | Demodulation algorithm adjustment  |
| 38h              | RxAlgorithm2  | Demodulation algorithm adjustment  |
| 39h              | RxAlgorithm3  | Demodulation algorithm adjustment  |
| 3Ah              | RxCk          | TypeA waveform falling time adjustment; phase selection  |
| 3Bh              | RxBand        | Signal-to-noise ratio adjustment   |
| 3Ch              | LPCD          | LPCD control bits  |
| 3Dh              | WUPeriod      | LPCD sleep time setting  |
| 3Eh              | SwingsCnt     | LPCD enable; LPCD detection time setting   |
| 3Fh              | Special       | Receiver demodulation control  |
| <b>Page 5</b>    |               |  |
| 31h              | Analog        | High temperature protection control bits   |
| 32h              | Noise         | Noise threshold control bits   |
| 33h              | StepCtrl      | Transmitter modulation control bits  |
| 34h              | AgcMin        | AGC amplitude threshold setting  |
| 38h              | RxAlgorithm6  | Demodulation algorithm adjustment  |

| Address<br>(Hex) | Register Name | Function                              |
|------------------|---------------|---------------------------------------|
| 39h              | RxAlgorithm7  | Demodulation algorithm adjustment     |
| 3Ah              | RxAlgorithm8  | Demodulation algorithm adjustment     |
| 3Bh              | RxAlgorithm9  | Demodulation algorithm adjustment     |
| <b>Page 6</b>    |               |                                       |
| 31h              | LPCDRef       | LPCD reference value                  |
| 32h              | LPCDDet       | LPCD detected value                   |
| 33h              | Calibration   | LPCD calibration control bits         |
| 34h              | RC27MCalValue | LPCD 27.12MHz clock calibration value |
| 35h              | RC32KCalValue | LPCD 32kHz clock calibration value    |
| 36h              | LPCDADCRef    | LPCD ADC reference level              |
| 38h              | CWGsN_LPCD    | LPCD N driver control                 |
| 39h              | CWGsP_LPCD    | LPCD P driver control                 |

## Register Description

### Public Register description

#### Page 0

#### • Command Register

Start and stop command execution.

| Address | Bit         | 7        | 6 | 5      | 4         | 3            | 2 | 1 | 0 |
|---------|-------------|----------|---|--------|-----------|--------------|---|---|---|
| 01h     | Name        | Reserved |   | RcvOff | PowerDown | Command[3:0] |   |   |   |
|         | Type        | R        |   | R/W    | R/W       | R/W          |   |   |   |
|         | Reset Value | 0        | 0 | 1      | 0         | 0            | 0 | 0 | 0 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5 **RcvOff:** Receiver analog block on/off control  
0: On  
1: Off

Bit 4 **PowerDown:** Software power-down mode control  
0: Chip in ready state  
1: Chip enters power-down mode

Bit 3~0 **Command[3:0]:** Command control  
Based on the value of these bits, the corresponding command is activated. Reading these bits shows which command is actually being executed. Refer to the Command Overview section for details.

#### • ComIE n Register

Interrupt enable and disable control bits.

| Address | Bit         | 7      | 6      | 5      | 4        | 3           | 2           | 1       | 0         |
|---------|-------------|--------|--------|--------|----------|-------------|-------------|---------|-----------|
| 02h     | Name        | IRqInv | TxIE n | RxIE n | IdleIE n | HiAlertIE n | LoAlertIE n | ErrIE n | TimerIE n |
|         | Type        | R/W    | R/W    | R/W    | R/W      | R/W         | R/W         | R/W     | R/W       |
|         | Reset Value | 1      | 0      | 0      | 0        | 0           | 0           | 0       | 0         |

Bit 7 **IRqInv:** IRQ pin state non-inverting/inverting with IRq bit state (Status1 register) control  
0: Non-invert  
1: Invert

In combination with the IRQPushPull bit in the DivIE n register, the default value of logic 1 ensures that the output level on the IRQ pin is 3-state.

- Bit 6      **TxIEN**: Send TxIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 5      **RxIEN**: Send RxIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 4      **IdleIEN**: Send IdleIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 3      **HiAlertIEN**: Send HiAlertIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 2      **LoAlertIEN**: Send LoAlertIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 1      **ErrIEN**: Send ErrIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 0      **TimerIEN**: Send TimerIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed

• **DivIEN Register**

Interrupt enable and disable control bits.

| Address | Bit         | 7           | 6        | 5         | 4          | 3        | 2      | 1        | 0 |
|---------|-------------|-------------|----------|-----------|------------|----------|--------|----------|---|
| 03h     | Name        | IRQPushPull | Reserved | TagDetIEn | MfinActIEn | Reserved | CRCIEn | Reserved |   |
|         | Type        | R/W         | —        | R/W       | R/W        | —        | R/W    | —        |   |
|         | Reset Value | 0           | 0        | 0         | 0          | 0        | 0      | 0        | 0 |

- Bit 7      **IRQPushPull**: IRQ output control  
0: Open-drain output  
1: Standard CMOS output
- Bit 6      **Reserved**: Reserved bit
- Bit 5      **TagDetIEN**: Send TagDetIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 4      **MfinActIEN**: Send MfinActIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 3      **Reserved**: Reserved bit
- Bit 2      **CRCIEN**: Send CRCIRq interrupt request to IRQ pin  
0: Not allowed  
1: Allowed
- Bit 1~0    **Reserved**: Reserved bits

• **ComIrq Register**

Interrupt request bits. All bits in this register can be cleared by software.

| Address | Bit         | 7    | 6     | 5     | 4       | 3          | 2          | 1      | 0        |
|---------|-------------|------|-------|-------|---------|------------|------------|--------|----------|
| 04h     | Name        | Set1 | TxIRq | RxIRq | IdleIRq | HiAlertIRq | LoAlertIRq | ErrIRq | TimerIRq |
|         | Type        | W    | D     | D     | D       | D          | D          | D      | D        |
|         | Reset Value | 0    | 0     | 0     | 1       | 0          | 1          | 0      | 0        |

- Bit 7      **Set1**: ComIrq register interrupt request flag control  
0: Clear interrupt request flag in the ComIrq register  
1: Set interrupt request flag in the ComIrq register

Hardware set high: When a related event occurs, the corresponding interrupt request flag in this register is automatically set high and an interrupt request is generated. It requires to set both Set1 and the corresponding interrupt request flag to 0 to clear the interrupt request.

Software set high: Set both Set1 and the corresponding interrupt request flag in this register to 1 to generate the interrupt request. It requires to set both Set1 and the corresponding interrupt request flag to 0 to clear the interrupt request.

- Bit 6 TxIRq:** Data transmission complete interrupt request flag  
 0: No request  
 1: Interrupt request  
 This flag is set high immediately after the last data bit has been sent.
- Bit 5 RxIRq:** Receiver detected valid data interrupt request flag  
 0: No request  
 1: Interrupt request  
 If the RxNoErr bit in the RxMode register is set high and the data received in the FIFO is valid, this interrupt request flag will be set high.
- Bit 4 IdleIRq:** Idle interrupt request flag  
 0: No request  
 1: Interrupt request  
 If a command terminates, such as changing from any command to the Idle command, this interrupt request flag will be set high. If an unknown command is started, the Command[3:0] field in the Command register will be 0000b and this interrupt request flag will be set high. Starting the Idle command does not set this flag.
- Bit 3 HiAlertIRq:** FIFO HiAlert interrupt request flag  
 0: No request  
 1: Interrupt request  
 This flag will be set high when the HiAlert bit in the Status1 register is set to 1. This flag can only be reset using the Set1 bit of this register.
- Bit 2 LoAlertIRq:** FIFO LoAlert interrupt request flag  
 0: No request  
 1: Interrupt request  
 This flag will be set high when the LoAlert bit in the Status1 register is set to 1. This flag can only be reset using the Set1 bit of this register.
- Bit 1 ErrIRq:** Error interrupt request flag  
 0: No request  
 1: Interrupt request  
 This flag will be set high when any bit of the Error register is set high.
- Bit 0 TimerIRq:** Timer interrupt request flag  
 0: No request  
 1: Interrupt request  
 This flag will be set high when the timing value TCounterVal indicated by the TCounterVal\_H and TCounterVal\_L registers is decreased to 0.

• **DivIrq Register**

Interrupt request bits. All bits in this register can be cleared by software.

| Address | Bit         | 7    | 6        | 5         | 4          | 3        | 2      | 1        | 0 |
|---------|-------------|------|----------|-----------|------------|----------|--------|----------|---|
| 05h     | Name        | Set2 | Reserved | TagDetIRq | MfinActIRq | Reserved | CRCIRq | Reserved |   |
|         | Type        | W    | —        | R/W       | D          | —        | D      | —        |   |
|         | Reset Value | 0    | 0        | 0         | 0          | 0        | 0      | 0        | 0 |

- Bit 7 Set2:** DivIrq register interrupt request flag control  
 0: Clear interrupt request flag in the DivIrq register  
 1: Set interrupt request flag in the DivIrq register  
 Hardware set high: When a related event occurs, the corresponding interrupt request flag in this register is automatically set high and an interrupt request is generated. It requires to set both Set2 and the corresponding interrupt request flag to 0 to clear the interrupt request.

Software set high: Set both Set2 and the corresponding interrupt request flag in this register to 1 to generate the interrupt request. It requires to set both Set2 and the corresponding interrupt request flag to 0 to clear the interrupt request.

- Bit 6 **Reserved:** Reserved bit
- Bit 5 **TagDetIRq:** Card detection interrupt request flag  
0: No request  
1: Interrupt request  
This flag will be set high when a card has been detected.
- Bit 4 **MfinActIRq:** MFIN valid interrupt request flag  
0: No request  
1: Interrupt request  
This flag will be set high when either a rising edge or a falling edge has been detected.
- Bit 3 **Reserved:** Reserved bit
- Bit 2 **CRCIRq:** CRC interrupt request flag  
0: No request  
1: Interrupt request  
This flag will be set high when the CRC command is valid and all data has been checked.
- Bit 1~0 **Reserved:** Reserved bits

• **Error Register**

This register shows the error status of the last command execution.

| Address | Bit         | 7     | 6       | 5        | 4          | 3       | 2      | 1         | 0           |
|---------|-------------|-------|---------|----------|------------|---------|--------|-----------|-------------|
| 06h     | Name        | WrErr | TempErr | Reserved | BufferOvfl | CollErr | CRCErr | ParityErr | ProtocolErr |
|         | Type        | R     | R       | —        | R          | R       | R      | R         | R           |
|         | Reset Value | 0     | 0       | 0        | 0          | 0       | 0      | 0         | 0           |

- Bit 7 **WrErr:** Write error flag  
0: No write error occurs  
1: Write error occurs  
If the host writes data to the FIFO buffer during the MFAuthent command execution or during the period between the last bit transmitted on the RF interface and the last bit received on the RF interface, this flag will be set high.
- Bit 6 **TempErr:** Temperature sensor over temperature flag  
0: No over temperature occurs  
1: Over temperature occurs  
This flag will be set high when the internal temperature sensor has detected an over temperature situation, in which case the antenna drivers will be turned off automatically.
- Bit 5 **Reserved:** Reserved bit
- Bit 4 **BufferOvfl:** FIFO buffer overflow flag  
0: Buffer not overflows  
1: Buffer overflows  
When the FIFO buffer is full, if the host or the chip internal state machine (such as receiver) continues to write data to the buffer, this flag will be set high. It can only be cleared by the FlushBuffer bit in the FIFOLevel register.
- Bit 3 **CollErr:** Data bit collision flag  
0: No collision occurs  
1: Collision occurs  
This flag will be set high when a bit collision has been detected. It is automatically cleared during the receiver start-up. This flag is only effective in the bit anti-collision mechanism of the 106kbit/s communication, and is usually set to 0 under 212kbit/s, 424kbit/s and 848kbit/s communication protocols.
- Bit 2 **CRCErr:** CRC error flag  
0: No CRC error occurs  
1: CRC error occurs  
This flag will be set high when the RxCRCEn bit in the RxMode register is set to 1 and a CRC

calculation error occurs. It is automatically cleared during the receiver start-up.

Bit 1 **ParityErr:** Parity error flag  
 0: No parity error occurs  
 1: Parity error occurs

This flag will be set high when a parity error occurs. It is automatically cleared during the receiver start-up. This flag is only effective in the 106kbit/s ISO/IEC 14443 A communication.

Bit 0 **ProtocolErr:** SOF(Start of Frame) error flag  
 0: No SOF error occurs  
 1: SOF error occurs

This flag will be set high when the SOF is incorrect. It is automatically cleared during the receiver start-up. This flag is only effective in the 106kbit/s communication.

#### • Status1 Register

CRC, interrupt and FIFO buffer status bits.

| Address | Bit         | 7        | 6     | 5        | 4   | 3        | 2        | 1       | 0       |
|---------|-------------|----------|-------|----------|-----|----------|----------|---------|---------|
| 07h     | Name        | Reserved | CRCOk | CRCReady | IRq | TRunning | Reserved | HiAlert | LoAlert |
|         | Type        | —        | R     | R        | R   | R        | —        | R       | R       |
|         | Reset Value | 0        | 0     | 1        | 0   | 0        | 0        | 0       | 1       |

Bit 7 **Reserved:** Reserved bit

Bit 6 **CRCOk:** CRC calculation correct flag  
 0: CRC calculation is in progress or CRC calculation is incorrect  
 1: CRC calculation is correct

This flag will be set high when the CRC result is 0. Since this bit value is uncertain during transmission or reception, the CRCErr bit in the Error register can be used for CRC result checking. This bit changes to 0 during CRC coprocessor calculation and changes to 1 when the CRC calculation is correctly executed.

Bit 5 **CRCReady:** CRC calculation complete flag  
 0: CRC calculation is not completed  
 1: CRC calculation is completed

This flag will be set high when the CRC calculation is completed. It is valid only when executing the CRC calculation of the CalcCRC command.

Bit 4 **IRq:** Interrupt request indication bit  
 0: No request  
 1: Interrupt request

To indicate any interrupt request, the corresponding interrupt enable bit must be set. Refer to the ComIE n and DivIE n register.

Bit 3 **TRunning:** Timer running flag  
 0: Not running  
 1: Running

When the timer is running, which means when the TCounterVal value is decremented with the timer clock, this flag is set high.

Bit 2 **Reserved:** Reserved bit

Bit 1 **HiAlert:** FIFO high level warning flag  
 If  $(64 - \text{FIFOLength}) \leq \text{WaterLevel}$ , HiAlert is set to 1.

Bit 0 **LoAlert:** FIFO low level warning flag  
 If  $\text{FIFOLength} \leq \text{WaterLevel}$ , LoAlert is set to 1.

**• Status2 Register**

Transmitter and receiver status bits.

| Address | Bit         | 7             | 6        | 5        | 4 | 3           | 2               | 1 | 0 |
|---------|-------------|---------------|----------|----------|---|-------------|-----------------|---|---|
| 08h     | Name        | TempSensClear | Reserved | Reserved |   | MFCrypto1On | ModemState[2:0] |   |   |
|         | Type        | R/W           | —        | —        |   | D           | R               |   |   |
|         | Reset Value | 0             | 0        | 0        | 0 | 0           | 0               | 0 | 0 |

- Bit 7 **TempSensClear:**  
When the temperature falls below the 120°C limit alarm value, the temperature error alarm can be removed by setting this bit high.
- Bit 6~4 **Reserved:** Reserved bits
- Bit 3 **MFCrypto1On:** Crypto\_M unit off/on control  
0: Off  
1: On  
Setting this bit to 1 turns on the Crypto\_M unit to enter the Crypto\_M standard card reader mode, where all data communication with the card is encrypted. This bit can only be set to 1 by a successful execution of the MFAuthent command and is cleared by software.
- Bit 5 **ModemState[2:0]:** Transmitter and receiver state machine status  
000: Idle  
001: Wait for the StartSend bit setting in the BitFraming register  
010: TxWait – If the TxWaitRF bit in the Mode register is set to 1, wait until RF field is present. The minimum time for TxWait is determined by TxWait[4:0].  
011: Transmitting  
100: RxWait – If the TxWaitRF bit in the Mode register is set to 1, wait until RF field is present. The minimum time for RxWait is determined by RxWait[5:0].  
101: Wait for data  
110: Receiving  
111: Undefined

**• FIFOData Register**

64-byte FIFO buffer input and output.

| Address | Bit         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---------------|---|---|---|---|---|---|---|
| 09h     | Name        | FIFOData[7:0] |   |   |   |   |   |   |   |
|         | Type        | D             |   |   |   |   |   |   |   |
|         | Reset Value | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- Bit 7~0 **FIFOData[7:0]:** Input/output port for the internal 64-byte FIFO buffer  
It acts as a parallel in / parallel output converter for all data stream inputs and outputs of the buffer.

**• FIFOLevel Register**

This register indicates the number of bytes stored in the FIFO buffer.

| Address | Bit         | 7           | 6              | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------|----------------|---|---|---|---|---|---|
| 0Ah     | Name        | FlushBuffer | FIFOLevel[6:0] |   |   |   |   |   |   |
|         | Type        | W           | R              |   |   |   |   |   |   |
|         | Reset Value | 0           | 0              | 0 | 0 | 0 | 0 | 0 | 0 |

- Bit 7 **FlushBuffer:** Clear FIFO buffer  
Setting this bit to 1 will immediately clear the internal FIFO buffer's read and write pointers, and the BufferOvfl bit in the Error register. Reading this bit always returns 0.
- Bit 6~0 **FIFOLevel[6:0]:** Indication for the number of bytes stored in the FIFO buffer  
Writing data to the FIFOData register increments the FIFOLevel value and reading data from the FIFOData register decrements the FIFOLevel value.



**• WaterLevel Register**

This register defines the level of FIFO buffer for overflow and empty warning.

| Address | Bit         | 7        | 6 | 5               | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|----------|---|-----------------|---|---|---|---|---|
| 0Bh     | Name        | Reserved |   | WaterLevel[5:0] |   |   |   |   |   |
|         | Type        | —        |   | R/W             |   |   |   |   |   |
|         | Reset Value | 0        | 0 | 0               | 0 | 1 | 0 | 0 | 0 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5~0 **WaterLevel[5:0]:** Define the level of FIFO buffer for overflow and underflow warning

If the remaining space in the FIFO buffer is less than or equal to the value defined by WaterLevel[5:0], the HiAlert bit in the Status1 register will be set high.

If the used space in the FIFO buffer is less than or equal to the value defined by WaterLevel[5:0], the LoAlert bit in the Status1 register will be set high.

**• Control Register**

Various control bits.

| Address | Bit         | 7        | 6         | 5        | 4 | 3 | 2               | 1 | 0 |
|---------|-------------|----------|-----------|----------|---|---|-----------------|---|---|
| 0Ch     | Name        | TStopNow | TStartNow | Reserved |   |   | RxLastBits[2:0] |   |   |
|         | Type        | W        | W         | —        |   |   | R               |   |   |
|         | Reset Value | 0        | 0         | 0        | 1 | 0 | 0               | 0 | 0 |

Bit 7 **TStopNow:** Timer immediate stop control

Setting this bit to 1 stops the timer immediately. Reading this bit always returns 0.

Bit 6 **TStartNow:** Timer immediate start control

Setting this bit to 1 starts the timer immediately. Reading this bit always returns 0.

Bit 5~3 **Reserved:** Reserved bits

Bit 2~0 **RxLastBits[2:0]:** Indication for the number of significant bits of last received byte

If this field value is 000b, it means the entire byte is valid.

**• BitFraming Register**

Adjustment for the bit-oriented frames.

| Address | Bit         | 7         | 6            | 5 | 4 | 3        | 2               | 1 | 0 |
|---------|-------------|-----------|--------------|---|---|----------|-----------------|---|---|
| 0Dh     | Name        | StartSend | RxAlign[2:0] |   |   | Reserved | TxLastBits[2:0] |   |   |
|         | Type        | W         | R/W          |   |   | —        | R/W             |   |   |
|         | Reset Value | 0         | 0            | 0 | 0 | 0        | 0               | 0 | 0 |

Bit 7 **StartSend:** Data transmission start control

Setting this bit to 1 activates the data transmission. This bit is valid only for the Transceive command execution.

Bit 6~4 **RxAlign[2:0]:** Define the bit position for the first bit received to be stored in the FIFO buffer

000: LSB of the received data is stored at Bit0, the second received bit is stored at Bit1, and so on.

001: LSB of the received data is stored at Bit1, the second received bit is stored at Bit2, and so on.

.....

111: LSB of the received data is stored at Bit7, the second received bit is stored at Bit0 of the next byte, and so on.

This bit field is set for bit-oriented frame reception and is only used for the bitwise anti-collision at 106kbit/s. For all other modes this bit field is set to "000".

Bit 3 **Reserved:** Reserved bit

Bit 2~0 **TxLastBits[2:0]:** Define the number of bits for the last byte to be transmitted

This bit field is set for bit-oriented frame transmission. If this bit field is "000", it means all bits of the last byte will be transmitted.

**• Coll Register**

This register defines the first bit collision detected on the RF interface.

| Address | Bit         | 7               | 6        | 5               | 4            | 3 | 2 | 1 | 0 |
|---------|-------------|-----------------|----------|-----------------|--------------|---|---|---|---|
| 0Eh     | Name        | ValuesAfterColl | Reserved | CollPosNotValid | CollPos[4:0] |   |   |   |   |
|         | Type        | R/W             | —        | R               | R            |   |   |   |   |
|         | Reset Value | 1               | 0        | 1               | 0            | 0 | 0 | 0 | 0 |

- Bit 7 **ValuesAfterColl:**  
If this bit is set to 0, all data bits will be cleared after a collision. It is only used in bitwise anti-collision at 106kbit/s, otherwise it is set to 1.
- Bit 6 **Reserved:** Reserved bit
- Bit 5 **CollPosNotValid:**  
If this bit is set to 1, it indicates that no collision is detected or the collision bit position is outside the rang defined by CollPos[4:0].
- Bit 4~0 **CollPos[4:0]:** Position of the first collision bit detected in the received frame (only data bits are interpreted)  
00000: Indicates a bit collision at the 32nd bit  
00001: Indicates a bit collision at the 1st bit  
.....  
01000: Indicates a bit collision at the 8th bit  
.....  
These bits are only interpreted when the CollPosNotValid bit is 0.

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**• Mode Register**

This register defines the general mode settings for transmission and reception.

| Address | Bit         | 7        | 6        | 5        | 4        | 3       | 2        | 1              | 0 |
|---------|-------------|----------|----------|----------|----------|---------|----------|----------------|---|
| 11h     | Name        | MSBFirst | Reserved | TxWaitRF | Reserved | PolMFin | Reserved | CRCPreSet[1:0] |   |
|         | Type        | R/W      | —        | R/W      | —        | R/W     | —        | R/W            |   |
|         | Reset Value | 0        | 0        | 1        | 1        | 1       | 1        | 0              | 1 |

- Bit 7 **MSBFirst:**  
When this bit is set to 1, the CRC coprocessor will calculate the CRC with the MSB first. The calculation result is stored in the CRCResult\_H and CRCResult\_L registers. During RF communication, this bit is ignored.
- Bit 6 **Reserved:** Reserved bit
- Bit 5 **TxWaitRF:**  
If this bit is set to 1, the transmitter is started when the RF field presents.
- Bit 4 **Reserved:** Reserved bit
- Bit 3 **PolMFin:** Define the MFIN pin polarity  
0: MFIN pin is low active  
1: MFIN pin is high active  
Note that the internal encoded envelop signal is low active, changing this bit will generate an MfinActIRq event.
- Bit 2 **Reserved:** Reserved bit
- Bit 1~0 **CRCPreSet[1:0]:** Define the preset value for the CRC coprocessor to execute CalcCRC command  
00: 0000h  
01: 6363h  
10: A671h  
11: FFFFh  
During any communication, the preset value is selected automatically according to the bit definition in the RxMode and TxMode registers.

**• TxMode Register**

This register defines the data rate during transmission.

| Address | Bit         | 7       | 6            | 5 | 4 | 3      | 2        | 1              | 0 |
|---------|-------------|---------|--------------|---|---|--------|----------|----------------|---|
| 12h     | Name        | TxCRCEn | TxSpeed[2:0] |   |   | InvMod | Reserved | TxFraming[1:0] |   |
|         | Type        | R/W     | D            |   |   | R/W    | —        | D              |   |
|         | Reset Value | 0       | 0            | 0 | 0 | 0      | 0        | 0              | 0 |

Bit 7 **TxCRCEn:**  
Setting this bit to 1 enables the CRC generation during the data transmission.

Bit 6~4 **TxSpeed[2:0]:** Define the bit rate during the data transmission  
 000: 106kbit/s  
 001: 212kbit/s  
 010: 424kbit/s  
 011: 848kbit/s  
 100~111: Reserved

This chip supports transmission rates up to 848kbit/s.

Bit 3 **InvMod:**  
If this bit is set to 1, the inverting value of the modulated data is sent.

Bit 2 **Reserved:** Reserved bit

Bit 1~0 **TxFraming[1:0]:** Define the transmission data structure  
 00: ISO/IEC 14443 A / Crypto\_M  
 01~10: Reserved  
 11: ISO/IEC 14443 B

**• RxMode Register**

This register defines the data rate during the data reception.

| Address | Bit         | 7       | 6            | 5 | 4 | 3       | 2          | 1         | 0 |
|---------|-------------|---------|--------------|---|---|---------|------------|-----------|---|
| 13h     | Name        | RxCRCEn | RxSpeed[2:0] |   |   | RxNoErr | RxMultiple | RxFraming |   |
|         | Type        | R/W     | D            |   |   | R/W     | R/W        | D         |   |
|         | Reset Value | 0       | 0            | 0 | 0 | 0       | 0          | 0         | 0 |

Bit 7 **RxCRCEn:**  
Setting this bit to 1 enables the CRC generation during the data reception.

Bit 6~4 **RxSpeed[2:0]:** Define the bit rate during the data reception  
 000: 106kbit/s  
 001: 212kbit/s  
 010: 424kbit/s  
 011: 848kbit/s  
 100~111: Reserved

This chip supports transmission rates up to 848kbit/s.

Bit 3 **RxNoErr:**  
If this bit is set to 1, an invalid data stream received (less than 4 bits) will be ignored and the receiver remains active.

Bit 2 **RxMultiple:**  
 0: Receiver stops after receiving one data frame  
 1: Receiver continuously receives multiple data frames  
 After this bit is set to 1, the Receive and Transceive commands will not terminate automatically. Continuous reception can be stopped by writing any command code to the Command register (except Receive command) or by clearing the bit by the host.

Bit 1~0 **RxFraming[1:0]:** Define the data structure to be received  
 00: ISO/IEC 14443 A / Crypto\_M  
 01~10: Reserved  
 11: ISO/IEC 14443 B

**• TxControl Register**

This register controls the logic status of the antenna driver pins TX1 and TX2.

| Address | Bit         | 7        | 6         | 5        | 4 | 3    | 2        | 1      | 0 |
|---------|-------------|----------|-----------|----------|---|------|----------|--------|---|
| 14h     | Name        | Reserved | InvTxRFOn | Reserved |   | TxCW | Reserved | TxRFEn |   |
|         | Type        | —        | R/W       | —        |   | R/W  | —        | R/W    |   |
|         | Reset Value | 1        | 0         | 0        | 0 | 0    | 0        | 0      | 0 |

Bit 7 **Reserved:** Reserved bit

Bit 6 **InvTxRFOn:**

If this bit is set to 1, the carrier on the TX pin is inverted when driver TX is enabled.

Bit 5~4 **Reserved:** Reserved bits

Bit 3 **TxCW:**

0: Do not output the unmodulated 13.56MHz energy carrier

1: Continuously output the unmodulated 13.56MHz energy carrier

Bit 2 **Reserved:** Reserved bit

Bit 1~0 **TxRFEn:**

00: Do not output the modulated 13.56MHz energy carrier

01: Continuously output the modulated 13.56MHz energy carrier on TX1

10: Continuously output the modulated 13.56MHz energy carrier on TX2

11: Continuously output the modulated 13.56MHz energy carrier on both TX1 and TX2

**• TxASK Register**

This register controls the transmitting modulation.

| Address | Bit         | 7        | 6           | 5        | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|----------|-------------|----------|---|---|---|---|---|
| 15h     | Name        | Reserved | Force100ASK | Reserved |   |   |   |   |   |
|         | Type        | —        | R/W         | —        |   |   |   |   |   |
|         | Reset Value | 0        | 1           | 0        | 0 | 0 | 0 | 0 | 0 |

Bit 7 **Reserved:** Reserved bit

Bit 6 **Force100ASK:**

Setting this bit to 1 will enforce a 100% ASK modulation independent of the ModGsP register setting.

Bit 5~0 **Reserved:** Reserved bits

**• TxSel Register**

This register selects the signal source for the antenna drivers.

| Address | Bit         | 7        | 6 | 5              | 4 | 3             | 2 | 1 | 0 |
|---------|-------------|----------|---|----------------|---|---------------|---|---|---|
| 16h     | Name        | Reserved |   | DriverSel[1:0] |   | MFOutSel[3:0] |   |   |   |
|         | Type        | —        |   | R/W            |   | R/W           |   |   |   |
|         | Reset Value | 0        | 0 | 0              | 1 | 0             | 0 | 0 | 0 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5~4 **DriverSel[1:0]:** Select the input signal of drivers TX1 and TX2

00: 3-state – If selected, the drivers can only be in 3-state mode in the software power-down mode

01: Modulation signal (envelope) from the internal encoder, Miller encoded

10: Modulation signal (envelope) from the MFIN pin

11: High level – depends on the InvTxRFOn bit setting

Bit 3~0 **MFOutSel[3:0]:** Define the MFOUT output signal

0000: 3-state

0001: Low level

0010: High level

0011: Signal defined by TstBusBitSel[2:0]

0100: TX tata stream with Miller encoding

0101: TX tata stream without Miller encoding

- 0110: RX data stream without Manchester decoding and with subcarrier
- 0111: RX data stream with Manchester decoding (“00/01” converted to 0, “10” converted to 1)
- 1000: RX data stream without Manchester decoding and without subcarrier
- 1001~1111: Reserved

#### • RxSel Register

This registers controls the internal receiver settings.

| Address | Bit         | 7            | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|---------|-------------|--------------|---|---|-------------|---|---|---|---|
| 17h     | Name        | UARTSel[1:0] |   |   | RxWait[5:0] |   |   |   |   |
|         | Type        | R/W          |   |   | R/W         |   |   |   |   |
|         | Reset Value | 1            | 0 | 0 | 0           | 1 | 0 | 0 | 0 |

Bit 7~6 **UARTSel[1:0]**: Select contactless UART input  
 00: Low level  
 01: Manchester signal with subcarrier from the MFIN pin  
 10: Modulated signal from the internal analog block  
 11: NRZ coding without subcarrier from the MFIN pin, only valid for transfer speed above 106kbit/s

Bit 5~0 **RxWait[5:0]**: Define the delay time before activating the receiver  
 After data transmission, the activation of the receiver has a delay of RxWait[5:0]×ETU, where ETU is defined by the RxWaitEtu bit in the Special register. During this frame guard time, any signal on the RX pin will be ignored. This parameter is ignored by the Receive command and is used by all other commnads. The counter starts immediately after the external RF field is switched on.

#### • Demod Register

This register defines the demodulation settings.

| Address | Bit         | 7          | 6 | 5     | 4            | 3        | 2 | 1 | 0 |
|---------|-------------|------------|---|-------|--------------|----------|---|---|---|
| 19h     | Name        | AddIQ[1:0] |   | FixIQ | TPrescalEven | Reserved |   |   |   |
|         | Type        | R/W        |   | R/W   | R/W          | —        |   |   |   |
|         | Reset Value | 0          | 1 | 0     | 0            | 1        | 1 | 0 | 1 |

Bit 7~6 **AddIQ[1:0]**: Define the use of I and Q channels during reception  
 00: Select a stronger signal channel  
 01: Select a stronger signal channel and freeze the selected channel during communication  
 10~11: Reserved

Note that the FixIQ bit must be set to 0 to enable the above settings.

Bit 5 **FixIQ**:  
 When this bit is set to 1, if AddIQ[1:0] is set to “x0”, the reception is fixed to I channel; if AddIQ[1:0] is set to “x1”, the reception is fixed to Q channel.

Bit 4 **TPrescalEven**: Select the formula to calculate the timer frequency  
 0:  $f_{\text{Timer}} = 13.56\text{MHz} / (2 \times \text{TPrescaler} + 1)$   
 1:  $f_{\text{Timer}} = 13.56\text{MHz} / (2 \times \text{TPrescaler} + 2)$

By default, the formula of option 0 is used for calculation. Refer to the Tmode and TPrescaler registers for TPrescaler definition.

Bit 3~0 **Reserved**: Reserved bits

**• MfTx Register**

This register defines the transmission waiting time.

| Address | Bit         | 7        | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|---------|-------------|----------|---|---|-------------|---|---|---|---|
| 1Ch     | Name        | Reserved |   |   | TxWait[4:0] |   |   |   |   |
|         | Type        | —        |   |   | R/W         |   |   |   |   |
|         | Reset Value | 0        | 1 | 1 | 0           | 0 | 0 | 1 | 0 |

Bit 7~5 **Reserved:** Reserved bits

Bit 4~0 **TxWait[4:0]:** Define the transmission waiting time

By default, waiting time=(TxWait[4:0])×ETU, where ETU is defined by the TxWaitEtu bit in the Special register.

**• MfRx Register**

| Address | Bit         | 7        | 6 | 5 | 4             | 3        | 2 | 1          | 0 |
|---------|-------------|----------|---|---|---------------|----------|---|------------|---|
| 1Dh     | Name        | Reserved |   |   | ParityDisable | Reserved |   | RxHPF[1:0] |   |
|         | Type        | —        |   |   | R/W           | —        |   | R/W        |   |
|         | Reset Value | 0        | 0 | 0 | 0             | 0        | 0 | 0          | 0 |

Bit 7~5 **Reserved:** Reserved bits

Bit 4 **ParityDisable:** Transmission and reception parity function on/off control

0: On

1: Off

When this bit is set to 1, the parity bit generation for transmission and parity check for reception are turned off, and the received parity bit is processed as data bit.

Bit 3~2 **Reserved:** Reserved bits

Bit 1~0 **RxHPF[1:0]:** Select high-pass bandwidth

00: 72kHz

01: 100kHz

10: 150kHz

11: 300kHz

Set to “11” at 106kbit/s, “10” at 212kbit/s, “01” at 424kbit/s and “00” at 848kbit/s.

**• TypeB Register**

This register configures the ISO/IEC 14443 B functions.

| Address | Bit         | 7        | 6        | 5        | 4           | 3       | 2       | 1          | 0 |
|---------|-------------|----------|----------|----------|-------------|---------|---------|------------|---|
| 1Eh     | Name        | RxSOFReq | RxEOFReq | Reserved | EOFSOFWidth | NoTxSOF | NoTxEOF | TxEGT[1:0] |   |
|         | Type        | R/W      | R/W      | —        | R/W         | R/W     | R/W     | R/W        |   |
|         | Reset Value | 0        | 0        | 0        | 0           | 0       | 0       | 0          | 0 |

Bit 7 **RxSOFReq:**

0: Receive data streams with or without SOF; remove SOF and do not write them to FIFO

1: Require SOF; ignore data streams without SOF

Bit 6 **RxEOFReq:**

0: Receive data streams with or without EOF; remove EOF and do not write them to FIFO

1: Require EOF; data stream without EOF generates a protocol error

Bit 5 **Reserved:** Reserved bit

Bit 4 **EOFSOFWidth:**

0: Define the minimum length of SOF and EOF in IOS/IEC 14443 B

1: Define the maximum length of SOF and EOF in IOS/IEC 14443 B

Bit 3 **NoTxSOF:**

If this bit is set to 1, the SOF will be omitted from the transmitted framing.

Bit 2 **NoTxEOF:**

If this bit is set to 1, the EOF will be omitted from the transmitted framing.

Bit 1~0     **TxEg[1:0]**: Define EGT(Extra Guard Time) length  
                  00: No EGT  
                  01: 1 bit  
                  10: 2 bits  
                  11: 3 bits

#### • SerialSpeed Register

This register selects the UART data rate. Refer to the UART Interface section for detailed configuration.

| Address | Bit         | 7          | 6 | 5 | 4          | 3 | 2 | 1 | 0 |  |
|---------|-------------|------------|---|---|------------|---|---|---|---|--|
| 1Fh     | Name        | BR_T0[2:0] |   |   | BR_T1[4:0] |   |   |   |   |  |
|         | Type        | R/W        |   |   | R/W        |   |   |   |   |  |
|         | Reset Value | 1          | 1 | 1 | 0          | 1 | 0 | 1 | 1 |  |

Bit 7~5     **BR\_T0[2:0]**: Adjust transmission data rate

Bit 4~0     **BR\_T1[4:0]**: Adjust transmission data rate

#### Page 2

#### • CRCResult\_H Register

This register shows the high byte value of the CRC calculation result.

| Address | Bit         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------------|---|---|---|---|---|---|---|
| 21h     | Name        | CRCResultMSB[7:0] |   |   |   |   |   |   |   |
|         | Type        | R                 |   |   |   |   |   |   |   |
|         | Reset Value | 1                 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bit 7~0     **CRCResultMSB[7:0]**: CRC calculation result high byte value  
 It is valid only when the CRCReady bit in the Status1 register is set high.

#### • CRCResult\_L Register

This register shows the low byte value of the CRC calculation result.

| Address | Bit         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------------|---|---|---|---|---|---|---|
| 22h     | Name        | CRCResultLSB[7:0] |   |   |   |   |   |   |   |
|         | Type        | R                 |   |   |   |   |   |   |   |
|         | Reset Value | 1                 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bit 7~0     **CRCResultLSB[7:0]**: CRC calculation result low byte value  
 It is valid only when the CRCReady bit in the Status1 register is set high.

#### • ModWidth Register

This register sets the modulation width.

| Address | Bit         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---------------|---|---|---|---|---|---|---|
| 24h     | Name        | ModWidth[7:0] |   |   |   |   |   |   |   |
|         | Type        | R/W           |   |   |   |   |   |   |   |
|         | Reset Value | 0             | 0 | 1 | 0 | 0 | 1 | 1 | 0 |

Bit 7~0     **ModWidth[7:0]**: Define the Miller modulation width to be (ModWidth+1) times the carrier frequency  
 The maximum value is half a bit cycle.

**• RFCfg Register**

This register configures the receiver gain.

| Address | Bit         | 7        | 6           | 5 | 4 | 3 | 2        | 1 | 0 |  |
|---------|-------------|----------|-------------|---|---|---|----------|---|---|--|
| 26h     | Name        | Reserved | RxGain[3:0] |   |   |   | Reserved |   |   |  |
|         | Type        | —        | R/W         |   |   |   | —        |   |   |  |
|         | Reset Value | 0        | 1           | 0 | 0 | 1 | 0        | 0 | 0 |  |

Bit 7 **Reserved:** Reserved bit

Bit 6~3 **RxGain[3:0]:** Define the receiver signal voltage gain factor

|      |      |      |      |
|------|------|------|------|
| 0000 | 18dB | 1000 | 34dB |
| 0001 | 20dB | 1001 | 36dB |
| 0010 | 22dB | 1010 | 38dB |
| 0011 | 24dB | 1011 | 40dB |
| 0100 | 26dB | 1100 | 42dB |
| 0101 | 28dB | 1101 | 44dB |
| 0110 | 30dB | 1110 | 46dB |
| 0111 | 32dB | 1111 | 48dB |

Bit 2~0 **Reserved:** Reserved bits

**• GsN Register**

This register defines the conductance value when antenna drivers TX1 and TX2 are turned on and used as N drivers.

| Address | Bit         | 7          | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
|---------|-------------|------------|---|---|---|-------------|---|---|---|
| 27h     | Name        | CWGsN[3:0] |   |   |   | ModGsN[3:0] |   |   |   |
|         | Type        | R/W        |   |   |   | R/W         |   |   |   |
|         | Reset Value | 1          | 0 | 0 | 0 | 1           | 0 | 0 | 0 |

Bit 7~4 **CWG<sub>s</sub>N[3:0]:** Define the conductance value of N driver when it outputs a CW signal  
 The conductance value is binary-weighted. The unit conductance value of the N driver is 1/160 S.  
 By setting this register, the conductance value of the N driver during the non-modulation period is:  
 $CWG_{sN}[3:0] \times (1/160) \text{ S}$ .

This field setting is valid only when the drivers TX1 and TX2 are turned on.

The highest bit is forced to 1 in the software power-down mode.

Bit 3~0 **ModGs<sub>s</sub>N[3:0]:** Define the conductance value of N driver when it outputs a MOD signal  
 The conductance value is binary-weighted. The unit conductance value of the N driver is 1/160 S.  
 By setting this register, the conductance value of the N driver during the modulation period is:  
 $ModGs_{sN}[3:0] \times (1/160) \text{ S}$ .

This field setting is valid only when the drivers TX1 and TX2 are turned on.

The highest bit is forced to 1 in the software power-down mode.

**• CWGsP Register**

This register defines the conductance value of the P driver during the non-modulation period.

| Address | Bit         | 7        | 6 | 5          | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|----------|---|------------|---|---|---|---|---|
| 28h     | Name        | Reserved |   | CWGsP[5:0] |   |   |   |   |   |
|         | Type        | —        |   | R/W        |   |   |   |   |   |
|         | Reset Value | 0        | 0 | 1          | 0 | 0 | 0 | 0 | 0 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5~0 **CWG<sub>s</sub>P[5:0]:** Define the conductance value of P driver when it outputs a CW signal  
 The conductance value is binary-weighted. The unit conductance value of the P driver is 1/640 S.  
 By setting this register, the conductance value of the P driver during the non-modulation period is:  
 $CWG_{sP}[5:0] \times (1/640) \text{ S}$ .

The highest bit is forced to 1 in the software power-down mode.



**• ModGsP Register**

This register defines the conductance value of the P driver during the modulation period.

| Address | Bit         | 7        | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|---------|-------------|----------|---|---|-------------|---|---|---|---|
| 29h     | Name        | Reserved |   |   | ModGsP[5:0] |   |   |   |   |
|         | Type        | —        |   |   | R/W         |   |   |   |   |
|         | Reset Value | 0        | 0 | 1 | 0           | 0 | 0 | 0 | 0 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5~0 **ModGsP[5:0]:** Define the conductance value of P driver when it outputs a MOD signal  
 The conductance value is binary-weighted. The unit conductance value of the P driver is 1/640 S.  
 By setting this register, the conductance value of the P driver during the modulation period is:  
 ModGsP[5:0]×(1/640) S.

Even if the Force100ASK bit in the TxASK register is set to 1, it has no effect on the ModGsP[5:0] value.

The highest bit is forced to 1 in the software power-down mode.

**• TMode Register**

This register defines the timer settings.

| Address | Bit         | 7     | 6        | 5 | 4            | 3                  | 2 | 1 | 0 |
|---------|-------------|-------|----------|---|--------------|--------------------|---|---|---|
| 2Ah     | Name        | TAuto | Reserved |   | TAutoRestart | TPrescaler_Hi[3:0] |   |   |   |
|         | Type        | R/W   | R/W      |   | R/W          | R/W                |   |   |   |
|         | Reset Value | 1     | 0        | 0 | 0            | 1                  | 0 | 0 | 0 |

Bit 7 **TAuto:** Timer auto start control

0: Timer is not affected by this control bit

1: Timer starts automatically at the end of data transmission at all communication speeds

After this bit is set to 1, if the RxMultiple bit in the RxMode register is 0, the timer will stop running immediately after receiving the 5th bit (1 start bit and 4 data bits); if the RxMultiple bit is 1 the timer will not stop, in which case the timer can only be stopped by setting the TstopNow bit in the Control register to 1.

Bit 6~5 **Reserved:** Reserved bits

Bit 4 **TAutoRestart:**

0: Timer decrements to 0 and the TimerIRQ flag in the ComIrq register is set to 1

1: Timer automatically restarts down-counting from the 16-bit timer reload value

Bit 3~0 **TPrescaler\_Hi[3:0]:** TPrescaler value higher 4 bits

Refer to the TPrescaler register.

**• TPrescaler Register**

This register defines the timer settings.

| Address | Bit         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------------|---|---|---|---|---|---|---|
| 2Bh     | Name        | TPrescaler_Lo[7:0] |   |   |   |   |   |   |   |
|         | Type        | R/W                |   |   |   |   |   |   |   |
|         | Reset Value | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **TPrescaler\_Lo[7:0]:** TPrescaler value lower 8 bits

If the TPrescalerEven bit in the Demod register is 0:  $f_{\text{Timer}} = 13.56\text{MHz} / (2 \times \text{TPrescaler} + 1)$

If the TPrescalerEven bit in the Demod register is 1:  $f_{\text{Timer}} = 13.56\text{MHz} / (2 \times \text{TPrescaler} + 2)$

$\text{TPrescaler} = [\text{TPrescaler\_Hi} : \text{TPrescaler\_Lo}]$

**• TReload\_H Register**

This register defines the high byte of the 16-bit timer reload value.

| Address | Bit         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------------|---|---|---|---|---|---|---|
| 2Ch     | Name        | TReloadVal_Hi[7:0] |   |   |   |   |   |   |   |
|         | Type        | R/W                |   |   |   |   |   |   |   |
|         | Reset Value | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **TReloadVal\_Hi[7:0]**: Timer 16-bit reload value higher 8 bits  
 When a start event occurs, the 16-bit reload value is loaded into the timer. Changing this register will only affect the timer on the next start event.

**• TReload\_L Register**

This register defines the low byte of the 16-bit timer reload value.

| Address | Bit         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------------|---|---|---|---|---|---|---|
| 2Dh     | Name        | TReloadVal_Lo[7:0] |   |   |   |   |   |   |   |
|         | Type        | R/W                |   |   |   |   |   |   |   |
|         | Reset Value | 0                  | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Bit 7~0 **TReloadVal\_Lo[7:0]** : Timer 16-bit reload value lower 8 bits  
 When a start event occurs, the 16-bit reload value is loaded into the timer. Changing this register will only affect the timer on the next start event.

**• TCounterVal\_H Register**

This register shows the high byte of the timer current value.

| Address | Bit         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---------------------|---|---|---|---|---|---|---|
| 2Eh     | Name        | TCounterVal_Hi[7:0] |   |   |   |   |   |   |   |
|         | Type        | R                   |   |   |   |   |   |   |   |
|         | Reset Value | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **TCounterVal\_Hi[7:0]**: Timer current value higher 8 bits

**• TCounterVal\_L Register**

This register shows the low byte of the timer current value.

| Address | Bit         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---------------------|---|---|---|---|---|---|---|
| 2Fh     | Name        | TCounterVal_Lo[7:0] |   |   |   |   |   |   |   |
|         | Type        | R                   |   |   |   |   |   |   |   |
|         | Reset Value | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **TCounterVal\_Lo[7:0]**: Timer current value lower 8 bits

**Page 3**
**• TestPinEn Register**

| Address | Bit         | 7        | 6              | 5 | 4 | 3 | 2 | 1 | 0        |
|---------|-------------|----------|----------------|---|---|---|---|---|----------|
| 33h     | Name        | Reserved | TestPinEn[5:0] |   |   |   |   |   | Reserved |
|         | Type        | R/W      | R/W            |   |   |   |   |   | —        |
|         | Reset Value | 1        | 0              | 0 | 0 | 0 | 0 | 0 | 0        |

Bit 7 **Reserved**: Reserved bit

Bit 6~1 **TestPinEn[5:0]**: Enable the output driver on one of the data pins D6~D1 that output the test signal  
 For example, TestPinEn0=1 enables the D1 pin output; TestPinEn5=1 enables the D6 pin output.  
 Note that if the SPI interface is used, only D1~D4 pins are available for output.

Bit 0 **Reserved**: Reserved bit

**• TestPinValue Register**

| Address | Bit         | 7     | 6                 | 5 | 4 | 3 | 2 | 1 | 0        |
|---------|-------------|-------|-------------------|---|---|---|---|---|----------|
| 34h     | Name        | UseIO | TestPinValue[5:0] |   |   |   |   |   | Reserved |
|         | Type        | R/W   | R/W               |   |   |   |   |   | —        |
|         | Reset Value | 0     | 0                 | 0 | 0 | 0 | 0 | 0 | 0        |

Bit 7 **UseIO:**  
Setting this bit to 1 enables the I/O functionality for the test port when one of the interfaces is used. The input/output behavior is defined by the TestPinEn[5:0] setting in the TestPinEn register.

Bit 6~1 **TestPinValue[5:0]:** Define the value of the test port when it is used as I/O port  
Each output must be enabled using the corresponding bit of TestPinEn[5:0] in the TestPinEn register. If the UseIO bit is set to 1, reading this field returns the D6~D1 pin values. If the UseIO bit is set to 0, reading this field returns the value of this field.

Bit 0 **Reserved:** Reserved bit

**• PageSel Register**

| Address | Bit         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------|---|---|---|---|---|---|---|
| 37h     | Name        | PageSel[7:0] |   |   |   |   |   |   |   |
|         | Type        | R/W          |   |   |   |   |   |   |   |
|         | Reset Value | 0            | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

Bit 7~0 **PageSel[7:0]:** Private register switch control  
0x5E: Enable access to Page 4  
0xAE: Enable access to Page 5  
0x5A: Enable access to Page 6

To configure the registers in pages 4~6, this register should first be configured to the correct switch value before executing any operations to the registers in the corresponding page.

**Private Register Description**
**Page 4**

PageSel[7:0] must first be set to 0x5E so as to configure the registers in page 4.

**• TestSel Register**

| Address | Bit         | 7        | 6 | 5 | 4 | 3 | 2 | 1                 | 0 |  |
|---------|-------------|----------|---|---|---|---|---|-------------------|---|--|
| 31h     | Name        | Reserved |   |   |   |   |   | TstBusBitSel[2:0] |   |  |
|         | Type        | R/W      |   |   |   |   |   | R/W               |   |  |
|         | Reset Value | 0        | 0 | 0 | 0 | 0 | 0 | 0                 | 0 |  |

Bit 7~3 **Reserved:** Reserved bits

Bit 6~3 **TstBusBitSel[2:0]:** Select an internal test signal to output on the MFOUT pin  
000: rx\_start  
001: bit\_sync  
010: ErrIrq  
011: ErrIrq + TimeoutIrq  
100: clk32k  
101: clk27m  
110: iq\_sel\_flag  
111: Undefined

**• DataPullID Register**

| Address | Bit         | 7           | 6        | 5            | 4                | 3 | 2 | 1 | 0        |
|---------|-------------|-------------|----------|--------------|------------------|---|---|---|----------|
| 32h     | Name        | PullUpManEn | Reserved | MfinPullUp_R | PDataPullUp[4:1] |   |   |   | Reserved |
|         | Type        | R/W         | R        | R/W          | R/W              |   |   |   | R/W      |
|         | Reset Value | 0           | 0        | 0            | 0                | 0 | 0 | 0 | 0        |

- Bit 7 **PullUpManEn**: Enable the manual control of pull-up resistor for pins MFIN and D7~D1  
 0: Disable  
 1: Enable
- Bit 6 **Reserved**: Reserved bit
- Bit 5 **MfinPullUp\_R**: MFIN pull-up resistor control (when PullUpManEn=1), low active
- Bit 4~1 **PDataPullUp[4:0]**: D7~D1 pull-up resistor control (when PullUpManEn=1), low active  
 PDataPullUp[4] controls D7, PDataPullUp[3] controls D6, PDataPullUp[2] controls D5 and PDataPullUp[1] controls D4~D1.
- Bit 0 **Reserved**: Reserved bit

**• RxAlgorithm0 Register**

| Address | Bit         | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0        |          |
|---------|-------------|----------|---|---|---|---|---|---|----------|----------|
| 33h     | Name        | Reserved |   |   |   |   |   |   | BSAdjCnt | BSAdjDis |
|         | Type        | R        |   |   |   |   |   |   | R/W      | R/W      |
|         | Reset Value | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 1        |          |

- Bit 7~2 **Reserved**: Reserved bits
- Bit 1 **BSAdjCnt**: Select the number of bit cycles used for bit synchronization of the OOK demodulation algorithm  
 0: 4 bit cycles  
 1: 8 bit cycles
- Bit 0 **BSAdjDis**: Control the bit synchronization of the OOK demodulation algorithm  
 0: Enable  
 1: Disable

**• AGCCfg0 Register**

| Address | Bit         | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0                 |
|---------|-------------|----------|---|---|---|---|---|---|-------------------|
| 34h     | Name        | Reserved |   |   |   |   |   |   | First_Gain_Idx[2] |
|         | Type        | R        |   |   |   |   |   |   | R/W               |
|         | Reset Value | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0                 |

- Bit 7~1 **Reserved**: Reserved bits
- Bit 0 **First\_Gain\_Idx[2]**: AGC (Automatic Gain Control) first step gain control bit 2  
 First\_Gain\_Idx[1:0] is located in the AGCCfg1 register.

**• AGCCfg1 Register**

| Address | Bit         | 7          | 6 | 5                   | 4 | 3                   | 2 | 1              | 0 |
|---------|-------------|------------|---|---------------------|---|---------------------|---|----------------|---|
| 35h     | Name        | EXT_AGC_en |   | Full_Scale_Num[1:0] |   | First_Gain_Idx[1:0] |   | Gain_Step[1:0] |   |
|         | Type        | R/W        |   | RR/W                |   | RR/W                |   | RR/W           |   |
|         | Reset Value | 1          | 1 | 1                   | 0 | 1                   | 1 | 0              | 0 |

- Bit 7~6 **EXT\_AGC\_en**: AGC function control  
 00: Disable AGC  
 01: Enable – signal stage  
 10: Enable – RxWait stage, signal stage  
 11: Enable – RxWait stage, post-RxWait signal stage, signal stage
- Bit 5~4 **Full\_Scale\_Num[1:0]**: Define the number of saturation points for gain reduction in the automatic gain mode

Bit 3~2 **First\_Gain\_Indx[1:0]**: AGC first step gain control bit 1~0

First\_Gain\_Indx[2] is located in the AGCCfg0 register.

First\_Gain\_Indx[2:0]=

- 000: 48dB
- 001: 44dB
- 010: 40dB
- 011: 36dB
- 100: 32dB
- 101: 42dB
- 110: 38dB
- 111: 34dB

Bit 1~0 **Gain\_Step[1:0]**: Select the gain decrement in the automatic gain mode

- 00: 2dB
- 01: 4dB
- 10: 6dB
- 11: Reserved

#### • RxAlgorithm1 Register

| Address | Bit         | 7       | 6        | 5          | 4 | 3        | 2     | 1        | 0 |
|---------|-------------|---------|----------|------------|---|----------|-------|----------|---|
| 36h     | Name        | IQFixEn | ManRxLPF | RxLPF[1:0] |   | EnRx2Bit | DC_bp | Reserved |   |
|         | Type        | RW      | RW       | RW         |   | RW       | RW    | RW       |   |
|         | Reset Value | 0       | 0        | 0          | 0 | 0        | 0     | 0        | 0 |

Bit 7 **IQFixEn**: Control the IQ channel manual selection in the Demod register

- 0: Disable
- 1: Enable

Bit 6 **ManRxLPF**: Enable the low-pass bandwidth manual selection

- 0: Automatic selection
- 1: Manual selection

Bit 5~4 **RxLPF[1:0]**: Low-pass bandwidth selection

- 00: 1.6MHz
- 01: 1.8MHz
- 10: 2.0MHz
- 11: 2.3MHz

Set to “00” at 106kbit/s, set to “01” at 212kbit/s, set to “10” at 424kbit/s and set to “11” at 848kbit/s.

Bit 3 **EnRx2Bit**: Improve noise immunity by algorithm

- 0: Enable – In Type A, the first 2 significant data bits are used to improve noise immunity, so data shorter than 2 bits cannot be received
- 1: Disable

Bit 2 **DC\_bp**: Demodulation algorithm DC removal control

- 0: Enable DC removal
- 1: Disable DC removal

Bit 1~0 **Reserved**: Reserved bits

#### • RxAlgorithm2 Register

| Address | Bit         | 7             | 6 | 5 | 4 | 3              | 2 | 1 | 0 |
|---------|-------------|---------------|---|---|---|----------------|---|---|---|
| 38h     | Name        | MinLevel[3:0] |   |   |   | CollRatio[3:0] |   |   |   |
|         | Type        | RW            |   |   |   | RW             |   |   |   |
|         | Reset Value | 0             | 1 | 1 | 0 | 1              | 0 | 1 | 1 |

Bit 7~4 **MinLevel[3:0]**: Demodulation algorithm minimum signal detection amplitude paramter 2

Bit 3~0 **CollRatio[3:0]**: Demodulation algorithm TypeA collision judgement criteria parameter

**• RxAlgorithm3 Register**

| Address | Bit         | 7        | 6            | 5 | 4 | 3                | 2 | 1 | 0 |
|---------|-------------|----------|--------------|---|---|------------------|---|---|---|
| 39h     | Name        | Reserved | TALevel[2:0] |   |   | EnergyLevel[3:0] |   |   |   |
|         | Type        | R        | RW           |   |   | RW               |   |   |   |
|         | Reset Value | 0        | 0            | 1 | 0 | 1                | 0 | 0 | 0 |

Bit 7 **Reserved:** Reserved bit

Bit 6~4 **TALevel[2:0]:** Demodulation algorithm transmission end criteria parameter 1

Bit 3~0 **EnergyLevel[3:0]:** Demodulation algorithm transmission end criteria parameter 2

**• RxCK Register**

| Address | Bit         | 7        | 6 | 5        | 4       | 3         | 2             | 1 | 0 |
|---------|-------------|----------|---|----------|---------|-----------|---------------|---|---|
| 3Ah     | Name        | Reserved |   | Reserved | TypeADT | CKDlyAuto | CKDlySel[2:0] |   |   |
|         | Type        | RW       |   | RW       | RW      | RW        | RW            |   |   |
|         | Reset Value | 0        | 0 | 0        | 0       | 1         | 0             | 0 | 0 |

Bit 7~5 **Reserved:** Reserved bits

Bit 4 **TypeADT:** TypeA wave falling time adjustment

0: The function does not take effect

1: Speed up the Type A wave falling edge

Bit 3 **CKDlyAuto:** IQ automatic phase selection

0: IQ phase is specified by CKDlySel[2:0]

1: IQ phase is automatically locked

Bit 2~0 **CKDlySel[2:0]:**

There are eight levels by setting this field from 000 to 111. It is used to select the phase angle when configuring the internal signal demodulation, which affects the card reading effect.

**• RxBand Register**

| Address | Bit         | 7        | 6 | 5            | 4 | 3 | 2            | 1 | 0 |
|---------|-------------|----------|---|--------------|---|---|--------------|---|---|
| 3Bh     | Name        | Reserved |   | MchAckH[2:0] |   |   | MchAckL[2:0] |   |   |
|         | Type        | —        |   | R/W          |   |   | R/W          |   |   |
|         | Reset Value | 0        | 0 | 1            | 0 | 0 | 1            | 0 | 1 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5~3 **MchAckH[2:0]:** Manchester encoding SOF detection, half Bit1 / Noise threshold factor

Bit 2~0 **MchAckL[2:0]:** Manchester encoding SOF detection, half Bit0 / half Bit1 threshold factor

**• LPCD Register**

| Address | Bit         | 7        | 6        | 5         | 4       | 3          | 2 | 1 | 0 |
|---------|-------------|----------|----------|-----------|---------|------------|---|---|---|
| 3Ch     | Name        | Reserved | Reserved | CLK32K_En | CalibEn | Delta[3:0] |   |   |   |
|         | Type        | R        | —        | R/W       | R/W     | R/W        |   |   |   |
|         | Reset Value | 0        | 0        | 0         | 0       | 0          | 0 | 0 | 0 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5 **CLK32K\_En:** 32kHz clock enable

0: Disable

1: Enable

Bit 4 **CalibEn:** Card detection calibration enable

0: Disable

1: Enable

Bit 3~0 **Delta[3:0]:** Define the difference between the detected values with and without card presence

**• WUPeriod Register**

| Address | Bit         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---------------|---|---|---|---|---|---|---|
| 3Dh     | Name        | WUPeriod[7:0] |   |   |   |   |   |   |   |
|         | Type        | R/W           |   |   |   |   |   |   |   |
|         | Reset Value | 0             | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

Bit 7~4 **WUPeriod[7:0]**: Sleep time setting  
 $T[\text{inactivity}] = \text{WUPeriod} \times 256 \times \text{Tclk\_32k}$

**• SwingsCnt Register**

| Address | Bit         | 7       | 6         | 5 | 4 | 3              | 2 | 1 | 0 |
|---------|-------------|---------|-----------|---|---|----------------|---|---|---|
| 3Eh     | Name        | LPCD_en | Skip[2:0] |   |   | SwingsCnt[3:0] |   |   |   |
|         | Type        | R/W     | R/W       |   |   | R/W            |   |   |   |
|         | Reset Value | 0       | 0         | 0 | 0 | 0              | 1 | 0 | 0 |

Bit 7 **LPCD\_en**: Card detection enable in software reset  
 0: Disable  
 1: Enable

Bit 6~4 **Skip[2:0]**: Enhance card detection stability and prevent false wake-up  
 For example, when the tag changes position, the initial detection wave may become unstable, or the detection wave may be unstable at high and low temperatures, which may cause false wake-up. Setting Skip[2:0] can prevent false wake-ups caused by signal jitter.  
 When the number of card detections exceeds the value defined by this field, a TagDetIRQ interrupt request will be generated.

Bit 3~0 **SwingsCnt[3:0]**: Detection time setting  
 $T[\text{detect}] = \text{SwingsCnt} \times 16 \times 4 \times \text{Tclk\_27M12}$

**• Special Register**

| Address | Bit         | 7           | 6 | 5          | 4 | 3        | 2 | 1         | 0         |
|---------|-------------|-------------|---|------------|---|----------|---|-----------|-----------|
| 3Fh     | Name        | ThrAck[1:0] |   | BPSKBSMode |   | Reserved |   | RxWaitEtu | TxWaitEtu |
|         | Type        | R/W         |   | R/W        |   | R/W      |   | R/W       | R/W       |
|         | Reset Value | 0           | 1 | 0          | 1 | 0        | 0 | 0         | 0         |

Bit 7~6 **ThrAck[1:0]**: Demodulation algorithm minimum signal detection amplitude parameter 3

Bit 5~4 **BPSKBSMode[1:0]**: Demodulation algorithm selection  
 00: Auto  
 01: Algorithm 1  
 10: Algorithm 2  
 11: Undefined

Bit 3~2 **Reserved**: Reserved bits

Bit 1 **RxWaitEtu**: RxWait ETU (Elementary Time Unit) setting  
 0: RxWait[5:0] bits in the RxSel register take effect, ETU=128/13.56MHz (about 9.4μs)  
 1: RxWait[5:0] bits in the RxSel register take effect, ETU=64/13.56MHz (about 4.7μs)

Bit 0 **TxWaitEtu**: TxWait ETU (Elementary Time Unit) setting  
 0: TxWait[4:0] bits in the MfTx register take effect, ETU=128/13.56MHz (about 9.4μs)  
 1: TxWait[4:0] bits in the MfTx register take effect, ETU=64/13.56MHz (about 4.7μs)

**Page 5**

PageSel[7:0] must first be set to 0xAE so as to configure the registers in page 5.

**• Analog Register**

| Address | Bit         | 7        | 6 | 5       | 4                 | 3 | 2            | 1 | 0        |
|---------|-------------|----------|---|---------|-------------------|---|--------------|---|----------|
| 31h     | Name        | Reserved |   | TEMP_en | TEMP_Protect[1:0] |   | RefCtrl[1:0] |   | Reserved |
|         | Type        | —        |   | R/W     | R/W               |   | R/W          |   | —        |
|         | Reset Value | 0        | 0 | 0       | 1                 | 0 | 1            | 0 | 0        |

Bit 7~6 **Reserved:** Reserved bits

Bit 5 **TEMP\_en:** High temperature protection enable  
 0: On  
 1: Off

Bit 4~3 **TEMP\_Protect[1:0]:** High temperature protection threshold selection  
 00: Undefined  
 01: 130°C  
 10: 140°C (default)  
 11: 150°C

Bit 2~1 **RefCtrl[1:0]:** ADC quantifiable range control  
 00: 440mV  
 01: 520mV  
 10: 600mV  
 11: 680mV

Bit 0 **Reserved:** Reserved bit

**• Noise Register**

| Address | Bit         | 7               | 6 | 5 | 4                 | 3                  | 2 | 1                 | 0 |
|---------|-------------|-----------------|---|---|-------------------|--------------------|---|-------------------|---|
| 32h     | Name        | NoiseEstm [2:0] |   |   | ForceReSync_ BPSK | BPSKEndFactor[1:0] |   | OOKEndFactor[1:0] |   |
|         | Type        | R/W             |   |   | R/W               | R/W                |   | R/W               |   |
|         | Reset Value | 0               | 1 | 1 | 1                 | 1                  | 1 | 0                 | 1 |

Bit 7~5 **NoiseEstm[2:0]:** Noise evaluation time length factor

Bit 4 **ForceReSync\_BPSK:**  
 If this bit is set to 1, execute resynchronization after demodulating each character of the BPSK frame.

Bit 3~2 **BPSKEndFactor[1:0]:** BPSK modulation end energy threshold factor

Bit 1~0 **OOKEndFactor[1:0]:** OOK modulation end energy threshold factor

**• StepCtrl Register**

| Address | Bit         | 7        | 6 | 5 | 4 | 3         | 2         | 1        | 0 |  |
|---------|-------------|----------|---|---|---|-----------|-----------|----------|---|--|
| 33h     | Name        | Reserved |   |   |   | StepCtrln | StepCtrlp | Reserved |   |  |
|         | Type        | R        |   |   |   | R/W       | R/W       | R        |   |  |
|         | Reset Value | 0        | 0 | 0 | 0 | 0         | 0         | 0        | 0 |  |

Bit 7~4 **Reserved:** Reserved bits

Bit 3 **StepCtrln:** Transmission modulation N driver control bit to control the rising and falling edges of the A/B waveforms

Bit 2 **StepCtrlp:** Transmission modulation P driver control bit to control the rising and falling edges of the A/B waveforms

Bit 1~0 **Reserved:** Reserved bits



**• AgcMin Register**

| Address | Bit         | 7        | 6 | 5            | 4 | 3 | 2            | 1 | 0 |
|---------|-------------|----------|---|--------------|---|---|--------------|---|---|
| 34h     | Name        | Reserved |   | AgcMinValue3 |   |   | AgcMinValue2 |   |   |
|         | Type        | R        |   | R/W          |   |   | R/W          |   |   |
|         | Reset Value | 0        | 0 | 0            | 1 | 0 | 0            | 0 | 0 |

Bit 7~6 **Reserved**: Reserved bits

Bit 5~3 **AgcMinValue3**: AGC amplitude threshold 3

Bit 2~0 **AgcMinValue2**: AGC amplitude threshold 2

**• RxAlgorithm6 Register**

| Address | Bit         | 7          | 6                  | 5 | 4 | 3            | 2              | 1 | 0 |
|---------|-------------|------------|--------------------|---|---|--------------|----------------|---|---|
| 38h     | Name        | Dis848kFlt | PeakValFactor[2:0] |   |   | DisSubEndChk | NoiseLimt[2:0] |   |   |
|         | Type        | R/W        | R/W                |   |   | R/W          | R/W            |   |   |
|         | Reset Value | 0          | 1                  | 1 | 1 | 0            | 1              | 1 | 0 |

Bit 7 **Dis848kFlt**: 848kbit/s subcarrier passing through filter control bit  
 0: Enable  
 1: Disable

Bit 6~4 **PeakValFactor[2:0]**: Subcarrier detection mean amplitude threshold factor

Bit 3 **DisSubEndChk**: Subcarrier end detection control bit  
 0: Enable  
 1: Disable

Bit 2~0 **NoiseLimt[2:0]**: Noise detection threshold

**• RxAlgorithm7 Register**

| Address | Bit         | 7              | 6 | 5                | 4 | 3              | 2 | 1               | 0 |
|---------|-------------|----------------|---|------------------|---|----------------|---|-----------------|---|
| 39h     | Name        | CntConfig[1:0] |   | PulseFactor[1:0] |   | WidthLimt[1:0] |   | OffsetLimt[1:0] |   |
|         | Type        | R/W            |   | R/W              |   | R/W            |   | R/W             |   |
|         | Reset Value | 0              | 1 | 0                | 1 | 0              | 1 | 1               | 0 |

Bit 7~6 **CntConfig[1:0]**: Subcarrier detection cycle threshold factor 2

Bit 5~4 **PulseFactor[1:0]**: Subcarrier detection energy threshold factor 2

Bit 3~2 **WidthLimt[1:0]**: Subcarrier detection cycle threshold factor 3

Bit 1~0 **OffsetLimt[1:0]**: Subcarrier detection cycle threshold factor 4

**• RxAlgorithm8 Register**

| Address | Bit         | 7          | 6 | 5 | 4                  | 3 | 2 | 1                  | 0 |
|---------|-------------|------------|---|---|--------------------|---|---|--------------------|---|
| 3Ah     | Name        | MinPeakVal |   |   | StartBit0Limt[2:0] |   |   | StartBit1Limt[1:0] |   |
|         | Type        | R/W        |   |   | R/W                |   |   | R/W                |   |
|         | Reset Value | 0          | 0 | 1 | 1                  | 0 | 0 | 0                  | 1 |

Bit 7~5 **MinPeakVal**: Subcarrier detection minimum amplitude threshold

Bit 4~2 **StartBit0Limt[2:0]**: Half-Bit0 detection cycle threshold for Manchester frame start bit detection

Bit 1~0 **StartBit1Limt[1:0]**: Half-Bit1 detection cycle threshold for Manchester frame start bit detection

**• RxAlgorithm9 Register**

| Address | Bit         | 7            | 6 | 5 | 4         | 3 | 2 | 1                 | 0 |
|---------|-------------|--------------|---|---|-----------|---|---|-------------------|---|
| 3Bh     | Name        | AgcMinValue1 |   |   | AgcCntNum |   |   | PreambleLimt[1:0] |   |
|         | Type        | RW           |   |   | R/W       |   |   | R/W               |   |
|         | Reset Value | 0            | 0 | 0 | 1         | 0 | 0 | 1                 | 0 |

Bit 7~5 **AgcMinValue1**: AGC amplitude threshold 1

Bit 4~2 **AgcCntNum**: AGC cycle threshold

Bit 1~0 **PreambleLimt[1:0]**: Preamble detection threshold

**Page 6**

PageSel[7:0] must first be set to 0x5A so as to configure the registers in page 6.

**• LPCDRef Register**

| Address | Bit         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---------------------|---|---|---|---|---|---|---|
| 31h     | Name        | ReferenceValue[7:0] |   |   |   |   |   |   |   |
|         | Type        | R                   |   |   |   |   |   |   |   |
|         | Reset Value | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **ReferenceValue[7:0]**: LPCD detection reference value

Note that when there is no tag (i.e., no load) above the antenna, adjust this value to differ from the LPCDADCRef register setting by  $\pm 5$ .

**• LPCDDet Register**

| Address | Bit         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------------|---|---|---|---|---|---|---|
| 32h     | Name        | DetectedValue[7:0] |   |   |   |   |   |   |   |
|         | Type        | R                  |   |   |   |   |   |   |   |
|         | Reset Value | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **DetectedValue[7:0]**: LPCD detection detected value

**• Calibration Register**

| Address | Bit         | 7         | 6         | 5            | 4           | 3           | 2           | 1         | 0 |
|---------|-------------|-----------|-----------|--------------|-------------|-------------|-------------|-----------|---|
| 33h     | Name        | CalibStep | CalibMode | LPCDADCManEn | LPCDEnRCcal | RC32KCalMan | RC27MCalMan | LPCDUseRC |   |
|         | Type        | R/W       | R/W       | R/W          | R/W         | R/W         | R/W         | R/W       |   |
|         | Reset Value | 0         | 0         | 0            | 0           | 0           | 0           | 0         | 0 |

Bit 7~6 **CalibStep**: CWGsP\_lpcd adjustment step size and range when CalibMode=1

- 00: Step=1, [CWGsP\_lpcd-8, CWGsP\_lpcd+7]
- 01: Step=2, [CWGsP\_lpcd-16, CWGsP\_lpcd+14]
- 10: Step=3, [CWGsP\_lpcd-24, CWGsP\_lpcd+21]
- 11: Step=4, [2, 62]

Bit 5 **CalibMode**: When CalibEn=1 and the LPCD mode is entered

- 0: Directly use the ADC sample data as the reference value
- 1: Adjust CWGsP\_lpcd, use the ADC data close to LPCDADCRef setting as the reference value

Bit 4 **LPCDADCManEn**: LPCD ADC manual enable

Bit 3 **LPCDEnRCcal**: Enable RC27MHz and RC32kHz calibration after the end of LPCD

- When LPCD\_en=1, enforce the RC27MHz calibration once;
- When LPCD\_en=1 or CLK32K\_En=1, enforce the RC32kHz calibration once.

Bit 2 **RC32KCalMan**: LPCD 32kHz RC manual calibration enable

Bit 1 **RC27MCalMan**: LPCD 27.12MHz RC manual calibration enable

Bit 0 **LPCDUseRC**: LPCD 27.12MHz RC enable

**• RC27MCalValue Register**

| Address | Bit         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---------------|---|---|---|---|---|---|---|
| 34h     | Name        | RC27MCalValue |   |   |   |   |   |   |   |
|         | Type        | R/W           |   |   |   |   |   |   |   |
|         | Reset Value | 1             | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **RC27MCalValue**: LPCD 27.12MHz RC calibration value

**• RC32KCalValue Register**

| Address | Bit         | 7        | 6 | 5             | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|----------|---|---------------|---|---|---|---|---|
| 35h     | Name        | Reserved |   | RC32KCalValue |   |   |   |   |   |
|         | Type        | —        |   | R/W           |   |   |   |   |   |
|         | Reset Value | 0        | 0 | 1             | 0 | 0 | 0 | 0 | 0 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5~0 **RC32KCalValue:** LPCD 32kHz RC calibration value

**• LPCDADCRef Register**

| Address | Bit         | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|------------|---|---|---|---|---|---|---|
| 36h     | Name        | LPCDADCRef |   |   |   |   |   |   |   |
|         | Type        | R/W        |   |   |   |   |   |   |   |
|         | Reset Value | 1          | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **LPCDADCRef:** LPCD ADC reference value

**• CWGsN\_LPCD Register**

| Address | Bit         | 7               | 6 | 5 | 4 | 3        | 2 | 1 | 0 |  |
|---------|-------------|-----------------|---|---|---|----------|---|---|---|--|
| 38h     | Name        | CWGsN_LPCD[3:0] |   |   |   | Reserved |   |   |   |  |
|         | Type        | R/W             |   |   |   | —        |   |   |   |  |
|         | Reset Value | 0               | 0 | 1 | 1 | 0        | 0 | 0 | 0 |  |

Bit 7~4 **CWG<sub>s</sub>N\_LPCD[3:0]:** Define the conductance value of N driver during the LPCD mode

Bit 3~0 **Reserved:** Reserved bits

**• CWGsP\_LPCD Register**

| Address | Bit         | 7        | 6 | 5               | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|----------|---|-----------------|---|---|---|---|---|
| 39h     | Name        | Reserved |   | CWGsP_LPCD[5:0] |   |   |   |   |   |
|         | Type        | —        |   | R/W             |   |   |   |   |   |
|         | Reset Value | 0        | 0 | 0               | 1 | 1 | 1 | 1 | 1 |

Bit 7~6 **Reserved:** Reserved bits

Bit 5~0 **CWG<sub>s</sub>P\_LPCD[5:0]:** Define the conductance value of P driver during the LPCD mode

## Command Set

The BC45B4522 operation is determined by an internal state machine capable of executing a set of commands. A command is executed by writing its command code into the Command register.

The parameters and/or data required for a command are processed by the FIFO buffer.

## General Features

Each command that requires a data bit stream (or data byte stream) as input immediately processes any data in the FIFO buffer. An exception to this is the Transceive command, which starts the transmitter by setting the StartSend bit in the BitFraming register.

Each command that requires some preset parameters only starts running when the correct number of parameters are received from the FIFO buffer.

The FIFO buffer is not immediately cleared when the commands start. Therefore, it is possible to write command parameters and data to the FIFO buffer before starting the command.

Each command can be interrupted by a new command written to the Command register, such as the Idle command.

## Command Overview

| Command     | Command Code | Action   |
|-------------|--------------|--|
| Idle        | 0000         | No action; cancels the current command execution   |
| CalcCRC     | 0011         | Activates the CRC coprocessor or performs a self-test  |
| Transmit    | 0100         | Transmits data from the FIFO buffer  |
| NoCmdChange | 0111         | No command change; used to modify some bits of the Command register without affecting the current command, such as the PowerDown bit |
| Receive     | 1000         | Activates the receiver circuit   |
| Transceive  | 1100         | Transmits data from the FIFO buffer to antenna and automatically activates the receiver after transmission                           |
| MFAuthent   | 1110         | Performs the MIFARE standard authentication as a reader  |
| SoftReset   | 1111         | Reset the chip   |

## Command Description

### Idle Command

This command places the chip in the idle mode. The command terminates itself.

### CalcCRC Command

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation starts. The calculation result is stored in the CRCResult\_H and CRCResult\_L registers. The CRC calculation is not limited to some specific bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is also added to the calculation.

The CRC preset value is controlled by the CRCPreset[1:0] bit field in the Mode register. The preset value is loaded into the CRC coprocessor when the command starts.

This command must be terminated by writing any command to the Command register, such as the Idle command.

### Transmit Command

The FIFO buffer content is transmitted immediately after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be properly configured for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the Command register.

### NoCmdChange Command

This command does not affect any running command in the Command register. It can be used to modify any bit in the Command register except the Command[3:0], such as RcvOff bit or PowerDown bit.

### Receive Command

The receiver circuit is activated by this command and then waits for a data stream to be received. All relevant registers must be correctly configured before starting this command.

This command automatically terminates when data stream ends. This is indicated by the frame end pattern or by the length byte according to the selected frame type and speed.

Note that the Receive command will not automatically terminate if the RxMultiple bit in the RxMode register is set to 1. In this case, the command must be terminated by starting another command in the Command register.

### Transceive Command

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmitting and after transmission the command changes to receive a data stream.

Each transmission process is started by setting the StartSend bit in the BitFraming register to logic 1. This command must be cleared by writing any other command to the Command register.

Note that if the RxMultiple bit in the RxMode register is set to 1, the Transceive command never leaves the receiving state because this state cannot be automatically cancelled.

### MFAuthent Command

This command is used to perform the Crypto\_M authentication to enable secure communication with any Crypto\_M common cards. The following data must be written into the FIFO buffer before starting

the command.

- Authentication command code (0x60, 0x61)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

12 bytes in total must be written into the FIFO buffer.

Note that all FIFO accesses are blocked when the MFAuthent command is active. If there is an access to the FIFO buffer, the WrErr bit in the Error register will be set high.

This command automatically terminates when the Crypto\_M card is authenticated and the MFCrypto1On bit in the Status2 register is set high.

This command does not automatically terminate if the card does not respond. Therefore, the timer must be initialised to the automatic mode. In this case, in addition to the IdleIRq flag, the TimerIRq flag can also be used as the command termination criterion. During the authentication process, the RxIRq and TxIRq flags are blocked. The MFCrypto1On bit is valid only after the authentication command is completed, either after processing the agreement or after writing the Idle command code to the Command register.

If an error occurs during the authentication process, the ProtocolErr bit in the Error register is set high and the MFCrypto1On bit in the Status2 register is cleared to zero.

#### **SoftReset Command**

This command performs a reset to the chip. The data in the internal buffer remains unchanged and all registers are set to the reset values. The command automatically terminates when finished.

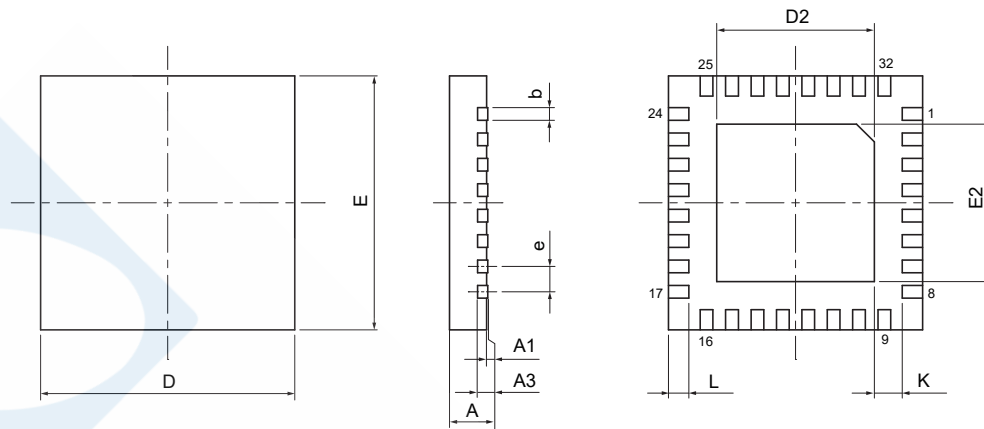
Note: The SerialSpeed register is reset and therefore the serial data rate is set to 9.6kbit/s.

## Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package/ Carton Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- [Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [Packing Materials Information](#)
- [Carton information](#)

**SAW Type 32-pin QFN (4mm×4mm×0.75mm) Outline Dimensions**


| Symbol | Dimensions in inch |       |       |
|--------|--------------------|-------|-------|
|        | Min.               | Nom.  | Max.  |
| A      | 0.028              | 0.030 | 0.031 |
| A1     | 0.000              | 0.001 | 0.002 |
| A3     | 0.008 REF          |       |       |
| b      | 0.006              | 0.008 | 0.010 |
| D      | 0.157 BSC          |       |       |
| E      | 0.157 BSC          |       |       |
| e      | 0.016 BSC          |       |       |
| D2     | 0.100              | —     | 0.108 |
| E2     | 0.100              | —     | 0.108 |
| L      | 0.014              | 0.016 | 0.018 |
| K      | 0.008              | —     | —     |

| Symbol | Dimensions in mm |      |      |
|--------|------------------|------|------|
|        | Min.             | Nom. | Max. |
| A      | 0.70             | 0.75 | 0.80 |
| A1     | 0.00             | 0.02 | 0.05 |
| A3     | 0.203 REF        |      |      |
| b      | 0.15             | 0.20 | 0.25 |
| D      | 4.00 BSC         |      |      |
| E      | 4.00 BSC         |      |      |
| e      | 0.40 BSC         |      |      |
| D2     | 2.55             | —    | 2.75 |
| E2     | 2.55             | —    | 2.75 |
| L      | 0.35             | 0.40 | 0.45 |
| K      | 0.20             | —    | —    |

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