## **RISC-V**

GOWIN Semiconductor now offers a solution of implementing configurable RISC-V IP in GW-2A FPGA. Here, the configurable RISC-V IP Core and System is a 32-bit RISC-V Microprocessor & Peripheral System with the following list of Architecture Structure and feature set:



Feature Set RISC-V with 5 pipe-lined structure RISC-V RV32IMAC, Atomic instruction Individually configurable ILM and DLM standard JTAG interface PLIC DMA -RTC -GPIO UART QSPI I2C PWM/PIT

Watch-Dog

The GOWIN Development Platform combines the RISC-V Microprocessor SW design flow and FPGA HW Design flow as a fully integrated single toolchain consisting of all GOWIN device model libraries and software driver libraries needed to program the GW2A-18/55 FPGA hosting with the configurable RISC-V & System Peripheral. The platform supports Application software compiling, linking, in-circuit-emulation/debugging on behalf of the embedded RISC-V microprocessor as well as synthesis and place & route of the FPGA design embedded with the RISC-V & System Soft IP.





A Development Board is also available to be used in conjunction with the

GOWIN programming tools for implementing RISC-V Microprocessor & Peripherals System in FPGA-SoC Design.



**RISC-V** for GW2A Release – Software Package and Documentation:

- 1. Go to http://gowinsemi.com/support/home/
- 2. Click "Download GOWIN EDA (Registration is required)

- 3. Choose Windows or Linux
- Download Two Software Packages a. Download the Gowin\_YunYuan\_V1.8.1.01Beta(\_win or \_linux) or later b. Under "RISC V for GW2A Release Package", click on the Dropbox link and download RISC-V for GW2A Release Package.
- 5. Go to http://gowinsemi.com/support/home/ and Click on "Apply License" for the GOWIN EDA FPGA Design License.
- 6. Go to http://www.gowinsemi.com/support/enquires/ and fill out form. Under "Enquiry" type "Request for AndeSight RDS for GOWIN SW Tool Chain License"

