FPGA's are known for high-speed IO interface flexibility as well as their ability to pipeline data processing with arithmetic logic elements. However, no FPGA company to date has been able to cost-effectively interface an FPGA directly to USB 2.0 due to its data rate, clock recovery, and IO requirements. As a result, product manufacturers have been limited to custom ASICs, feature limited microcontrollers, or expensive SoCs in order to enable USB 2.0 support.

The new GOWIN USB 2.0 interfacing solution eliminates the need for external PHYs, which were previously required to achieve USB HS (high speed) 480Mbps data rates. Popular applications include bridging to other peripherals such as JTAG, SPI, and I2S, communicating with MIPI CSI-2 cameras and DSI displays, developing USB hubs, data traffic monitors and recorders, Bluetooth LE, and security dongles.

GOWIN Semiconductor has been pathing the way for innovative new FPGA products for several years now and the release of their USB 2.0 interfacing solution is the latest edition to this success. The solution includes a USB v2.0 soft PHY as well as a USB v2.0 Device Controller IP, which are included in GOWIN's EDA Software's IP Core Generator. **The USB 2.0 IPs are available free of charge with all GOWIN FPGA products.** A reference design, as well as development boards, are available, which instantiate the USB 2.0 IP cores along with a USB 2.0 to UART bridging example to get started. The IP cores support almost all GOWIN FPGAs and provide a line rate of 480Mbps in High-Speed mode per the USB 2.0 specification.

Contact Alcom for Evaluation Unit or GW2AR-18 Datasheet