



GW2A series of FPGA Products

Data Sheet

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Revision History

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1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW2A series of the FPGA products, which helps you to understand the GW2A series of the FPGA products quickly and select and use devices appropriately.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [UG290, Gowin FPGA Products Programming and Configuration User Guide](#)
- [UG111, GW2A series FPGA Products Package and Pinout](#)
- [UG110, GW2A-18 Pinout](#)
- [UG113, GW2A-55Pinout](#)

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables

Abbreviations and Terminology	Name
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
TDM	Time Division Multiplexing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
GPIO	Gowin Programmable IO
LQ144	LQFP144
EQ144	ELQFP144
PG256	PBGA256
PG256S	PBGA256S
PG256C	PBGA256C
PG256E	PBGA256E
PG484	PBGA484
PG1156	PBGA1156
UG324	UBGA324
UG324D	UBGA324D
UG676	UBGA676

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com



Electronics

2 General Description

The GW2A series of FPGA products are the first generation products of the Arora family. They offer a range of comprehensive features and rich internal resources like high-performance DSP resources, a high-speed LVDS interface, and abundant BSRAM memory resources. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products suitable for high-speed, low-cost applications.

GOWINSEMI continually invests the development of next-generation FPGA hardware environment through the market-oriented independent research and developments that supports the GW2A series of FPGA products, which can be used for FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- Lower power consumption
 - 55nm SRAM technology
 - Core voltage: 1.0V
 - Clock dynamically turns on and off
- Multiple I/O standards
 - LVC MOS33/25/18/15/12; LV TTL33, SSTL33/25/18 I, II, SSTL15; HSTL18 I, II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE MLVDSE, LVPECLE, RSDSE
 - Input hysteresis option
 - Supports 4mA, 8mA, 16mA, 24mA, etc. drive options
 - Slew rate option
 - Output drive strength option
 - Individual bus keeper, weak pull-up, weak pull-down, and open drain option
 - Hot socket
- High performance DSP
 - High performance digital signal processing ability
 - Supports 9 x 9, 18 x 18, 36 x 36 bits multiplier and 54 bits accumulator;
 - Multipliers cascading
 - Registers pipeline and bypass

- Adaptive filtering through signal feedback
- Supports barrel shifter
- Abundant slices
 - Four input LUT (LUT4)
 - Double-edge flip-flops
 - Supports shift register and distributed register
- Block SRAM with multiple modes
 - Supports dual port, single port, and semi-dual port
 - Supports bytes write enable
- Flexible PLLs
 - Frequency adjustment (multiply and division) and phase adjustment
 - Supports global clock
- Configuration
 - JTAG configuration
 - Four GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT
 - Data stream file encryption and security bit settings

2.2 Product Resources

Table 2-1 Product Resources

Device	GW2A-18	GW2A-55
LUT4	20,736	54,720
Flip-Flop (FF)	15,552	41,040
Shadow SRAM S-SRAM (bits)	41,472	109,440
Block SRAM B-SRAM (bits)	828K	2,520K
B-SRAM quantity B-SRAM	46	140
18 x 18 Multiplier	48	40
Maximum ¹ (PLLs)	4	6
Total number of I/O banks	8	8
Max. I/O	384	608
Core voltage	1.0V	1.0V

Note!

[1]Different packages support different numbers of PLL. Up to six PLLs can be supported.

Table 2-2 GW2A-18 PLL List

Package	Device	PLL
LQ144 ¹	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
EQ144 ¹	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
MG196 ²	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1
QN88	GW2A-18	PLLL1/ PLLR1
PG256	GW2A-18	PLLL/PLLR
PG256S	GW2A-18	PLLL/PLLR

Package	Device	PLL
PG256C	GW2A-18	PLLL/PLLR
PG256E ³	GW2A-18	PLLL0/PLLR0
PG484	GW2A-18	PLLL/PLLR
UG324	GW2A-18	PLLL0/PLLL1/PLLR0/PLLR1

Note!

- [1] For the LQ144 and EQ144 package, V_{CCPLL1} and V_{CC} are internal short circuited.
- [2] For the MG196/UG324 package, V_{CCPLL} , V_{CCPLLR} , and V_{CC} are internal short circuited.
- [3] For the PG256E package, V_{CCPLL0} , $V_{CCPLLR0}$, and V_{CC} are internal short circuited.

Table 2-3 Package Information and Max. I/O

Package	Pitch(mm)	Size(mm)	E-pad Size (mm)	GW2A-18	GW2A-55
QN88	0.4	10 x 10	6.74 x 6.74	66 (22)	-
LQ144	0.5	20 x 20	-	119 (34)	-
EQ144	0.5	20 x 20	9.74 x 9.74	119 (34)	-
MG196	0.5	8 x 8	-	114 (39)	-
PG256	1.0	17 x 17	-	207 (73)	-
PG256S	1.0	17 x 17	-	192 (72)	-
PG256C	1.0	17 x 17	-	190 (64)	-
PG256E	1.0	17 x 17	-	162 (29)	-
PG484	1.0	23 x 23	-	319 (78)	319 (76)
PG1156	1.0	35 x 35	-	-	607 (97)
UG324	0.8	15 x 15	-	239 (90)	240 (86)
UG324D	0.8	15 x 15	-	-	240 (71)
UG676	0.8	21 x 21	-	-	525 (97)

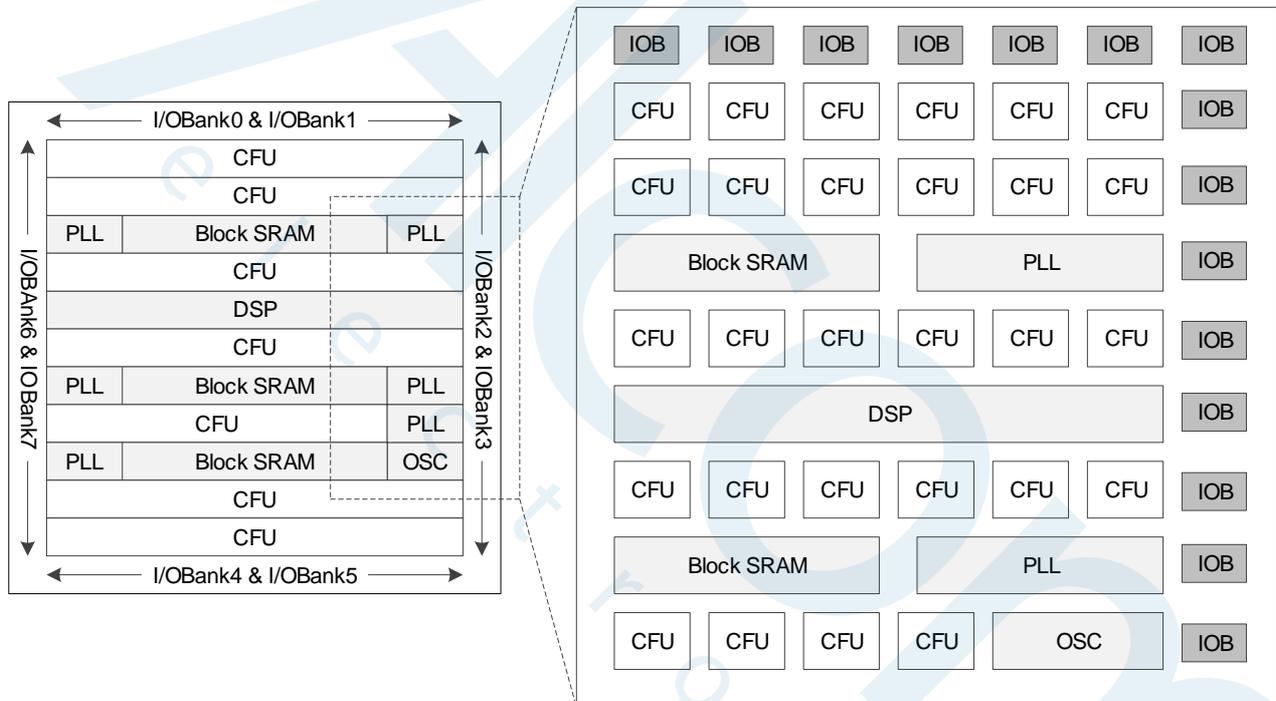
Note!

- [1] The package types in this data sheet are written with abbreviations. See [5.1 Part Name](#) for further information.
- “” denotes that the various device pins are compatible when the package types are the same.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O; When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O plus one;
- The IO speed of JTAG pins multiplexing is less than 40 MHz.

3 Architecture

3.1 Architecture Overview

Figure 3-1 Architecture Diagram



See Figure 3-1 for an overview of the architecture of the GW2A series of FPGA products. Please refer to Table 2-1 for GW2A-18 and GW2A-55 devices internal resources. The core of device is an array of Configurable Logic Unit (CFU) surrounded by IO blocks. Besides, GW2A provides B-SRAM, DSP, PLL, and on chip oscillator.

Configurable Function Unit (CFU) is the base cell for the array of GW2A series FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see [3.2 Configurable Function Unit](#).

The I/O resources in the GW2A series of FPGA products are arranged around the periphery of the devices in groups referred to as banks, which are divided into eight Banks, including Bank0 ~ Bank7. I/O resources support multiple I/O standards, and support regular mode, SRD mode, generic DDR mode, and DDR_MEM mode. For more detailed information, see [3.3IOB](#).

The B-SRAM is embedded as a row in the GW2A series of FPGA products. In the FPGA array, each B-SRAM occupies three columns of CFU. Each B-SRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. For more detailed information, see [3.4Block SRAM \(B-SRAM\)](#).

DSP is embedded in the GW2A series of FPGA products. DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two multipliers with 18 by 18 inputs, and a three input ALU54. For more detailed information, see [3.5 DSP](#).

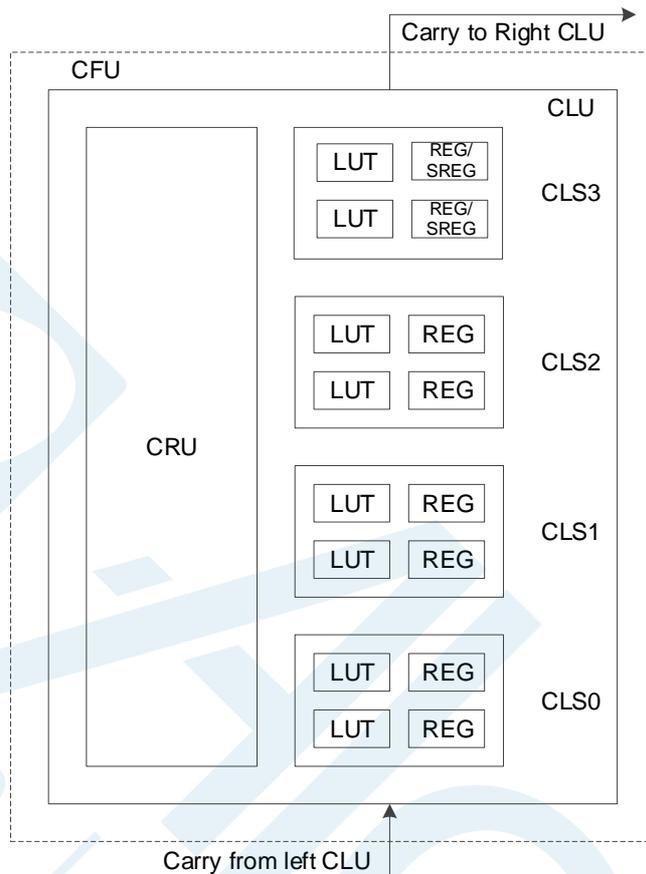
GW2A provides one PLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each GW2A series of FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125 MHz, providing the clock resource for the MSPI mode. It also provides a clock resource for user designs with the clock precision reaching $\pm 5\%$. For more detailed information, please refer to [3.6Clock](#), [3.10On Chip Oscillator](#).

FPGA provides abundant CRUs, connecting all the resources in the FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW2A series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more detailed information, see [3.6Clock](#), [3.7Long Wire \(LW\)](#), and [3.8Global Set/Reset \(GSR\)](#).

3.2 Configurable Function Unit

The configurable function unit (CFU) is the base cell for the array of the GW2A series of FPGA Products. Each CFU consists of a configurable logic unit (CLU) and its routing resource configurable routing unit (CRU). In each CLU, there are four configurable logic slices (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-2 below.

Figure 3-2 CFU Structure

**Note!**

SERG needs special patch supporting. Please contact Gowin technical support or local Office for this patch.

3.2.1 CLU

The CLU supports three operation modes: Basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

Each LUT can be configured as one four-input LUT. Higher input number of LUT can be formed by combining the LUT4 together.

- Each CLS can form one five input LUT5.
- Two CLSs can form one six input LUT6.
- Four CLSs can form one seven input LUT7.
- Eight CLSs (two CLUs) can form one eight-input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as the ALU mode to implement the following functions.

- Adder and subtractor
- Up/down counter
- Comparator, including greater-than, less-than, and not-equal-to
- MULT

- Memory mode

In this mode, a 16 x 4 S-SRAM or ROM can be constructed by using CLSs.

This SRAM can be initialized during the device configuration stage. The initialization data can be generated in the bit stream file from Gowin Yunyuan software.

Each configurable logic slice (CLS) has two registers (REG), as shown in Figure3-3 below.

Figure3-3 Register in CLS

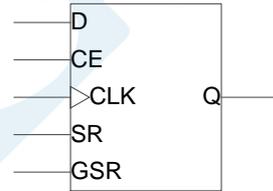


Table 3-1 Register Description in CLS

Signal	I/O	Description
D	I	Data input ¹
CE	I	CLK enable, can be high or low effective ²
CLK	I	Clock, can be rising edge or falling edge triggering ²
SR	I	Set/Reset, can be configured as ² : <ul style="list-style-type: none"> ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSR ^{3,4}	I	Global Set/Reset, can be configured as ⁴ : <ul style="list-style-type: none"> ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Register

Note!

- [1] The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU is independent.
- [3] In the GW2A series of FPGA products, GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

3.2.2 CRU

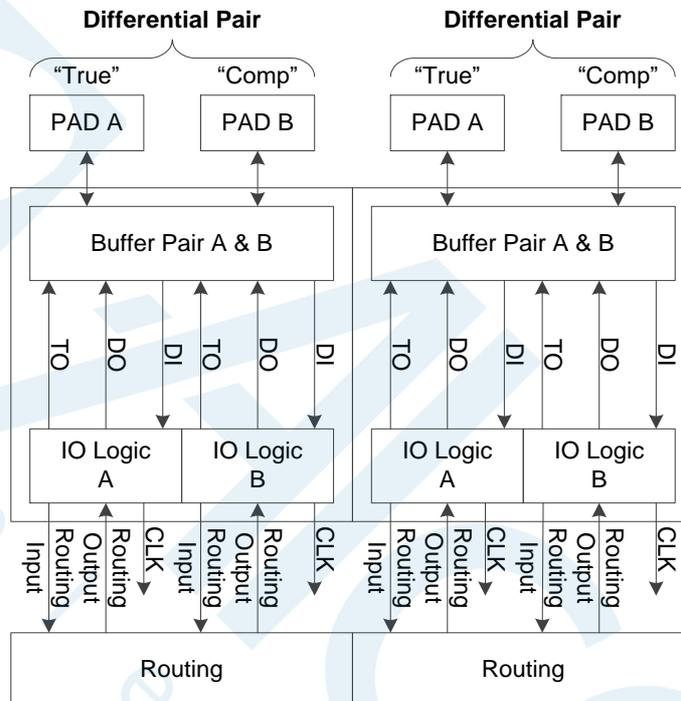
The main functions of the CRU are as follows:

- Input selection: Select input signals for the CFU.
- Configurable Routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

3.3 IOB

The IOB in the GW2A series of FPGA products includes IO Buffer, IO Logic, and its Routing Unit. As shown below, each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as a single end input/output.

Figure 3-4 IOB Structure View



IOB Features:

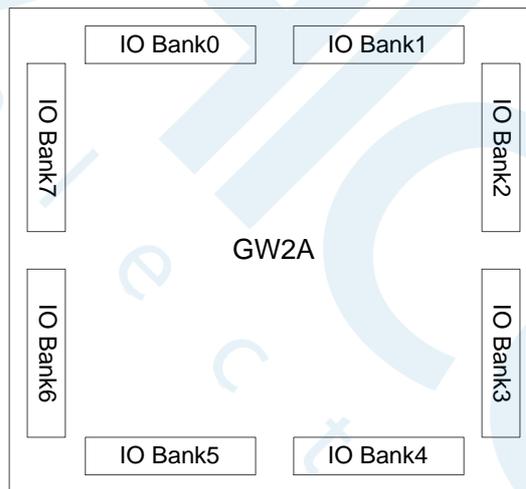
- V_{CC0} supplied with each bank
- LVCMOS, PCI, LVTTTL, LVDS, SSTL, and HSTL
- Input hysteresis option
- Output drive strength option
- Slew rate option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode

3.3.1 I/O Buffer

There are eight I/O Banks in the GW2A series of FPGA products, as shown in Figure 3-5. Each Bank has independent IO source V_{CCO} . V_{CCO} can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V. For LQ144 devices, $V_{CCO2/6}$ and V_{CCX} are internal short-circuited, and the power supply can be set to 2.5V and 3.3V. For more detailed information, please refer to Table 4-2. In order to support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as reference voltage. User can choose from internal reference voltage of the bank ($0.5 \times V_{CCO}$) or external reference voltage using any IO from the bank. V_{CCX} is 2.5V and 3.3V.

Different banks in the GW2A Series of FPGA Products support different on-chip resistor settings, including single-ended resistor and differential resistor. Single-ended resistor is set for SSTL/HSTL I/O and is supported in Bank 2/3/6/7. Differential resistor is set for LVDS input and is only supported in Bank 0/1. Please refer to [UG289, Gowin Programmable IO User Guide](#) for more detailed information.

Figure 3-5 GW2A I/O Bank Distribution



Note!

By default, the Gowin Programmable IO is tri-stated weak pull-up.

For the V_{CCO} requirements of different I/O standards, see Table 3-2.

Table 3-2 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVTTTL33	Single end	3.3	4,8,12,16,24
LVC MOS33	Single end	3.3	4,8,12,16,24
LVC MOS25	Single end	2.5	4,8,12,16
LVC MOS18	Single end	1.8	4,8,12
LVC MOS15	Single end	1.5	4,8
LVC MOS12	Single end	1.2	4,8
SSTL25_I	Single end	2.5	8
SSTL25_II	Single end	2.5	8

I/O output standard	Single/Differ	Bank V _{CCO} (V)	Driver Strength (mA)
SSTL33_I	Single end	3.3	8
SSTL33_II	Single end	3.3	8
SSTL18_I	Single end	1.8	8
SSTL18_II	Single end	1.8	8
SSTL15	Single end	1.5	8
HSTL18_I	Single end	1.8	8
HSTL18_II	Single end	1.8	8
HSTL15_I	Single end	1.5	8
PCI33	Single end	3.3	N/A
LVPECL33E	Differential	3.3	16
MLVDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8
LVDS25	Differential	2.5/3.3	3.5/2.5/2/1.25
RSDS	Differential	2.5/3.3	2
MINILVDS	Differential	2.5/3.3	2
PPLVDS	Differential	2.5/3.3	3.5
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8
HSTL18D_II	Differential	1.8	8
HSTL15D_I	Differential	1.5	8

Table 3-3 Output I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V _{CCO} (V)	Hysteresis	Need V _{REF}
LVTTTL33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS25	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS18	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVC MOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single end	1.5/1.8/2.5/3.3	No	Yes

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
SSTL25_I	Single end	2.5/3.3	No	Yes
SSTL25_II	Single end	2.5/3.3	No	Yes
SSTL33_I	Single end	3.3	No	Yes
SSTL33_II	Single end	3.3	No	Yes
SSTL18_I	Single end	1.8/2.5/3.3	No	Yes
SSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL18_I	Single end	1.8/2.5/3.3	No	Yes
HSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL15_I	Single end	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single end	3.3	Yes	No
LVDS	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No

3.3.2 I/O Logic

Figure 3-6 shows the I/O logic output of the GW2A series of FPGA products.

Figure 3-6 I/O Logic Output

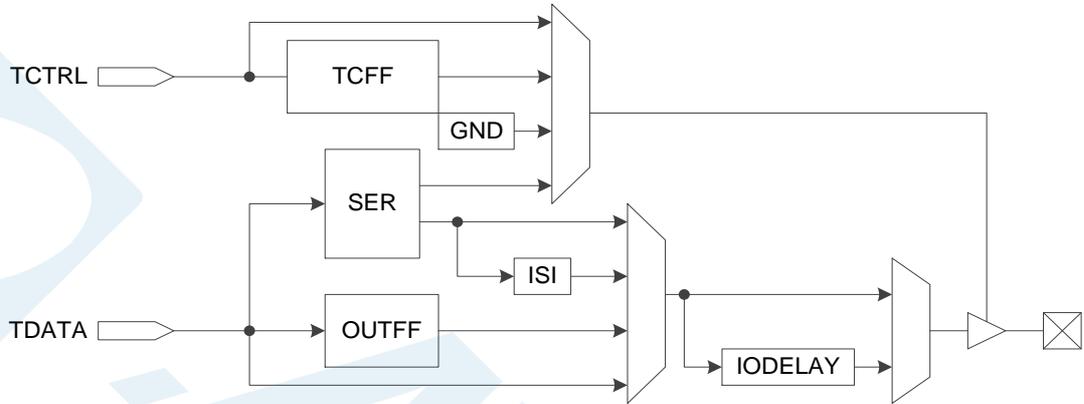
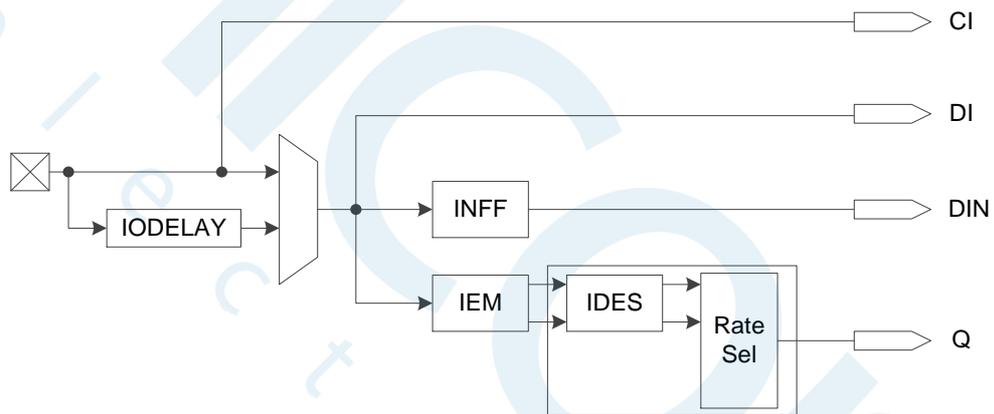


Figure 3-7 shows the I/O logic input of the GW2A series of FPGA products.

Figure 3-7 I/O Logic Input

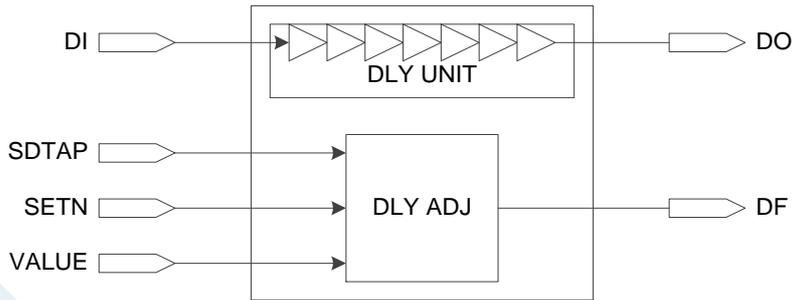


A description of the I/O logic modules of the GW2A series of FPGA products is presented below.

IODELAY

See Figure 3-8 for an overview of the IODELAY. Each I/O of the GW2A series of FPGA products has an IODELAY cell. A total of 128(0~127) step delay is provided, with one-step delay time of about 18ps.

Figure 3-8 IODELAY



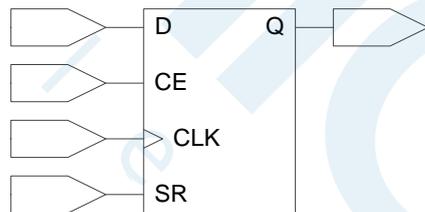
The delay cell can be controlled in two ways:

- Static control.
- Dynamic control: Usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time.

I/O Register

See Figure 3-9 for the I/O register in the GW2A series of FPGA products. Each I/O provides one input register, INFF, one output register, OUTFF, and a tristate Register, TCFF.

Figure 3-9 Register Structure in I/O Logic



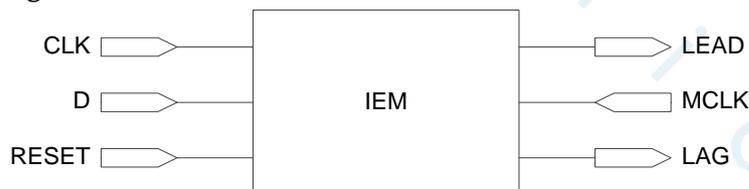
Note!

- CE can be either active low (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode, as shown in Figure 3-10.

Figure 3-10 IEM Structure



De-serializer DES and Clock Domain Transfer

The GW2A series of FPGA products provides a simple serializer SER for each output I/O to support advanced I/O protocols. The Clock domain transfer module of the input clock in DES provides the ability to safely

switch the external sampling clock to the internal continuous running clock. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- The internal continuous clock is used instead of the discontinuous DQS for data sampling. The function is applied to the interface of DDR memory.
- For the DDR3 memory interface standard, align the data after DQS read-leveling.
- In regular DDR mode, when DQS.RCLK is used for sampling, the clock domain transfer module also needs to be used.

Each DQS provides WADDR and RADDR signals to the same group in the clock domain transfer module.

Serializer SER

The GW2A series of FPGA products provides a simple serializer (SER) for each output I/O to support advanced I/O protocols.

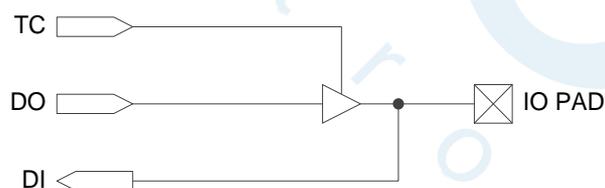
3.3.3 I/O Logic Modes

The I/O Logic in the GW2A series of FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-11, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

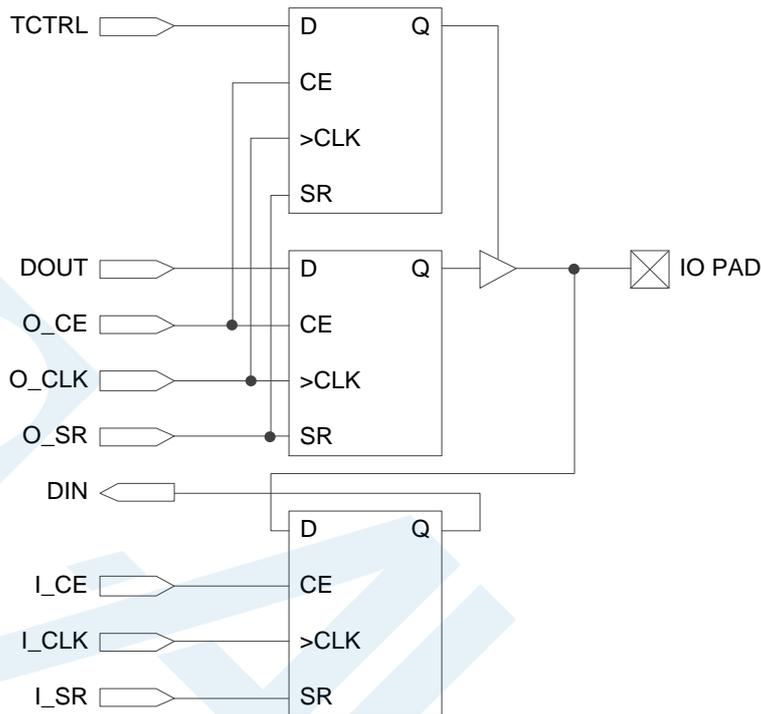
Figure 3-11 I/O Logic in Basic Mode



SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-12. This can effectively improve IO timing.

Figure 3-12 I/O Logic in SDR Mode



Note!

- CLK enable O_CE and I_CE can be configured as active high or active low;
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O_SR and I_SR can be either synchronized reset, synchronized set, asynchronous reset, asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

Generic DDR Mode

Higher speed I/O protocols can be supported in generic DDR mode.

Figure 3-13 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

Figure 3-13 I/O Logic in DDR Input Mode

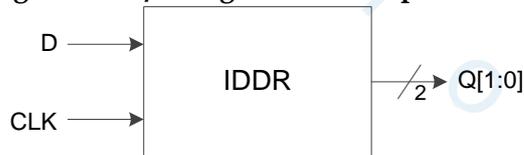
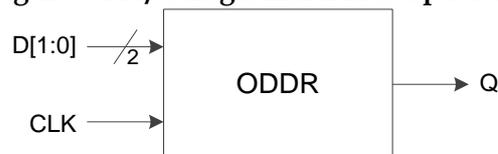


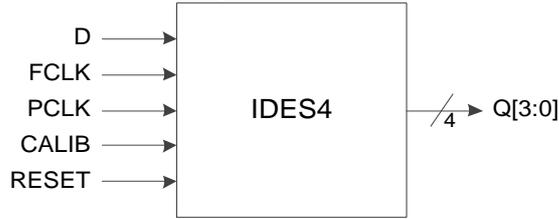
Figure 3-14 shows the generic DDR output, with a speed ratio of PAD to FPGA internal logic 2:1.

Figure 3-14 I/O Logic in DDR Output Mode

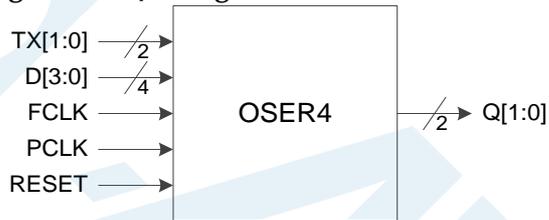


IDES4

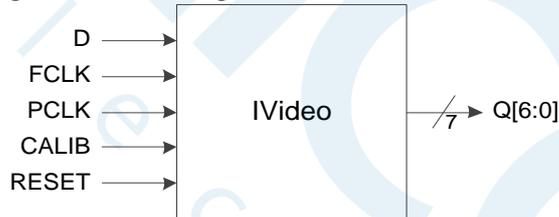
In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

Figure 3-15 I/O Logic in IDES4 Mode**OSER4 Mode**

In OSER4 mode, the speed ratio of PAD to FPGA internal logic is 4:1.

Figure 3-16 I/O Logic in OSER4 Mode**IVideo Mode**

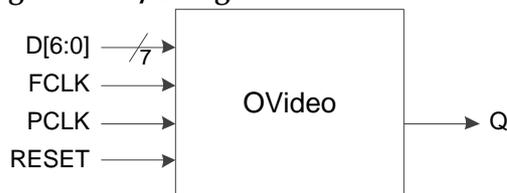
In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

Figure 3-17 I/O Logic in IVideo Mode**Note!**

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

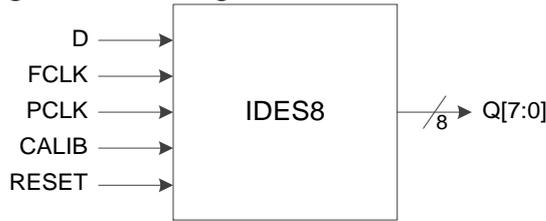
OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is 7:1.

Figure 3-18 I/O Logic in OVideo Mode**IDES8 Mode**

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

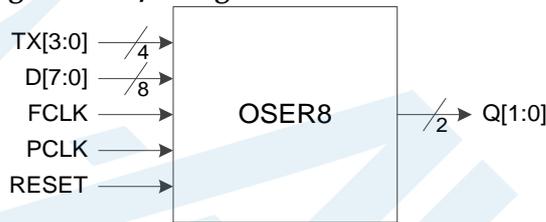
Figure 3-19 I/O Logic in IDER8 Mode



OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

Figure 3-20 I/O Logic in OSER8 Mode



IDER10 Mode

In IDER10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

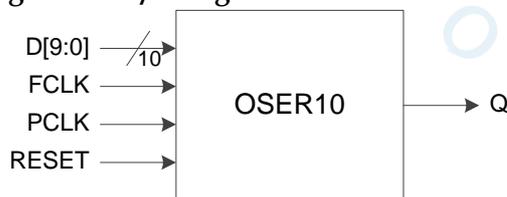
Figure 3-21 I/O Logic in IDER10 Mode



OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

Figure 3-22 I/O Logic in OSER10 Mode



The GW2A series of FPGA products support IO interface mode with memory, support double/four/eight speed rate input and output, including IDDR_MEM, IDER4_MEM, IDER8_MEM, ODDR_MEM, OSER4_MEM, and OSER8_MEM modes.

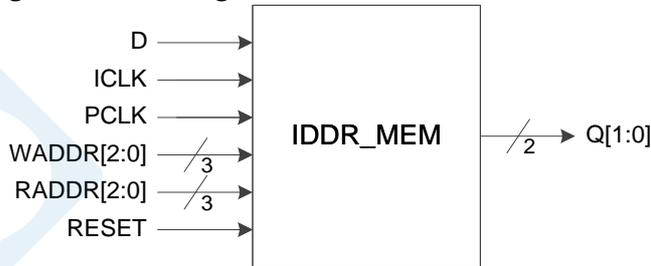
IDDR_MEM/IDER4_MEM/IDER8_MEM needs to be used with DQS. ICLK connects output signal DQSR90 of DQS and sends data to IO interfaces according to ICLK clock edge. WADDR [2: 0] connects output signal WPOINT of DQS; RADDR [2: 0] connects output signal RPOINT of

DQS.

ODDR_MEM/OSER4_MEM/OSER8_MEM needs to be used with DQS. TCLK connects output signal DQSW0 or DQSW270 of DQS, and outputs data from IO interfaces according to TCLK clock edge.

IDDR_MEM Mode

Figure 3-23 I/O Logic in IDDR_MEM Mode



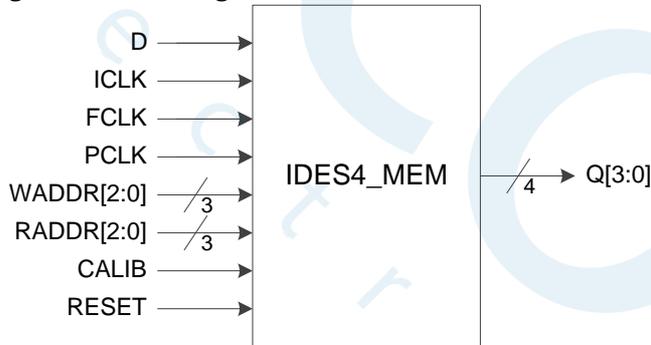
ODDR_MEM Mode

Figure 3-24 I/O Logic in ODDR_MEM Mode



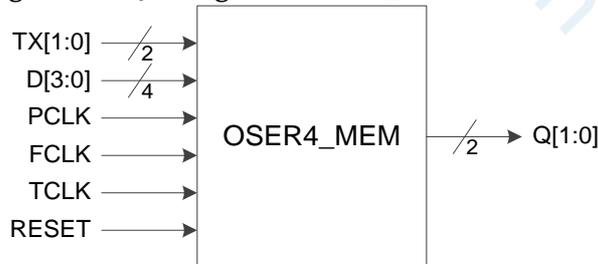
IDES4_MEM Mode

Figure 3-25 I/O Logic in IDES4_MEM Mode



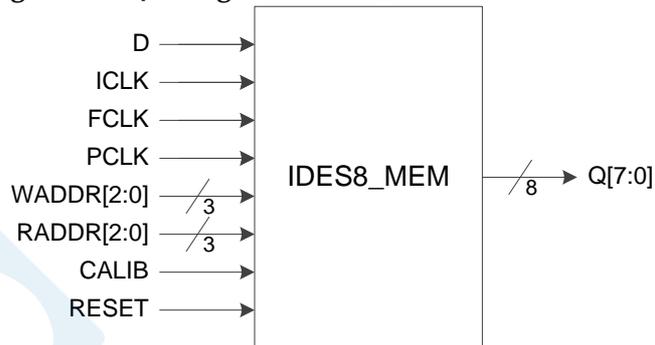
OSER4_MEM Mode

Figure 3-26 I/O Logic in OSER4_MEM Mode



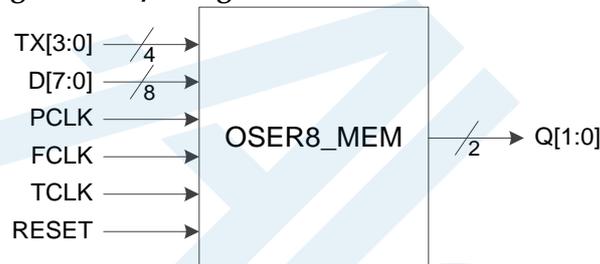
IDES8_MEM Mode

Figure 3-27 I/O Logic in IDES8_MEM Mode



OSER8_MEM Mode

Figure 3-28 I/O Logic in OSER8_MEM Mode



3.4 Block SRAM (B-SRAM)

3.4.1 Introduction

The GW2A series of FPGA products provide abundant SRAM. The Block SRAM (B-SRAM) is embedded as a row in the FPGA array and is different from S-SRAM (Shadow SRAM). Each B-SRAM occupies three columns of CFU in the FPGA array. Each B-SRAM has 18,432 bits (18Kbits). There are five operation modes: single port, dual port, semi-dual port, ROM, and FIFO. The signals and functional descriptions of B-SRAM are listed in the following table.

An abundance of B-SRAM resources provide a guarantee for the user's high-performance design. B-SRAM features include the following:

- Max. 18,432 bits per B-SRAM
- B-SRAM itself can run at 380 MHz at max (typical, Read-before-write is 230MHz)
- Single port
- Dual port
- Semi-dual port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode

- Enable Byte operation for double byte or above
- Normal read and write mode
- Read-before-write mode
- Write-through mode

Table 3-4 B-SRAM Signals

Port Name	I/O	Description
DIA	I	Port A data input
DIB	I	Port B data input
ADA	I	Port A address
ADB	I	Port B address
CEA	I	Clock enable, Port A
CEB	I	Clock enable, Port B
RESETA	I	Register reset, Port A
RESETB	I	Register reset, Port B
WREA	I	Read/write enable, Port A
WREB	I	Read/write enable, Port B
BLKSELA, BLKSELB	I	Block select
CLKA	I	Read/write cycle clock for Port A input registers
CLKB	I	Read/write cycle clock for Port B input registers
OCEA	I	Clock enable for Port A output registers
OCEB	I	Clock enable for Port B output registers
DOA	O	Port A data output
DOB	O	Port B data output

3.4.2 Configuration Mode

The B-SRAM mode in the GW2A series of FPGA products supports different data bus widths. See Table 3-5.

Table 3-5 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Single Port Mode

In the single port mode, B-SRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of B-SRAM. Normal-Write Mode and Write-through Mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge.

For further information about Single Port Block Memory ports and the related description, please refer to [SUG283E, Gowin Primitives User Guide](#) > 3 Memory.

Dual Port Mode

B-SRAM support dual port mode. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

For further information about Dual Port Block Memory ports and the related description, please refer to [SUG283E, Gowin Primitives User Guide](#) > 3 Memory.

Semi-Dual Port Mode

Semi-Dual Port supports read and write at the same time on different ports, but it is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

For further information about Semi-Dual Port Block Memory ports and the related description, please refer to [SUG283E, Gowin Primitives User Guide](#) > 3 Memory.

Read Only

B-SRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each B-SRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to [SUG283E, Gowin Primitives User Guide](#) > 3 Memory.

3.4.3 Mixed Data Bus Width Configuration

The B-SRAM in the GW2A series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-6 and Table 3-7 below.

Table 3-6 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

“*” denotes the modes supported.

Table 3-7 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x32	2K x 9	1K x 18	512x36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

“*” denotes the modes supported.

3.4.4 Byte-enable

The B-SRAM in the GW2A series of FPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the B-SRAM write operation.

3.4.5 Parity Bit

There are parity bits in B-SRAM. The 9th bit in each byte can be used as a parity bit or for data storage. However, the parity operation is not yet supported.

3.4.6 Synchronous Operation

- All the input registers of B-SRAM support synchronous write.
- The output register can be used as a pipeline register to improve design performance.
- The output registers are bypass-able.

3.4.7 Power up Conditions

B-SRAM initialization is supported when powering up. During the power-up process, B-SRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

3.4.8 B-SRAM Operation Modes

B-SRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the B-SRAM via output registers or without using the registers.

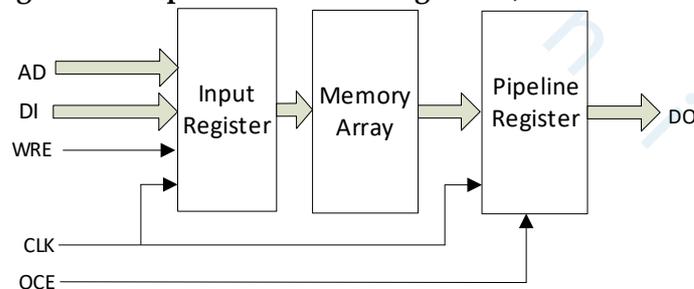
Pipeline Mode

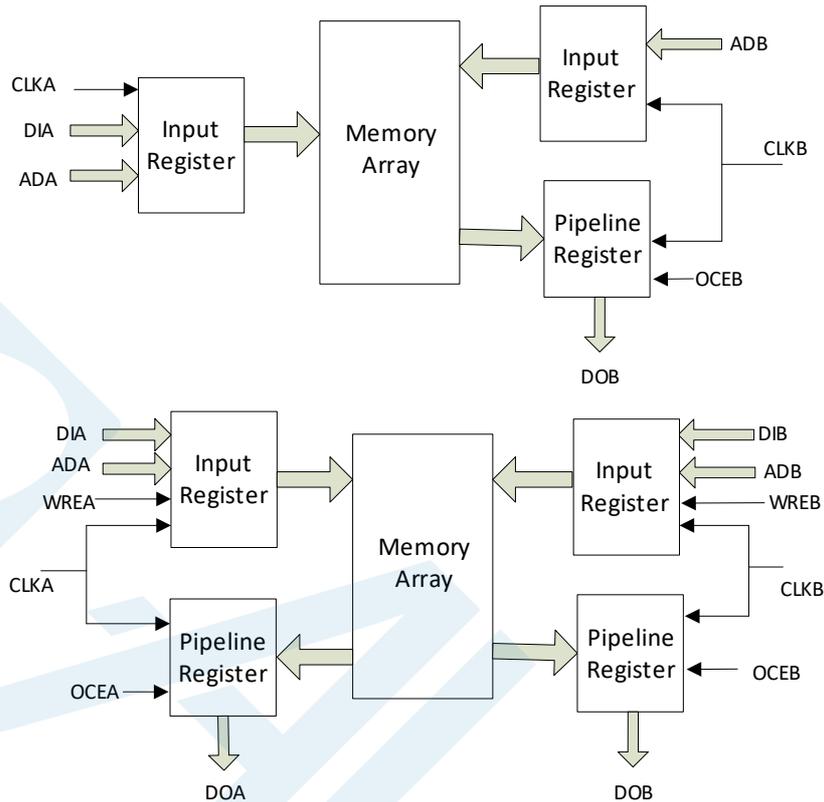
While writing in the B-SRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register is not used. The data is kept in the output of the memory array.

Figure 3-29 Pipeline Mode in Single Port, Dual Port and Semi-Dual Port





Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

3.4.9 Clock Operations

Table 3-8 lists the clock operations in different B-SRAM modes:

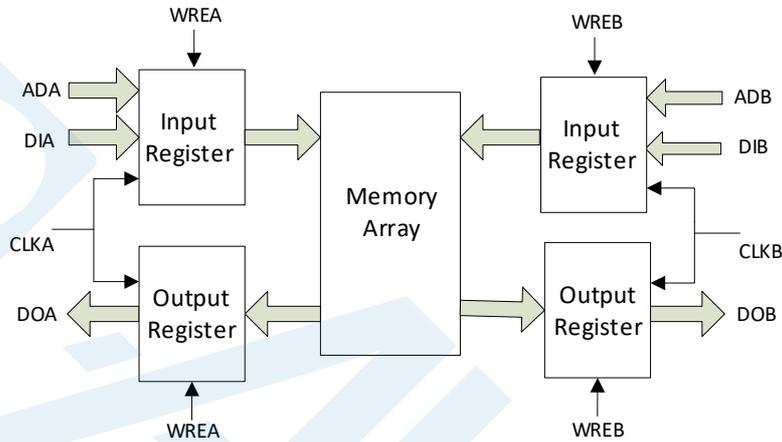
Table 3-8 Clock Operations in Different B-SRAM Modes

Clock Operations	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-30 shows the independent clocks in the dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

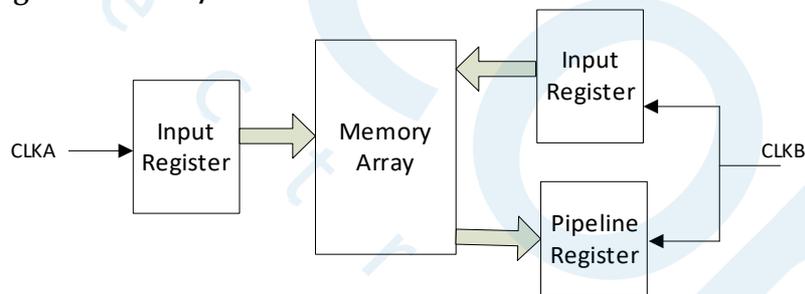
Figure 3-30 Independent Clock Mode



Read/Write Clock Operation

Figure 3-31 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

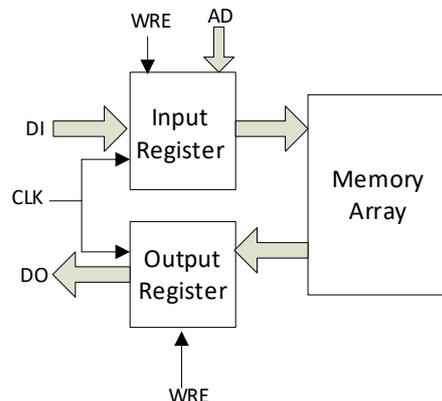
Figure 3-31 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-32 shows the clock operation in single port mode.

Figure 3-32 Single Port Clock Mode



3.5 DSP

3.5.1 Introduction

The GW2A series of FPGA products have abundant DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP offers the following functions:

- Multiplier with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

Macro

DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one 3 input ALU.

Figure 3-33 shows the structure of one Macro:

Figure 3-33 DSP Macro

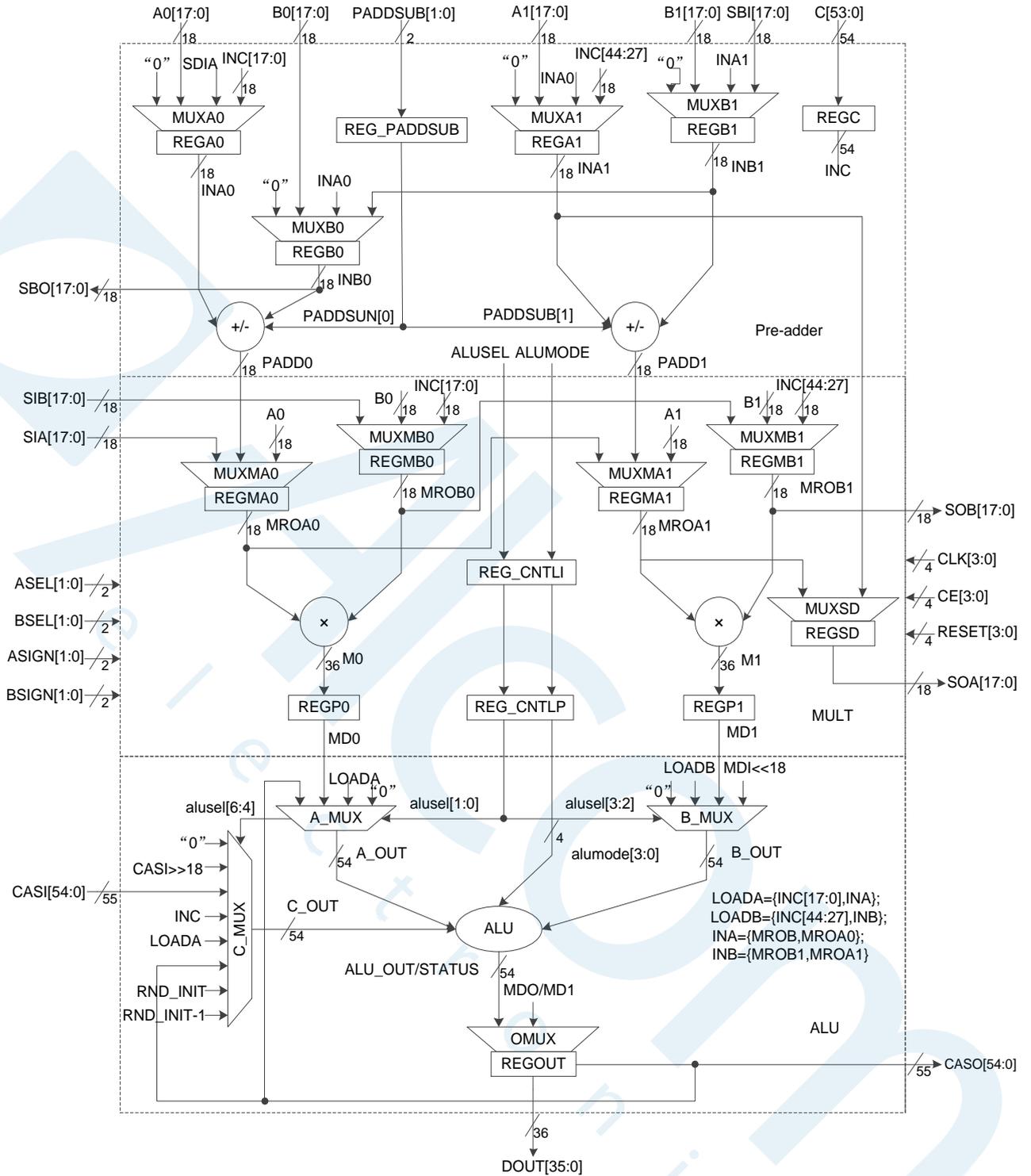


Table 3-9 shows DSP ports description.

Table 3-10 shows internal registers.

Table 3-9 DSP Ports Description

Port Name	I/O	Description
A0[17:0]	I	18-bit data input A0
B0[17:0]	I	18-bit data input B0
A1[17:0]	I	18-bit data input A1

Port Name	I/O	Description
B1[17:0]	I	18-bit data input B1
C[53:0]	I	54-bit data input C
SIA[17:0]	I	Shift data input A, used for CASCADE connection. The input signal SIA is directly connected to the output signal SOA of previously adjacent DSP and the delay from SIA to SOA inside a DSP is one clock cycle.
SIB[17:0]	I	Shift data input B, used for CASCADE connection. The input signal SIB is directly connected to the output signal SOB of previously adjacent DSP and the delay from SIB to SOB inside a DSP is one clock cycle.
SBI[17:0]	I	Pre - adder logic shift input, backward direction.
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection.
PADDSI0[1:0]	I	Source select for Multiplier or pre-adder input A
BSEL[1:0]	I	Source select for Multiplier input B
ASIGN[1:0]	I	Sign bit for input A
BSIGN[1:0]	I	Sign bit for input B
PADDSUB[1:0]	I	Operation control signals of pre-adder, used for pre-adder logic add/subtract selection
CLK[3:0]	I	Clock input
CE[3:0]	I	Clock Enable
RESET[3:0]	I	Reset input, synchronous or asynchronous
SOA[17:0]	O	Shift data output A
SOB[17:0]	O	Shift data output B
SBO[17:0]	O	Pre - adder logic shift output, backward direction.
DOUT[35:0]	O	DSP output data
CASO[54:0]	O	ALU output to next DSP block for cascade connection, the highest bit is sign-extended.

Table 3-10 Internal Registers Description

Register	Description and Associated Attributes
A0 register	Registers for A0 input
A1 register	Registers for A1 input
B0 register	Registers for B0 input
B1 register	Registers for B1 input
C register	C register
P1_A0 register	Registers for A0 input of left multiplier
P1_A1 register	Registers for A1 input of right multiplier
P1_B0 register	Registers for B0 input of left multiplier
P1_B1 register	Registers for B1 input of right multiplier
P2_0 register	Registers for pipeline of left multiplier
P2_1 register	Registers for pipeline of right multiplier
OUT register	Registers for DOUT output
OPMODE register	Registers for operation mode control
SOA register	Registers for shift output at port SOA

PADD

Each DSP macro features two units of pre-adders to implement

pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs.,

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.

Each input end supports pipeline mode and bypass mode.

GOWINSEMI PADD can be used as function block independently, which supports 9-bit and 18-bit width.

MULT

Multipliers locate after the pre-adder. Multipliers can be configured as 9 x 9, 18 x 18, 36 x 18 or 36 x 36. Pipeline Mode and Bypass Mode are supported both in input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Two adjacent DSP macros can form a 36 x 36 multiplier.

ALU

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. The registered and bypass mode are supported both in input and output ports. The functions are as following:

- Multiplier output data / 0, addition/subtraction operations for data A and data B;
- Multiplier output data / 0, addition/subtraction operations for data B and bit C;
- Addition/subtraction operations for data A, data B, and bit C;

3.5.2 DSP Operations

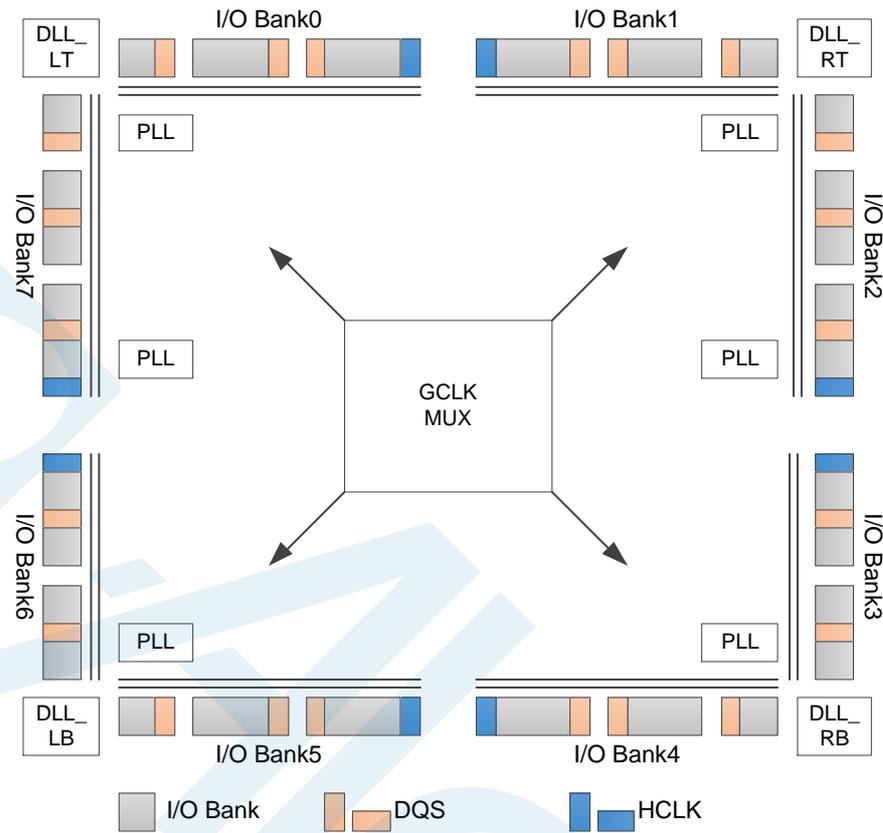
Based on ALUSEL [6:0] and ALUMODE [3:0], DSP can be configured as different operation modes: Operation Mode:

- Multiplier
- Accumulator
- MULTADDALU

3.6 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. The GW2A series of FPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW2A series of FPGA products provide PLL, high speed clock HCLK, DDR memory interface, DQS, etc.

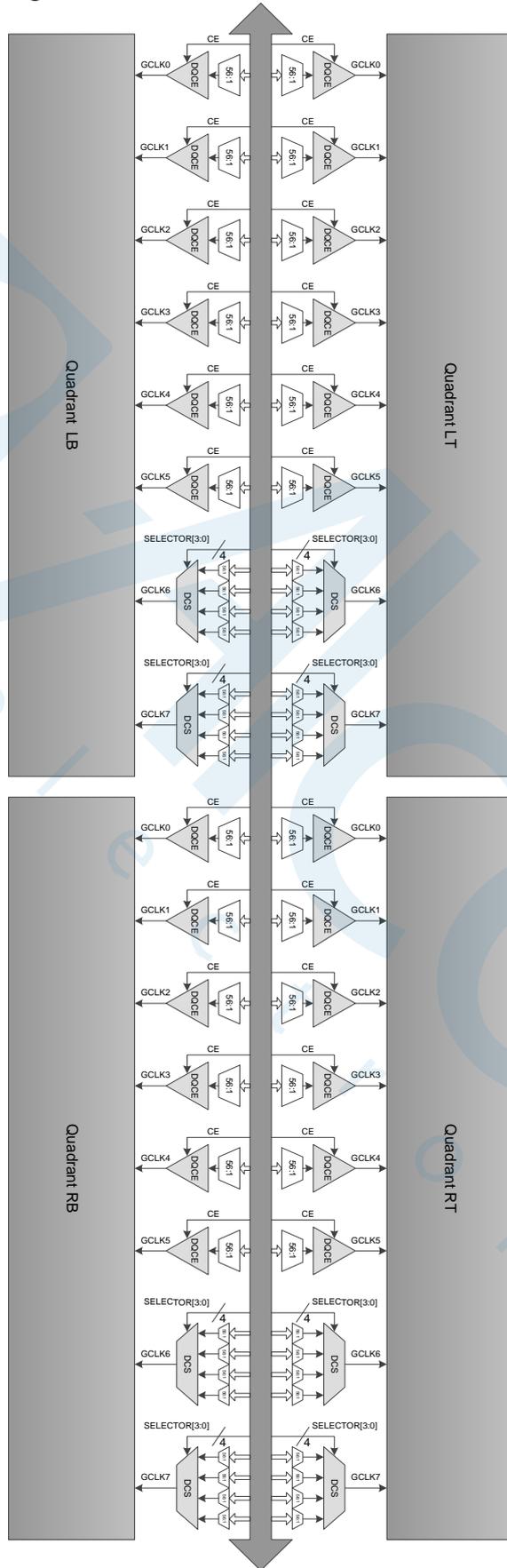
Figure 3-34 GW2A Clock Resources



3.6.1 Global Clock

GCLK is distributed in the GW2A devices as four quadrants. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

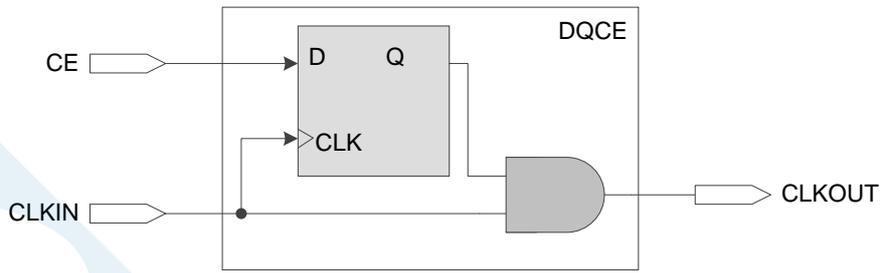
Figure 3-35 GCLK Quadrant Distribution



GCLK0~GCLK5 can be turned on or off by Dynamic Quad Clock

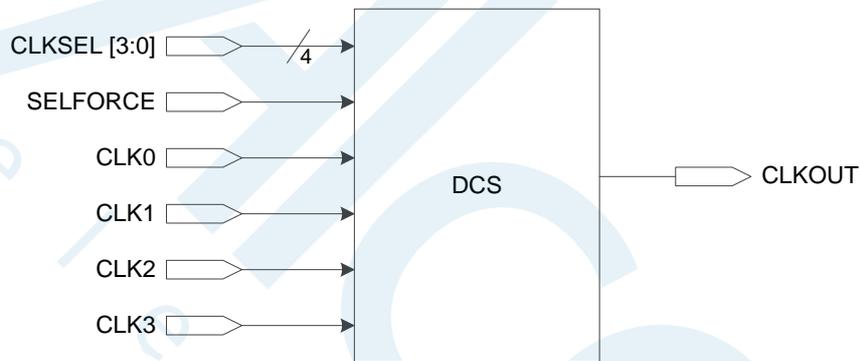
Enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

Figure 3-36 DQCE Concept



GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-37. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

Figure 3-37 DCS Concept

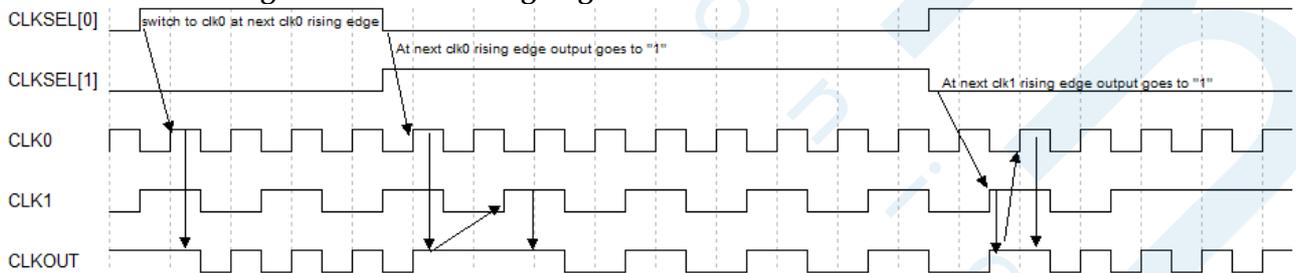


DCS can be configured in the following modes:

- DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-38.

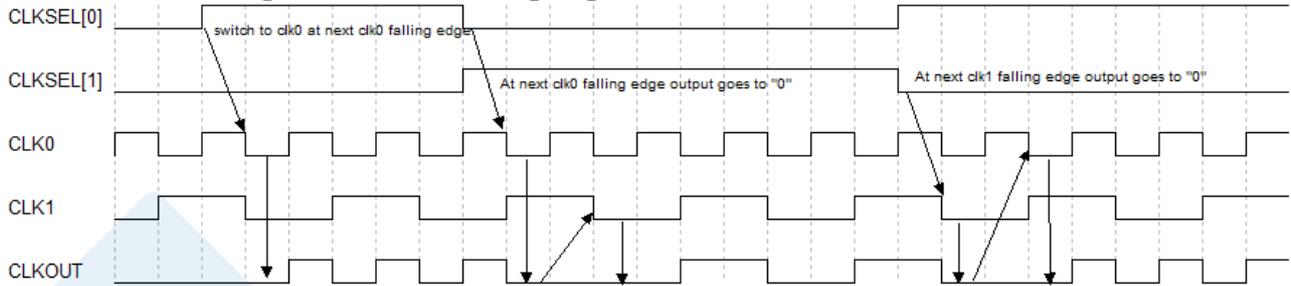
Figure 3-38 DCS Rising Edge



- DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-39.

Figure 3-39 DCS Falling Edge



- **Clock Buffer Mode**

In this mode, DCS acts as a clock buffer.

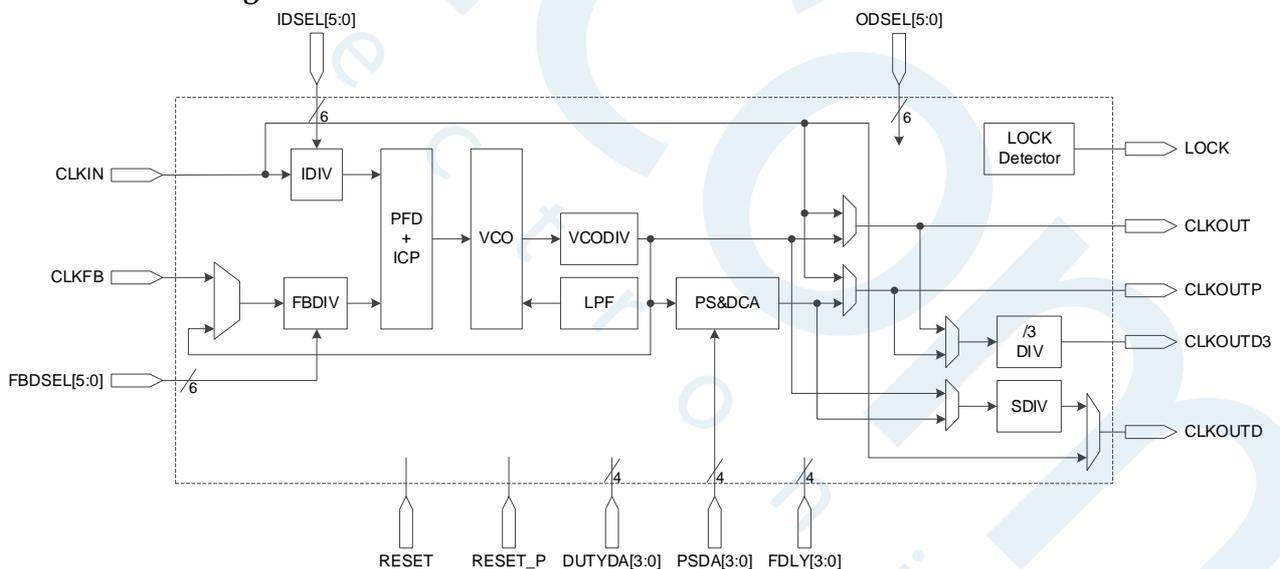
3.6.2 PLL

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks in the GW2A series of FPGA products provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-40 for the PLL structure.

Figure 3-40 PLL Structure



See Table 3-11 for a definition of the PLL ports.

Table 3-11 PLL Ports Definition

Port Name	Signal	Description
CLKIN [5:0]	I	Reference clock input
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
INSEL[2:0]	I	Dynamic clock control selector: 0~5

Port Name	Signal	Description
IDSEL [5:0]	I	Dynamic IDIV control: 1~64
FBDSEL [5:0]	I	Dynamic FBDIV control:1~64
PSDA [3:0]	I	Dynamic phase control (rising edge effective)
DUTYDA [3:0]	I	Dynamic duty cycle control (falling edge effective)
FDLY[3:0]	I	CLKOUTP dynamic delay control
CLKOUT	O	Clock output with no phase and duty cycle adjustment
CLKOUTP	O	Clock output with phase and duty cycle adjustment
CLKOUTD	O	Clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	O	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	O	PLL lock status: 1 locked, 0 unlocked

The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

For further PLL features, please refer to [4.4.6 PLL Switching Characteristic](#).

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

1. $f_{\text{CLKOUT}} = (f_{\text{CLKIN}} * \text{FBDIV}) / \text{IDIV}$
2. $f_{\text{VCO}} = f_{\text{CLKOUT}} * \text{ODIV}$
3. $f_{\text{CLKOUTD}} = f_{\text{CLKOUT}} / \text{SDIV}$
4. $f_{\text{PFD}} = f_{\text{CLKIN}} / \text{IDIV} = f_{\text{CLKOUT}} / \text{FBDIV}$

Note!

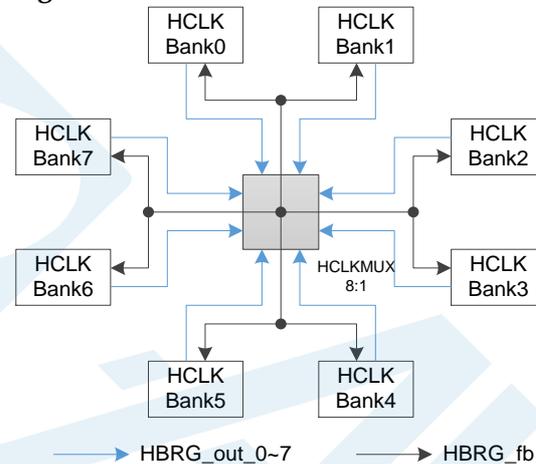
- f_{CLKIN} : The frequency of the input clock CLKIN
- f_{CLKOUT} : The clock frequency of CLKOUT and CLKOUTP
- f_{CLKOUTD} : The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- f_{PFD} : PFD Phase Comparison Frequency, and the minimum value of f_{PFD} should be no less than 3MHz

Adjust IDIV, FBDIV, ODIV, and SDIV to achieve the required clock frequency.

3.6.3 HCLK

HCLK is the high-speed clock in the GW2A series FPGA products, which can support high-speed data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure 3-41.

Figure 3-41 GW2A HCLK Distribution



As shown in Figure 3-41, there is an 8: 1 HCLKMUX module in the middle of the high-speed clock HCLK. HCLKMUX can send HCLK clock signal from any Bank to any other bank, which makes the use of HCLK more flexible.

HCLK can provide user with the function modules as follows:

- DHCEN: Dynamic high-speed clock enable module, functions similar to DQCE. Dynamically turn on / off high-speed clock signal.
- CLKDIV/ CLKDIV2: high-speed clock divider module, each bank has a CLKDIV. Generates a clock divided by the input clock phase, which is used in the IO logic mode.
- DCS: Dynamic High Speed Clock Selector.
- DLLDLY: The dynamic delay adjustment module, the clock signal for the dedicated clock pin input.

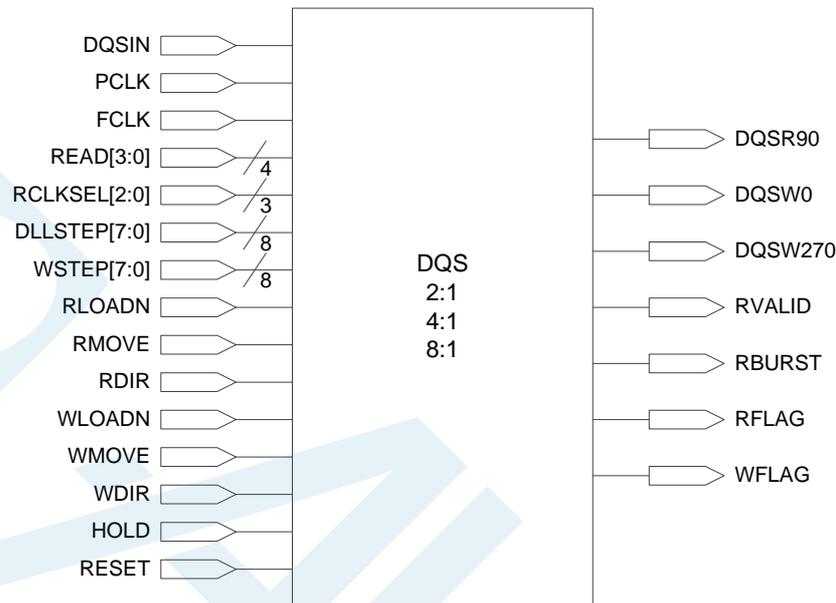
3.6.4 DDR Memory Interface Clock Management DQS

The DQS module of the GW2A series of FPGA products provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase
- Provide a read / write pointer for input cache
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module has three operating modes to meet the needs of different I/O interfaces, as shown in Figure 3-42.

Figure 3-42 DQS



CDRCLKGEN

CDRCLKGEN is used to support high-speed asynchronous input interfaces, such as SGMII. Each location has only one DQS and CDRCLKGEN.

CDRCLKDIV

The function of the clock divider module is similar to that of HCLKDIV.

3.7 Long Wire (LW)

As a supplement to the CRU, the GW2A series of FPGA products provide another routing resource - Long Wire, which can be used as clock, clock enable, set/reset, or other high fan out signals.

3.8 Global Set/Reset (GSR)

A global set/reset (GSR) network is built into the GW2A series of FPGA products. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

3.9 Programming Configuration

The GW2A series of FPGA products support SRAM. Each time the device is powered on, it needs to download the bit stream file to configure. Users can select to keep backup data in external Flash chip according to requirements. After power-up, the GW2A devices read configuration data

from external Flash into the SRAM.

Besides JTAG, the GW2A series of FPGA products also support GOWINSEMI's own configuration mode: GowinCONFIG (SSPI, MSPI, SERIAL, and CPU). For more detailed information, please refer to [UG290, Gowin FPGA Products Programming and Configuration User Guide](#).

3.10 On Chip Oscillator

There is an internal oscillator in each of the GW2A series of FPGA product. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-12 for the output frequency. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is employed to get the output clock frequency:

$$f_{\text{out}}=250 \text{ MHz/Param}$$

Note!

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

Table 3-12 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz ¹	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz ²

Note!

- [1] Default Frequency is 2.5 MHz.
- [2] 125 MHz is not suitable for MSPI.

4 AC/DC Characteristic

Note!

Users should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

4.1 Operating Conditions

4.1.1 Absolute Max. Ratings

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V _{CC}	Core voltage	-0.5V	1.1V
V _{CCPLL}	PLL Power	-0.5V	1.1V
V _{CCO}	I/O Bank Power	-0.5V	3.75V
V _{CCX}	Auxiliary voltage	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65 °C	+150 °C
Junction Temperature (Industrial)	Junction Temperature	-40 °C	+125 °C

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V _{CC}	Core voltage.	0.95V	1.05V
V _{CCPLLX}	Left PLL power supply	0.95V	1.05V
V _{CCPLLRX}	Right PLL power supply	0.95V	1.05V
V _{CCO}	I/O Bank Power	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.7V	3.465V
T _{JCOM}	Junction temperature of commercial operation	0 °C	+85 °C
T _{JIND}	Junction temperature of Industrial operation	-40 °C	+100 °C
T _{JAUT}	Junction temperature of Automotive operation	-40°C	+105°C

Note!

For the detailed recommended operating conditions for different packages, please refer to [UG110, GW2A-18 Pinout](#) and [UG113, GW2A-55 Pinout](#).

4.1.3 Power Supply Ramp Rates

Table 4-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
T _{RAMP}	Power supply ramp rates for all power supplies	0.01mV/μs	-	10mV/μs

4.1.4 Hot Socket Specifications

Table 4-4 Hot Socket Specifications

Name	Description	Condition	I/O	Max.
I _{HS}	Input leakage current (Input or I/O leakage current)	V _{IN} =V _{IL} (MAX)	I/O	150uA
I _{HS}	Input leakage current (Input or I/O leakage current)	V _{IN} =V _{IL} (MAX)	TDI, TDO TMS, TCK	120uA

4.1.5 POR Specifications

Table 4-5 POR Specifications

Name	Description	Min.	Max.
POR Voltage	Power on reset voltage of V _{CC}	0.65V	0.85V

4.2 ESD

Table 4-6 GW2A ESD - HBM

Device	GW2A-18	GW2A-55
QN88	HBM>1,000V	-
LQ144	HBM>1,000V	-
EQ144	HBM>1,000V	-
MG196	HBM>1,000V	-
PG256	HBM>1,000V	-
PG256S	HBM>1,000V	-
PG256C	HBM>1,000V	-
PG256E	HBM>1,000V	-
PG484	HBM>1,000V	HBM>1,000V
PG1156	-	HBM>1,000V
UG324	HBM>1,000V	HBM>1,000V
UG324D	-	HBM>1,000V
UG676	-	HBM>1,000V

Table 4-7 GW2A ESD - CDM

Device	GW2A-18	GW2A-55
QN88	CDM>500V	-
LQ144	CDM>500V	-
EQ144	CDM>500V	-
MG196	CDM>500V	-
PG256	CDM>500V	-
PG256S	CDM>500V	-
PG256C	CDM>500V	-
PG256E	CDM>500V	-
PG484	CDM>500V	CDM>500V
PG1156	-	CDM>500V
UG324	CDM>500V	CDM>500V
UG324D	-	CDM>500V
UG676	-	CDM>500V

4.3 DC Electrical Characteristics

4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I _{IL} , I _{IH}	Input or I/O leakage	V _{CCO} < V _{IN} < V _{IH} (MAX)	-	10uA	-
		0V < V _{IN} < V _{CCO}	-	0.01uA	-
I _{PU}	I/O Active Pull-up Current	0 < V _{IN} < 0.7V _{CCO}	-	-100uA	-
I _{PD}	I/O Active Pull-down Current	V _{IL} (MAX) < V _{IN} < V _{CCO}	-	100uA	-
C1	I/O Capacitance			5pF	8pF
V _{HYST}	Hysteresis for Schmitt Trigger inputs	V _{CCO} =3.3V, Hysteresis=L2H	-	240mV	-
		V _{CCO} =2.5V, Hysteresis=L2H	-	140mV	-
		V _{CCO} =1.8V, Hysteresis=L2H	-	65mV	-
		V _{CCO} =1.5V, Hysteresis=L2H	-	30mV	-
		V _{CCO} =3.3V, Hysteresis=H2L	-	200mV	-
		V _{CCO} =2.5V, Hysteresis=H2L	-	130mV	-
		V _{CCO} =1.8V, Hysteresis=H2L	-	60mV	-
		V _{CCO} =1.5V, Hysteresis=H2L	-	40mV	-
		V _{CCO} =3.3V, Hysteresis=High	-	440mV	-
		V _{CCO} =2.5V, Hysteresis=High	-	270mV	-
		V _{CCO} =1.8V, Hysteresis=High	-	125mV	-
		V _{CCO} =1.5V, Hysteresis=High	-	70mV	-

4.3.2 Static Supply Current

Table 4-9 Static Supply Current

Name	Description	LV/UV	Device	Typ.
I _{CC}	Core Current	LV	GW2A-55	100mA
			GW2A-18	35mA
I _{CCX}	V _{CCX} current (V _{CCX} =2.5V)	LV	GW2A-55	30mA
I _{CCO}	I/O Bank current (V _{CCO} =2.5V)	LV	GW2A-55	70uA

4.3.3 I/O Operating Conditions Recommended

Table 4-10 I/O Operating Conditions Recommended

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Note!

It is recommended to set the VCCO of the Bank using TrueLVDS to 2.5V.

4.3.4 IOB Single - Ended DC Electrical Characteristic

Table 4-11 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	$V_{CCO}-0.4V$	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	$V_{CCO}-0.2V$	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	$V_{CCO}-0.4V$	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	$V_{CCO}-0.2V$	0.1	-0.1
LVCMOS18	-0.3V	$0.35 \times V_{CCO}$	$0.65 \times V_{CCO}$	3.6V	0.4V	$V_{CCO}0.4V$	4	-4
							8	-8
					0.2V	$V_{CCO}-0.2V$	12	-12
							0.1	-0.1
LVCMOS15	-0.3V	$0.35 \times V_{CCO}$	$0.65 \times V_{CCO}$	3.6V	0.4V	$V_{CCO}-0.4V$	4	-4
							8	-8
					0.2V	$V_{CCO}-0.2V$	0.1	-0.1
LVCMOS12	-0.3V	$0.35 \times V_{CCO}$	$0.65 \times V_{CCO}$	3.6V	0.4V	$V_{CCO}-0.4V$	2	-2
							4	-4
					0.2V	$V_{CCO}-0.2V$	0.1	-0.1
PCI33	-0.3V	$0.3 \times V_{CCO}$	$0.5 \times V_{CCO}$	3.6V	$0.1 \times V_{CCO}$	$0.9 \times V_{CCO}$	1.5	-0.5
SSTL33_I	-0.3V	$V_{REF}-0.2V$	$V_{REF}+0.2V$	3.6V	0.7	$V_{CCO}-1.1V$	8	-8
SSTL25_I	-0.3V	$V_{REF}-0.18V$	$V_{REF}+0.18V$	3.6V	0.54V	$V_{CCO}-0.62V$	8	-8
SSTL25_II	-0.3V	$V_{REF}-0.18V$	$V_{REF}+0.18V$	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	$V_{REF}-0.125V$	$V_{REF}+0.125V$	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	$V_{REF}-0.125V$	$V_{REF}+0.125V$	3.6V	0.40V	$V_{CCO}-0.40V$	8	-8
SSTL15	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	0.40V	$V_{CCO}-0.40V$	8	-8
HSTL18_I	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	0.40V	$V_{CCO}-0.40V$	8	-8
HSTL18_II	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	0.40V	$V_{CCO}-0.40V$	8	-8
HSTL15_II	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	NA	NA	NA	NA

4.3.5 IOB Differential Electrical Characteristics

Table 4-12 IOB Differential Electrical Characteristics
LVDS

Name	Description	Condition	Min.	Typ.	Max.	Unit
V_{INA}, V_{INB}	Input Voltage (Input Voltage)		0	-	2.4	V
V_{CM}	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	± 100	-	-	mV
I_{IN}	Input Current	Power On or Power Off	-	-	± 10	μA
V_{OH}	Output High Voltage for VOP or VOM	$R_T = 100\Omega$	-	-	1.60	V
V_{OL}	Output High Voltage for VOP or VOM	$R_T = 100\Omega$	0.9	-	-	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100\Omega$	250	350	450	mV
ΔV_{OD}	Change in VOD Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100\Omega$	1.125	1.20	1.375	V
ΔV_{OS}	Change in VOS Between High and Low		-	-	50	mV
I_S	Short-circuit current	$V_{OD} = 0V$ output short-circuit	-	-	15	mA

4.4 Switching Characteristic

4.4.1 Internal Switching Characteristics

Table 4-13 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.337	ns
t_{LUT5_CFU}	LUT5 delay	-	0.694	ns
t_{LUT6_CFU}	LUT6 delay	-	1.005	ns
t_{LUT7_CFU}	LUT7 delay	-	1.316	ns
t_{LUT8_CFU}	LUT8 delay	-	1.627	ns
t_{SR_CFU}	Set/Reset to Register output	-	0.93	ns
t_{CO_CFU}	Clock to Register output	-	0.38	ns

4.4.2 B-SRAM Internal Timing Parameters

Table 4-14 B-SRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	2.55	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.28	ns

4.4.3 DSP Internal Timing Parameters

Table 4-15 DSP Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COIR_DSP}	Clock to output from input register	-	2.40	ns
t_{COPR_DSP}	Clock to output from pipeline register	-	1.20	ns
t_{COOR_DSP}	Clock to output from output register	-	0.42	ns

4.4.4 External Switching Characteristics

Table 4-16 External Switching Characteristics

Name	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

4.4.5 On chip Oscillator Output Frequency

Table 4-17 On chip Oscillator Output Frequency

Name	Description	Min.	Typ.	Max.
f _{MAX}	Output Frequency (0 to 85°C)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100°C)	100MHz	125MHz	150MHz
t _{DT}	Output Clock Duty Cycle	43%	50%	57%
t _{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

4.4.6 PLL Switching Characteristic

Table 4-18 PLL Switching Characteristic

Device	Speed Grade	Name	Min.	Max.
GW2A-18	C9/18 C8/17 A6	CLKIN	3MHZ	500MHZ
		PFD	3MHZ	500MHZ
		VCO	500MHZ	1250MHZ
		CLKOUT	3.90625MHZ	625MHZ
	C7/16	CLKIN	3MHZ	400MHZ
		PFD	3MHZ	400MHZ
		VCO	400MHZ	1000MHZ
		CLKOUT	3.125MHZ	500MHZ
GW2A-55	C9/18 C8/17 A6	CLKIN	3MHZ	500MHZ
		PFD	3MHZ	500MHZ
		VCO	500MHZ	1250MHZ
		CLKOUT	3.90625MHZ	625MHZ

Device	Speed Grade	Name	Min.	Max.
	C7/I6	CLKIN	3MHZ	400MHZ
		PFD	3MHZ	400MHZ
		VCO	400MHZ	1000MHZ
		CLKOUT	3.125MHZ	500MHZ

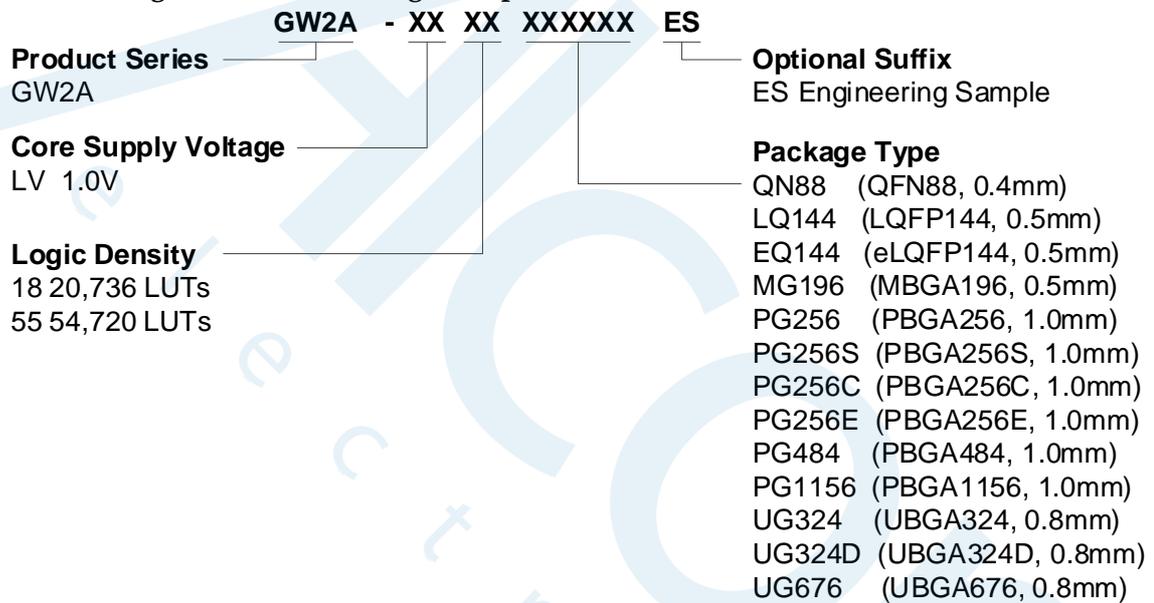
4.5 Configuration Interface Timing Specification

The GW2A series of FPGA products GowinCONFIG support the following configuration modes: MSPI, SSPI, CPU, and SERIAL. For detailed information, please refer to UG290, *Gowin FPGA Products Programming and Configuration User Guide*.

5 Ordering Information

5.1 Part Name

Figure 5-1 Part Naming Example- ES





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