GOWIN
PROGRAMMING FOR THE FUTURE

GW5AT series of FPGA Products

Package & Pinout User Guide

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Revision History

Date	Version	Description
04/20/2023	1.0E	Initial version published.
05/25/2023	1.1E	The info. of PG484 package added.
07/06/2023	1.1.1E	The info. of PG676A package added.
09/08/2023	1.1.2E	The info. of UG324 package added.
11/30/2023	1.1.3E	● The info. of UG324A package added. ● “Table 2-1 Package, Max. User I/O Information, and LVDS Pairs” in “2 Overview” optimized.
02/02/2022	1.1.4E	● The info. of UG484 package for GW5AT-75 devices added. ● The IO info. of all packages updated.
03/29/2024	1.1.5E	The info. of PG484A and UG225 packages for GW5AT-60 devices added.
06/28/2024	1.1.6E	● The names of voltage pins updated. ● The info. of UG324 package for GW5AT-138 devices removed. ● The info. of UG324S package for GW5AT-60 devices added.

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1 About This Guide

1.1 Purpose

This manual introduces Gowin GW5AT series of FPGA products package and provides pin definitions, lists of pin numbers, pin distribution views, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1225, Arora V 60K FPGA Products Data Sheet
- DS981, Arora V 138K & 75K FPGA Products Data Sheet
- UG982, GW5AT-138 Pinout
- UG1221, GW5AT-75 Pinout
- UG1222, GW5AT-60 Pinout

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPG	FCPBGA Package
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
PG	PBGA Package
UG	UBGA Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin GW5AT series of FPGA products are the fifth generation of Arora family with abundant internal resources, a new-architecture and high-performance DSP supporting AI operations, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, GW5AT series integrate self-developed DDR3, 12.5Gbps SerDes supporting multiple protocols, and provide a variety of packages. They are suitable for applications such as low power, high performance and compatibility design.

Gowin provides a new generation of FPGA hardware development environment that supports GW5AT series of products, capable of fulfilling one-stop work such as FPGA synthesis, placement & routing, bitstream generation and download, etc.

2.1 PB-Free Package

GW5AT series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW5AT series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Pairs

Package			Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5AT-60	GW5AT-75	GW5AT-138
Name	Type	Description						
FPG676A	FCPBGA	Flip Chip	1.0	27x27	-	-	-	311 (150)
PG484	PBGA	Wire Bond	1.0	23x23	-	-	-	271 (133)
PG484A	PBGA	Wire Bond	1.0	23x23	-	297 (143)	-	291 (143)
PG676A	PBGA	Wire Bond	1.0	27x27	-	-	-	311 (150)
UG225	UBGA	Wire Bond	0.8	13x13	-	113 (53)	-	-
UG324A	UBGA	Wire Bond	0.8	15x15	-	-	-	141 (68)
UG324S	UBGA	Wire Bond	0.8	15x15	-	198(98)	-	-
UG484	UBGA	Wire Bond	0.8	19x19	-	-	311 (150)	-

2.3 Power Pins

Table 2-2 GW5AT Power Pins

VDD12_MIPI	VDDA_MIPI	VDDD_MIPI	VDDX_MIPI
VDDA_Q0	VDDA_Q1	VDDHA_Q0	VDDHA_Q1
VDDT_Q0	VDDT_Q1	VDDT_Q1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCIO6
VCCIO7	VCCIO8	VCCIO9	VCCIO10
VCCIO11	VCCIO12	VCC	VCCX
VREFP	VREFN	V_EFUSE	VCC_ADC
VCC_LDO			

2.4 Pin Quantity

2.4.1 Quantity of GW5AT-138 Pins

Table 2-3 Quantity of GW5AT-138 Pins

Pin Type		GW5AT-138				
		FPG676A (Flip Chip)	PG484A	PG484	PG676A	UG324A
Single-ended IO/Differential Pair/LVDS[1]	BANK0	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0
	BANK1	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0
	BANK2	50/24/24	50/24/24	50/24/24	50/24/24	25/12/12
	BANK3	50/24/24	50/24/24	50/24/24	50/24/24	25/12/12
	BANK4	50/24/24	50/24/24	50/24/24	50/24/24	50/24/24
	BANK5	50/24/24	35/17/17	35/17/17	50/24/24	13/6/6
	BANK6	50/24/24	50/24/24	50/24/24	50/24/24	13/6/6
	BANK7	50/24/24	50/24/24	30/14/14	50/24/24	4/2/2
	BANK10	12/6/6	12/6/6	12/6/6	12/6/6	12/6/6

Pin Type	GW5AT-138				
	FPG676A (Flip Chip)	PG484A	PG484	PG676A	UG324A
Max. User I/O[2]	311	296	276	311	141
Differential Pair	150	143	133	150	68
True LVDS Output	150	143	133	150	68
VCCIO0	0	0	0	0	0
VCCIO1	0	0	0	0	0
VCCIO2	6	6	6	6	4
VCCIO3	6	6	6	6	3
VCCIO4	6	6	6	6	7
VCCIO5	6	5	5	6	2
VCCIO6	6	6	6	6	2
VCCIO7	6	6	6	6	2
VCCIO10	2	2	2	2	2
VCCX	3	3	3	3	3
VCC	13	14	14	13	18
VCC_LDO	6	6	6	6	1
VDDHA _Q1	1	1	0	0	0
VDDHA_Q0	1	1	2	0	1
VDDHA_Q0/VDDHA_Q1	0	0	0	2	0
VDDA_Q1/VDDD_Q1	3	0	0	0	0
VDDA_Q0/VDDD_Q0	3	0	0	0	0
VDDA_Q0	0	3	3	3	2
VDDA_Q1	0	0	0	3	0
VDDT_Q1	2	0	0	2	0
VDDT_Q0	2	2	2	2	2
VDDA_MIPI	0	0	0	2	0
VDDD_MIPI	0	0	0	2	0
VDDX_MIPI	1	0	1	1	1
VDDA_MIPI/VDDD_MIPI	4	0	2	0	3
VSS	120	88	88	120	76
MODE0	1	1	1	1	1
MODE1	1	1	1	1	1
MODE2	1	1	1	1	1
NC	102	8	5	103	9

Note!

- [1] Single-ended/Differential I/O quantity includes CLK pins and download pins.
- [2] RECONFIG_N pin cannot be multiplexed as I/O.

2.4.2 Quantity of GW5AT-75 Pins

Table 2-4 Quantity of GW5AT-75 Pins

Pin Type		GW5AT-75
		UBGA484
Single-ended IO/Differential Pair/LVDS[1]	BANK0	0/0/0
	BANK1	0/0/0
	BANK2	50/19/19
	BANK3	50/19/19
	BANK4	50/0/0
	BANK5	50/20/20
	BANK6	50/19/19
	BANK7	50/18/18
	BANK10	11/0/0
Max. User I/O[2]		311
Differential Pair		150
True LVDS Output		150
VCCIO2		3
VCCIO3		4
VCCIO4		4
VCCIO5		5
VCCIO6		3
VCCIO7		3
VCCIO10		2
VCCIO11/VCCX/VDDX_MIPI		2
VCC		12
VCC_LDO		3
VDDA_MIPI/VDDD_MIPI		2
VDDA_Q0		2
VDDHA_Q0/VDDHA_Q1		2
VDDT_Q0		3
VDDA_Q1		2
VDDT_Q1		3
VSS		52
MODE0		1
MODE1		1
MODE2		1
NC		1

Note!

- [1] Single-ended/Differential I/O quantity includes CLK pins and download pins.

- [2] RECONFIG_N pin cannot be multiplexed as I/O.

2.4.3 Quantity of GW5AT-60 Pins

Table 2-5 Quantity of GW5AT-60 Pins

Pin Type		GW5AT-60		
		PBGA484A	UBGA324S	UBGA225
Single-ended IO/Differential Pair/LVDS[1]	BANK0	0/0/0	0/0/0	0/0/0
	BANK1	25/12/12	34/17/17	8/4/4
	BANK2	26/12/12	22/11/11	6/3/3
	BANK3	8/4/4	14/7/7	8/4/4
	BANK4	16/8/8	16/8/8	6/3/3
	BANK5	34/16/16	34/16/16	20/9/9
	BANK6	20/10/10	0/0/0	0/0/0
	BANK7	24/12/12	0/0/0	0/0/0
	BANK8	24/12/12	0/0/0	16/8/8
	BANK9	66/33/33	56/28/28	36/18/18
	BANK10	25/12/12	8/4/4	5/2/2
	BANK11	25/12/12	10/5/5	4/2/2
	BANK12	4/2/0	4/2/0	4/2/0
Max. User I/O[2]		297	198	113
Differential Pair		145	98	55
True LVDS Output		143	96	53
VCCIO1		3	3	0
VCCIO2		3	3	0
VCCIO2		0	2	0
VCCIO4		3	2	0
VCCIO5		3	2	2
VCCIO6		2	0	0
VCCIO7		2	0	0
VCCIO8		2	0	2
VCCIO9		6	6	2
VCCIO10		3	2	0
VCCIO11		3	2	0
VCCIO1/VCCIO2		0	0	1
VCCIO10/VCCIO11		0	0	2
VCCIO12/VCCIO3/VCCIO4		0	0	2
VCCIO12/VCCIO3		2	0	0
VCCIO12/VCCIO6/VCCIO7/VCCIO8/ VCCX/VDDHA_Q0		0	11	0
VCC		14	11	7

Pin Type	GW5AT-60		
	PBGA484A	UBGA324S	UBGA225
VCCX	4	0	0
VDD12_MIPI	0	4	1
VDDA_MIPI/VDDD_MIPI	0	0	3
VDDX_MIPI/VCCIO6/VCCIO7/VCCX	0	0	6
VDDA_Q0	3	0	3
VDDHA_Q0	1	0	2
VDDT_Q0	2	0	3
VCC_ADC	1	0	1
V_EFUSE	1	1	1
VREFN	1	0	0
VREFP	1	0	0
VSS	87	45	35
MODE0	1	1	1
MODE1	1	1	1
MODE2	1	0	0
NC	15	7	0

Note!

- [1] Single-ended/Differential I/O quantity includes CLK pins and download pins.

2.5 I/O BANK Introduction

GW5AT-138 has six GPIO Banks (Bank2~7), two SerDes Banks and a Bank for configuration (Bank 10). Bank 10 can also be used as an I/O Bank. See *DS981, GW5AT series of FPGA Products Data Sheet > 2.3 Input/Output Blocks* for details.

This manual provides the pin distribution view of GW5AT series of FPGA products. For details, please refer to Chapter 3 View of Pin Distribution. The I/O Banks that form GW5AT series of FPGA products are marked with different colors.

Various symbols and colors are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes the I/O in BANK2.
- "  " denotes the I/O in BANK3.
- "  " denotes the I/O in BANK4.
- "  " denotes the I/O in BANK5.
- "  " denotes the I/O in BANK6.
- "  " denotes the I/O in BANK7.
- "  " denotes the I/O in BANK10.
- "  " denotes the DIO in SerDes Bank Q0, SerDes Bank Q1, MIPI, and ADC.
- "  " denotes VCC, VCCX, and VCCIO, and the filling color does not change.
- "  " denotes VSS, and the filling color does not change.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW5AT-138 Pin Distribution

3.1.1 View of FPG676A (Flip Clip) Pin Distribution

Figure 3-1 View of GW5AT-138 FPG676A (Flip Chip) Pin Distribution (Top View)

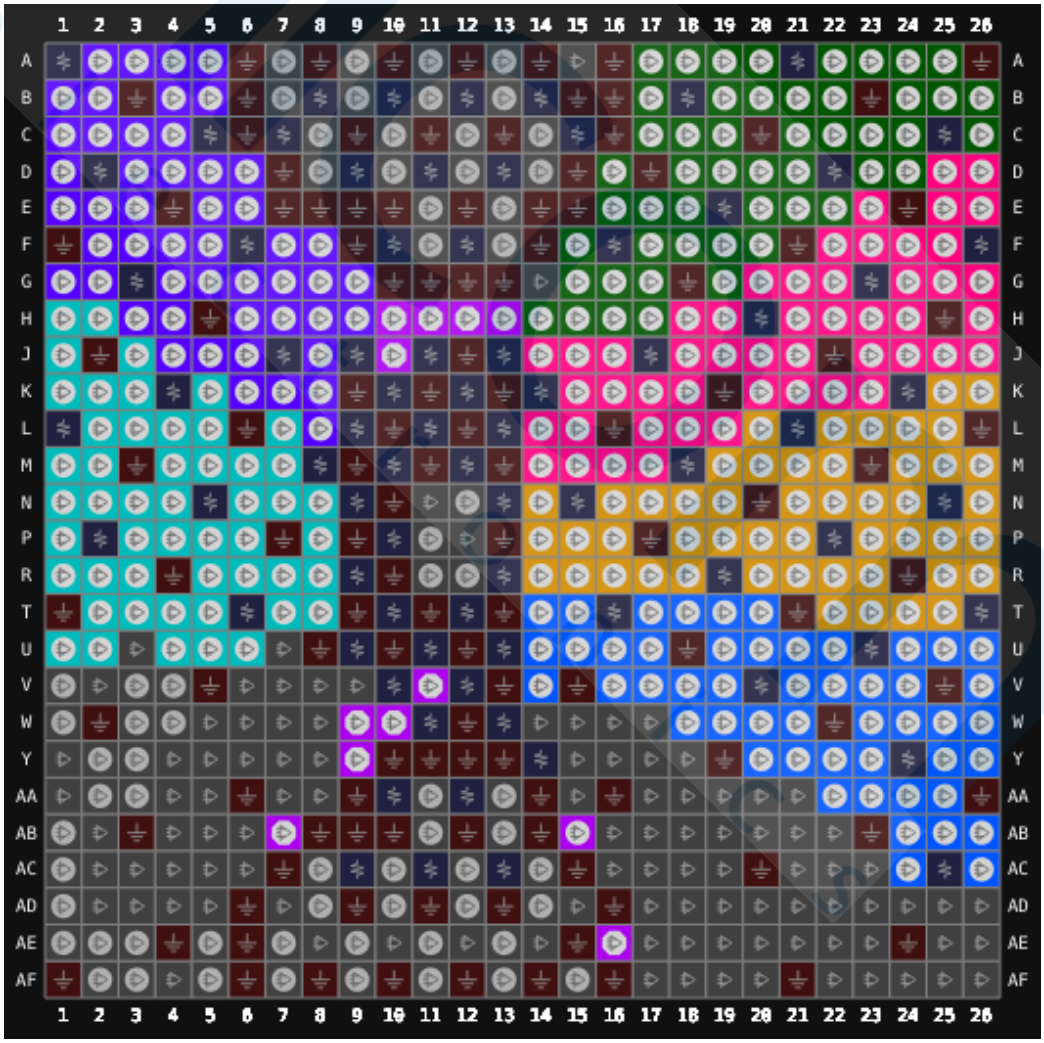


Table 3-1 Other Pins in GW5AT-138 FPG676A (Flip Chip)

VCCIO2	V20,U23,T26,Y24,AC25,T16
VCCIO3	R19,K24,N25,N15,P22,L21
VCCIO4	F26,M18,J17,H20,G23,K14
VCCIO5	C25,D22,F16,A21,B18,E19
VCCIO6	J7,D2,F6,C5,A1,G3
VCCIO7	M8,K4,P2,T6,L1,N5
VCCIO10	W11,Y14
VCCX	N9,L9,J9
VCC	L11,V10,P10,L13,K12,V12,K10,T12,M10,T10,J11,J13,U11
VCC_LDO	C15,B8,B14,C7,B12,B10
VDDHA_Q1	R9
VDDHA_Q0	U9
VDDA_Q1/VDDD_Q1	AC9,AC13,AC11
VDDA_Q0/VDDD_Q0	D11,D9,D13
VDDT_Q1	AA12,AA10
VDDT_Q0	F10,F12
VDDX_MIPI	M12
VDDA_MIPI/VDDD_MIPI	N13,R13,U13,W13
VSS	M11,AE15,B15,A10,A12,A14,A16,A26,A6,A8,AA14,AA16,AA26,AA6,AB10,AB12,AB14,AB23,AB3,AA9,AB8,AC15,AC20,AC7,AD11,AD13,AD6,AD9,AD16,AE24,AE4,AE6,AF1,AF10,AF12,AF14,AF16,AF21,AF6,AF8,B16,B23,B3,B6,C11,C13,C16,C20,C6,C9,D15,D17,D7,E10,E12,E14,E24,E4,E7,E8,E9,F1,F14,F21,F9,G10,G11,AB9,G13,Y12,G18,G12,H25,H5,J12,J2,J22,K11,K13,K19,K9,L10,L12,L16,L26,L6,M13,M23,M3,M9,N10,N20,P13,P17,P7,P9,R10,R24,R4,T1,T11,T13,T21,T9,U10,U12,U18,U8,V15,V25,V5,E15,W12,W2,W22,Y11,Y10,Y13,Y19,V13

3.1.2 View of PG484A Pin Distribution

Figure 3-2 View of GW5AT-138 PG484A Pin Distribution (Top View)

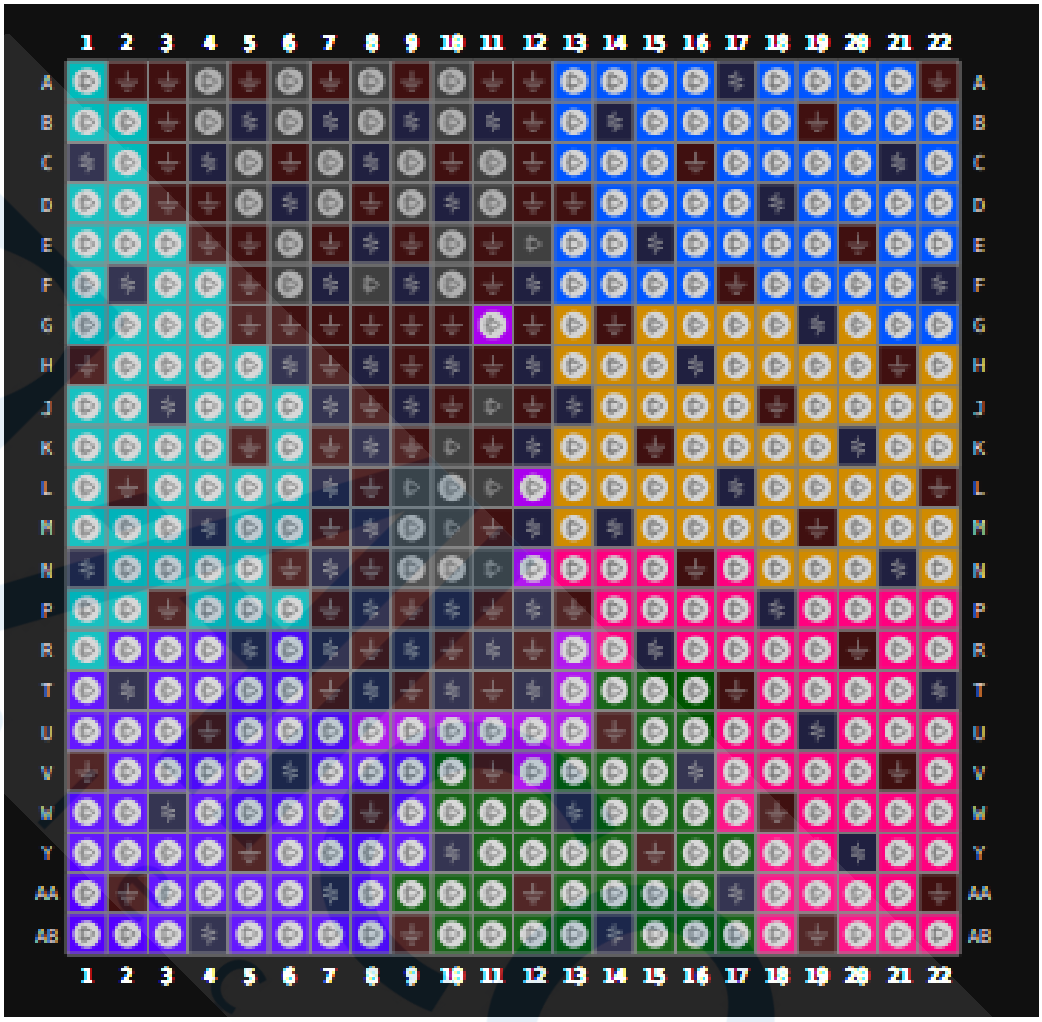


Table 3-2 Other Pins in GW5AT-138 PG484A

VCCIO2	B14,D18,E15,F22,A17,C21
VCCIO3	L17,J13,H16,G19,K20,N21
VCCIO4	U19,Y20,T22,M14,P18,R15
VCCIO5	W13,V16,AA17,AB14,Y10
VCCIO6	AA7,V6,W3,T2,R5,AB4
VCCIO7	C1,J3,N1,M4,H6,F2
VCCIO10	F12,T12
VCCX	P12,M12,R11
VCC	H8,T8,R9,H10,P8,N7,J7,R7,K8,L7,P10,T10,J9,M8
VCC_LDO	B7,B9,B5,B11,C4,C8
VDDHA_Q1	K12
VDDHA_Q0	H12
VDDA_Q0/VDDD_Q0	F7,D10,D6
VDDT_Q0	E8,F9

VSS	K9,D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,T17,U4,U14,V1,V11,V21,W8,W18,Y5,Y15

3.1.3 View of PG484 Pin Distribution

Figure 3-3 View of GW5AT-138 PG484 Pin Distribution (Top View)

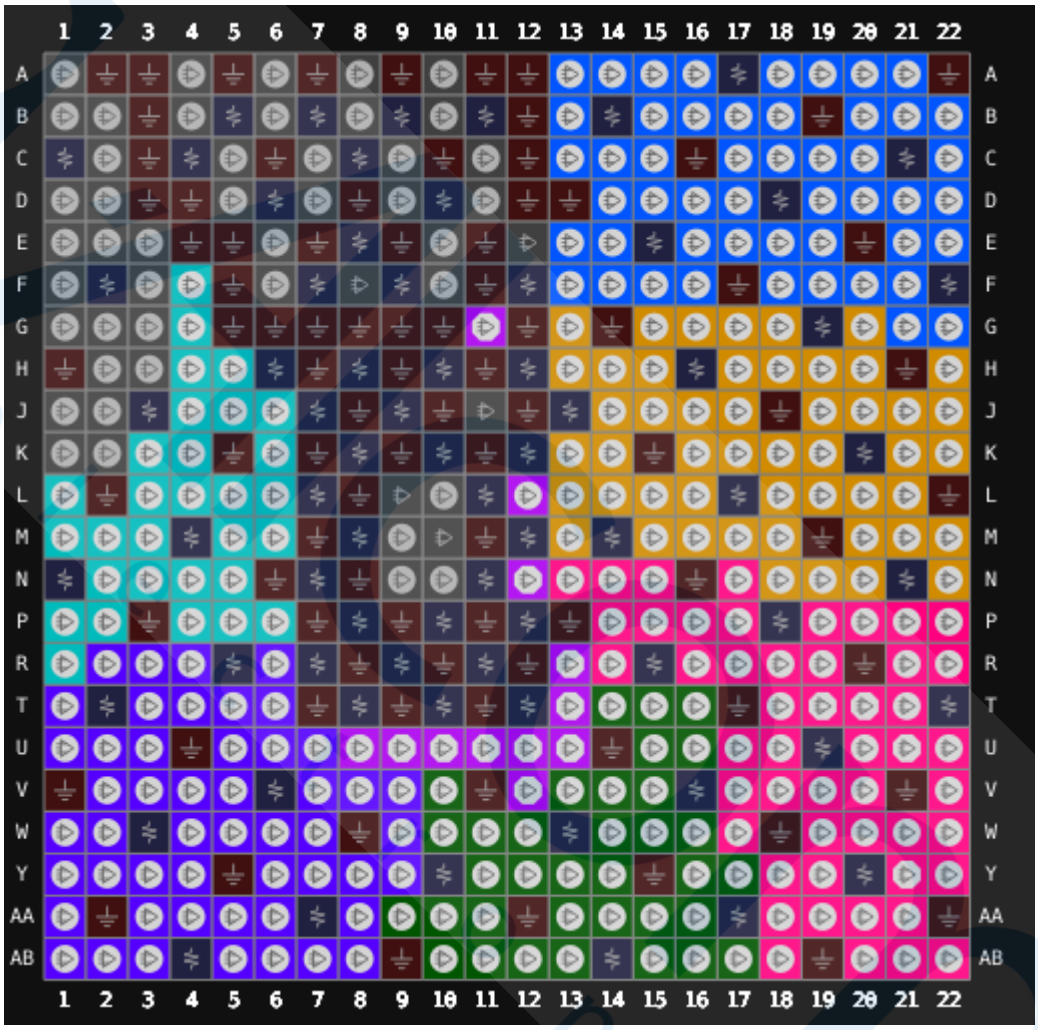


Table 3-3 Other Pins in GW5AT-138 PG484

VCCIO2	B14,D18,E15,F22,A17,C21
VCCIO3	L17,J13,H16,G19,K20,N21
VCCIO4	U19,Y20,T22,M14,P18,R15
VCCIO5	W13,V16,AA17,AB14,Y10
VCCIO6	AA7,V6,W3,T2,R5,AB4
VCCIO7	C1,J3,N1,M4,H6,F2
VCCIO10	F12,T12
VCCX	P12,M12,R11
VCC	H8,T8,R9,H10,P8,N7,J7,R7,K8,L7,P10,T10,J9,M8
VCC_LDO	B7,B9,B5,B11,C4,C8
VDDX_MIPI	K10
VDDA_MIPI/VDDD_MIPI	L11,N11
VDDHA_Q0	H12, K12
VDDA_Q0/VDDD_Q0	F7,D10,D6
VDDT_Q0	E8,F9
VSS	K9,D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,T17,U4,U14,V1,V11,V21,W8,W18,Y5,Y15

3.1.4 View of PG676A Pin Distribution

Figure 3-4 View of GW5AT-138 PG676A Pin Distribution (Top View)

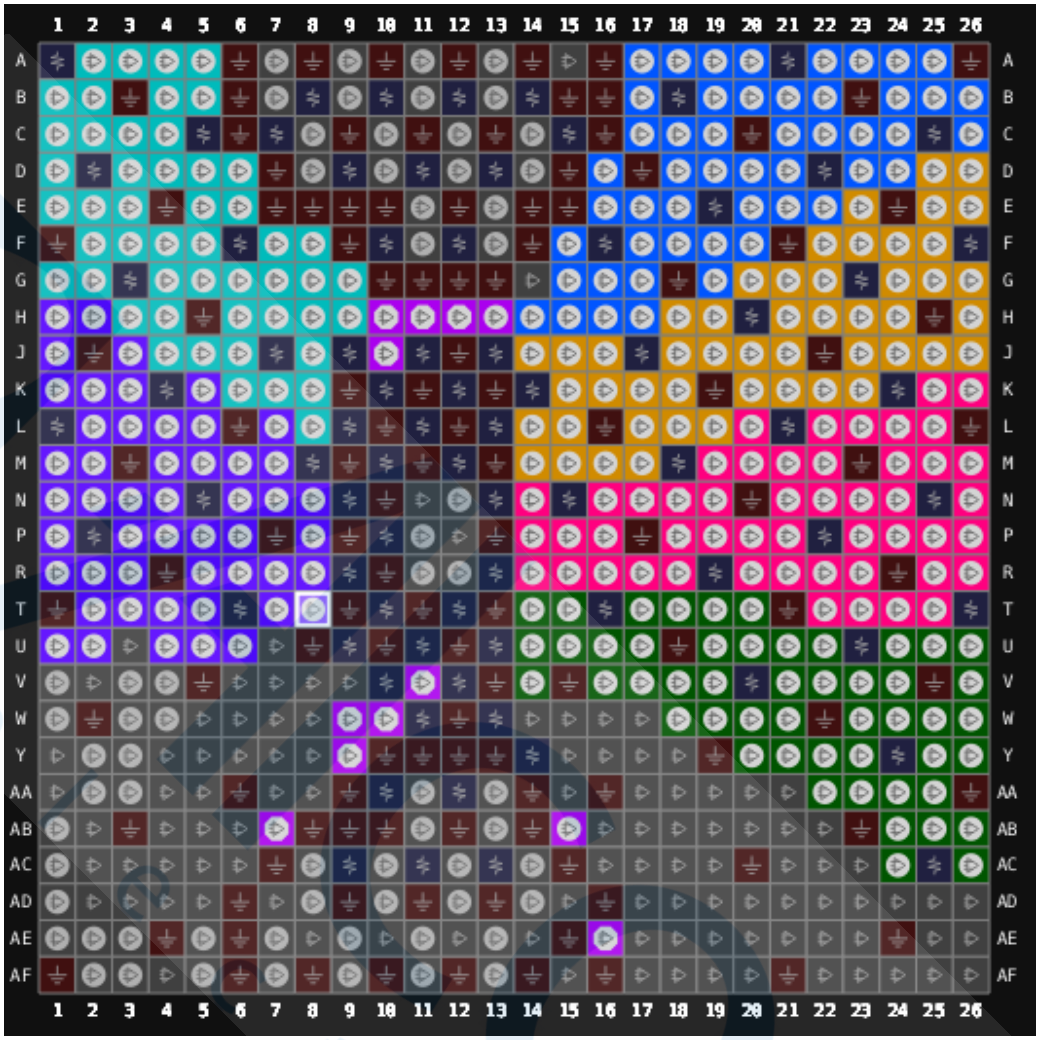


Table 3-4 Other Pins in GW5AT-138 PG676A

VCCIO2	E19,C25,A21,D22,F16,B18
VCCIO3	G23,K14,M18,H20,F26,J17
VCCIO4	L21,P22,N15,K24,N25,R19
VCCIO5	Y24,T16,U23,V20,AC25,T26
VCCIO6	L1,P2,N5,T6,K4,M8
VCCIO7	J7,D2,A1,G3,C5,F6
VCCIO10	Y14,W11
VCCX	N9,L9,J9
VCC	V12,V10,T12,L13,T10,L11,K12,M10,U11,K10,J11,P10,J13
VCC_LDO	B12,B10,C7,C15,B14,B8
VDDX_MIPI	M12
VDDA_MIPI	N13,R13
VDDD_MIPI	U13,W13

VDDHA_Q0/VDDHA_Q1	U9,R9
VDDA_Q0	AA12,AC11,AA10
VDDT_Q0	AC13,AC9
VDDA_Q1	F12,D9,F10
VDDT_Q1	D13,D11
VSS	M11,AE15,B15,A10,A12,A14,A16,A26,A6,A8,AA14,AA16,AA26,AA6,AB10,AB12,AB14,AB23,AB3,AA9,AB8,AC15,AC20,AC7,AD11,AD13,AD6,AD9,AD16,AE24,AE4,AE6,AF1,AF10,AF12,AF14,AF16,AF21,AF6,AF8,B16,B23,B3,B6,C11,C13,C16,C20,C6,C9,D15,D17,D7,E10,E12,E14,E24,E4,E7,E8,E9,F1,F14,F21,F9,G10,G11,AB9,G13,Y12,G18,G12,H25,H5,J12,J2,J22,K11,K13,K19,K9,L10,L12,L16,L26,L6,M13,M23,M3,M9,N10,N20,P13,P17,P7,P9,R10,R24,R4,T1,T11,T13,T21,T9,U10,U12,U18,U8,V15,V25,V5,E15,W12,W2,W22,Y11,Y10,Y13,Y19,V13

3.1.5 View of UG324A Pin Distribution

Figure 3-5 View of GW5AT-138 UG324A Pin Distribution (Top View)

Table 3-5 Other Pins in GW5AT-138 UG324A

VCCIO2	A16,C10,D17,B13
VCCIO3	H15,G18,E14
VCCIO4	T11,P17,V15,R14,L16,U8,U18
VCCIO5	T1,V5
VCCIO6	P7,R4
VCCIO7	L6,M3
VCCIO10	E10,R10
VCCX	K13,M13,P13
VCC	P9,K7,L12,N8,N10,F9,G8,H7,P11,F7,L8,K11,M7,J8,H9,M11,J12,N12
VCC_LDO	H13
VDDX_MIPI	J10
VDDA_MIPI/VDDD_MIPI	F11,H11,G10
VDDHA_Q0	G12
VDDA_Q0	E5,F5
VDDT_Q0	B4,C5
VSS	A1,A5,A7,A8,A11,A18,B3,B7,B8,B18,C2,C6,C7,C15,D3,D4,D7,D12,E2,E6,E7,E9,F4,F6,F10,F16,G1,G5,G6,G7,G9,G11,G13,H3,H4,H5,H6,H8,H10,H12,J1,J2,J3,J7,J11,J13,J17,K4,K8,K12,K14,L1,L7,L11,L13,M8,M12,M18,N5,N7,N9,N11,N13,N15,P2,P8,P12,R9,T6,T16,U3,U13,V1,V10,V18,J9

3.2 View of GW5AT-75 Pin Distribution

3.2.1 View of UG484 Pin Distribution

Figure 3-6 View of GW5AT-75 UG484 Pin Distribution (Top View)

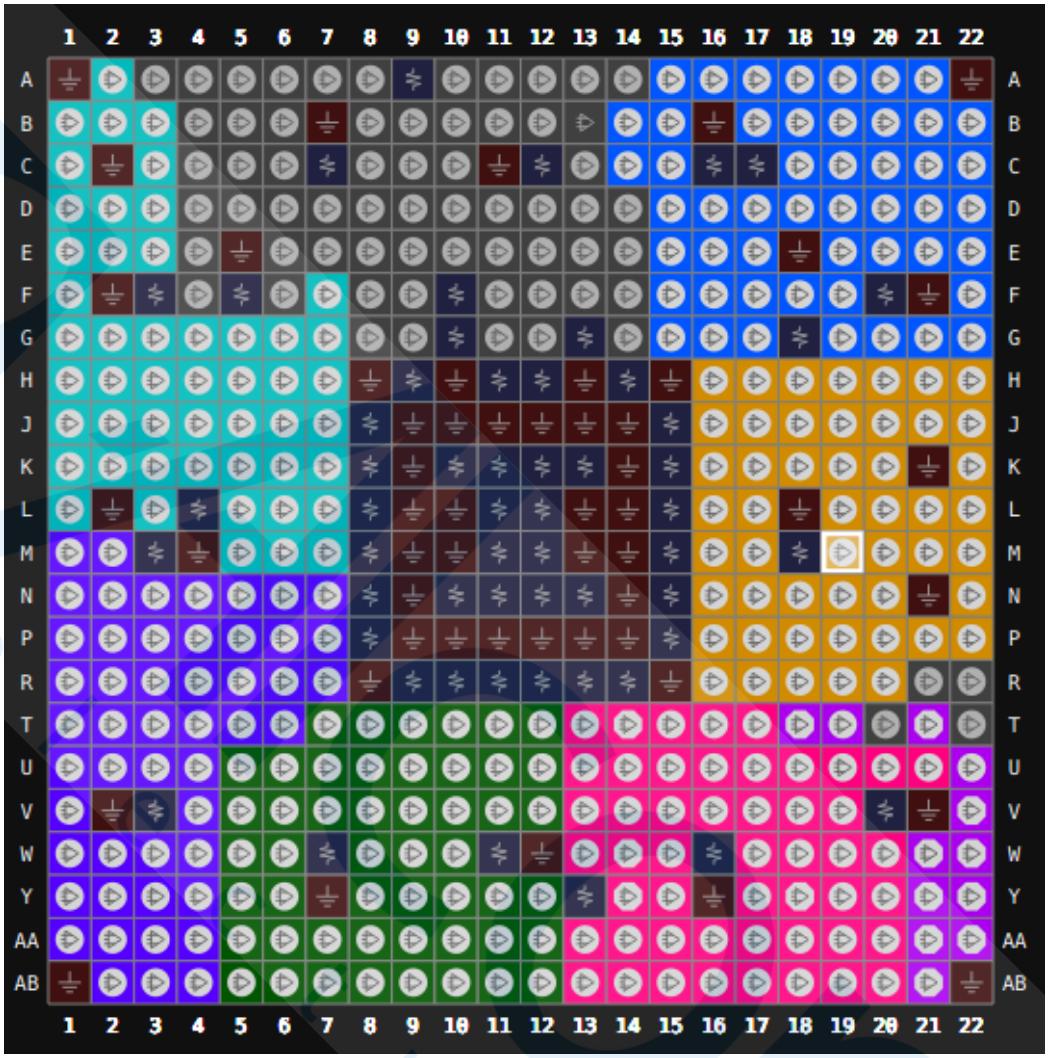


Table 3-6 Other Pins in GW5AT-75 UG484

VCCIO2	G18,F20,L15
VCCIO3	P15,N15,M15,M18
VCCIO4	R13,R12,R14,Y13
VCCIO5	R11,R9,R10,W11,W7
VCCIO6	P8,N8,V3
VCCIO7	L8,M3,M8
VCCIO10	V20,W16
VCCIO11/VCCX/VDDX_MIPI	L4,F3
VCC_LDO	K8,J8,F5
VCC	L11,M12,N12,M11,K10,K12,N11,N10,K13,N13,L12,K11
VDDT_Q1	C12,H14,H12

VDDA_Q1	C16,G13
VDDT_Q0	F10,C17,H11
VDDHA_Q0/VDDHA_Q1	K15,J15
VDDA_Q0	C7,G10
VDDA_MIPI/VDDD_MIPI	H9,A9
VSS	A22,AB22,F21,K21,N21,V21,E18,L18,B16,Y16,H15,R15,J14,K14,L14,M14,N14,P14,H13,J13,L13,M13,P13,J12,P12,W12,C11,J11,P11,H10,J10,L10,M10,P10,J9,K9,L9,M9,N9,P9,H8,R8,B7,Y7,E5,M4,C2,F2,L2,V2,A1,AB1

3.3 View of GW5AT-60 Pin Distribution

3.3.1 View of PG484A Pin Distribution

Figure 3-7 View of GW5AT-60 PG484A Pin Distribution (Top View)

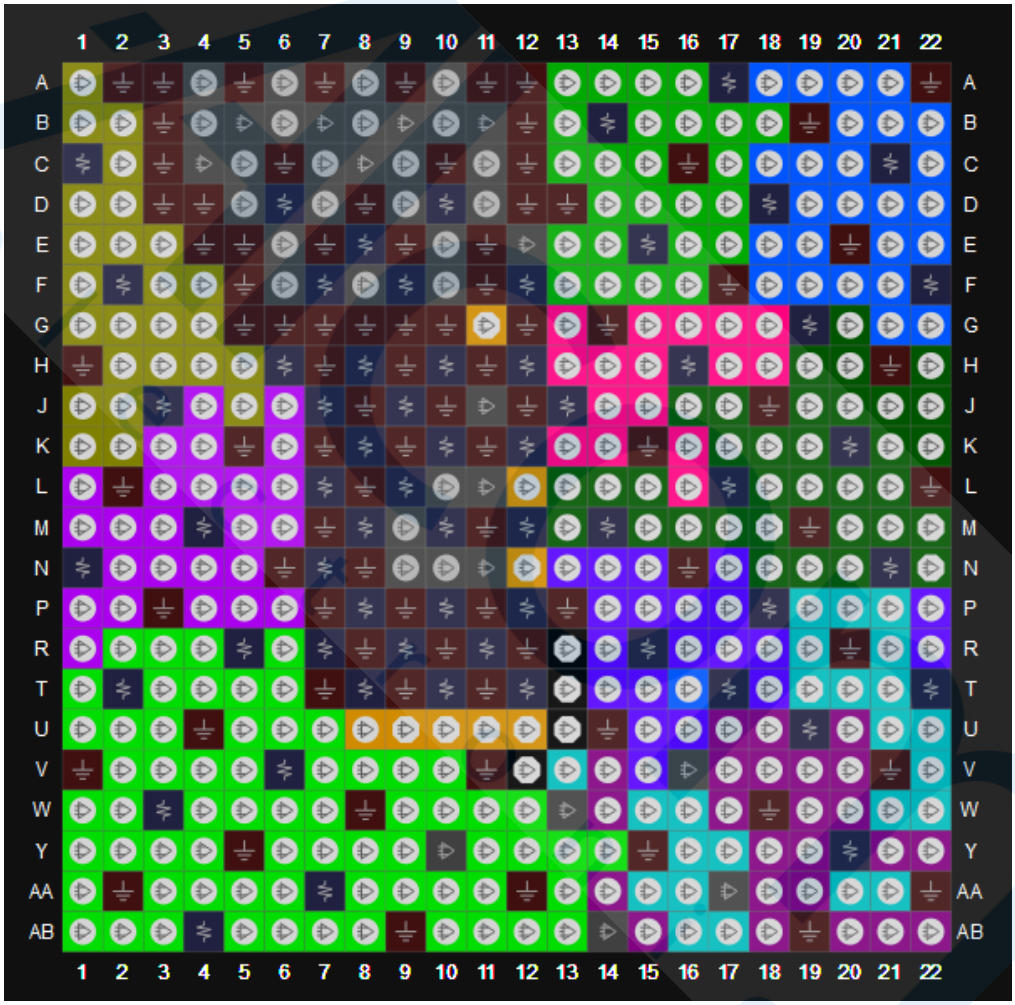


Table 3-7 Other Pins in GW5AT-60 PG484A

VCCIO1	B14,A17,C21
VCCIO2	D18,E15,F22
VCCIO4	H16,J13,G19
VCCIO5	L17,N21,K20
VCCIO6	M14,P18
VCCIO7	T22,R15
VCCIO8	Y20,U19
VCCIO9	V6,AB4,T2,AA7,W3,R5
VCCIO10	C1,H6,F2
VCCIO11	M4,J3,N1
VCCIO12/VCCIO3	F12,T12
VCC	J9,P10,P8,N7,H10,M8,R9,T8,R7,T10,K8,H8,J7,L7
VCCX	P12,R11,H12,M12
VCC_ADC	K10
V_EFUSE	T17
VREFN	L9
VREFP	M10
VDDA_Q0	F9,E8,F7
VDDHA_Q0	K12
VDDT_Q0	D10,D6
VSS	D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,U4,U14,V1,V11,V21,W8,W18,Y5,Y15,K9

3.3.2 View of UG225 Pin Distribution

Figure 3-8 View of GW5AT-60 UG225 Pin Distribution (Top View)

Table 3-8 Other Pins in GW5AT-60 UG225

VCCIO5	M14,J12
VCCIO8	P12,P8
VCCIO9	M7,P4
VCCIO1/VCCIO2	B12
VCCIO10/VCCIO11	M2,L4
VCCIO12/VCCIO3/VCCIO4	D14,H14
VCC	F9,H9,G8,J8,H7,K7,J10
VCC_ADC	E12
V_EFUSE	L11
VDDA_MIPI/VDDD_MIPI	D2,H2,G4
VDDX_MIPI/VCCIO6/VCCIO7/ VCCX	M12,J6,B1,F7,K9,G10
VDD12_MIPI	G6
VDDA_Q0	D5,D11,B8
VDDHA_Q0	D7,D9
VDDT_Q0	A10,A6,B4
VSS	A1,A15,B10,B6,C13,C3,E11,F14,F2,F6,G7,G9,H8,J7,J9,K14,K2,K6,N13,N3,P10,P6,R1,R15,A2,B2,A4,D3,E4,A8,C9,C11,A12,C7,C5

3.3.3 View of UG324S Pin Distribution

Figure 3-9 View of GW5AT-60 UG324S Pin Distribution (Top View)

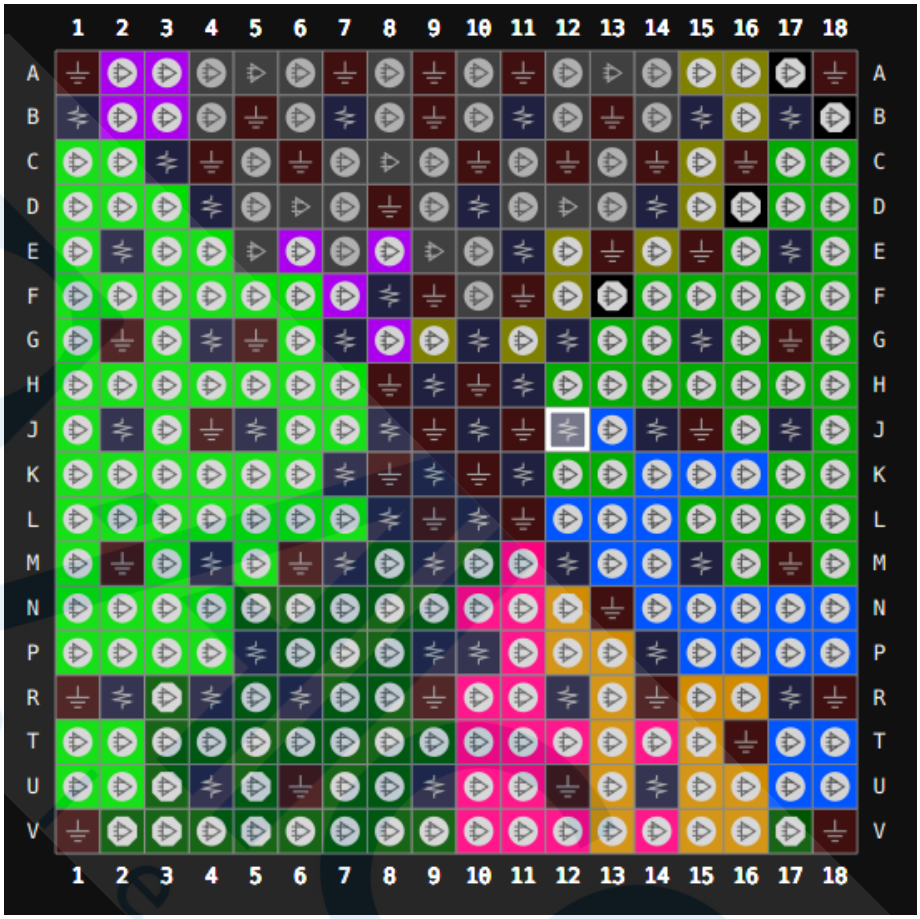


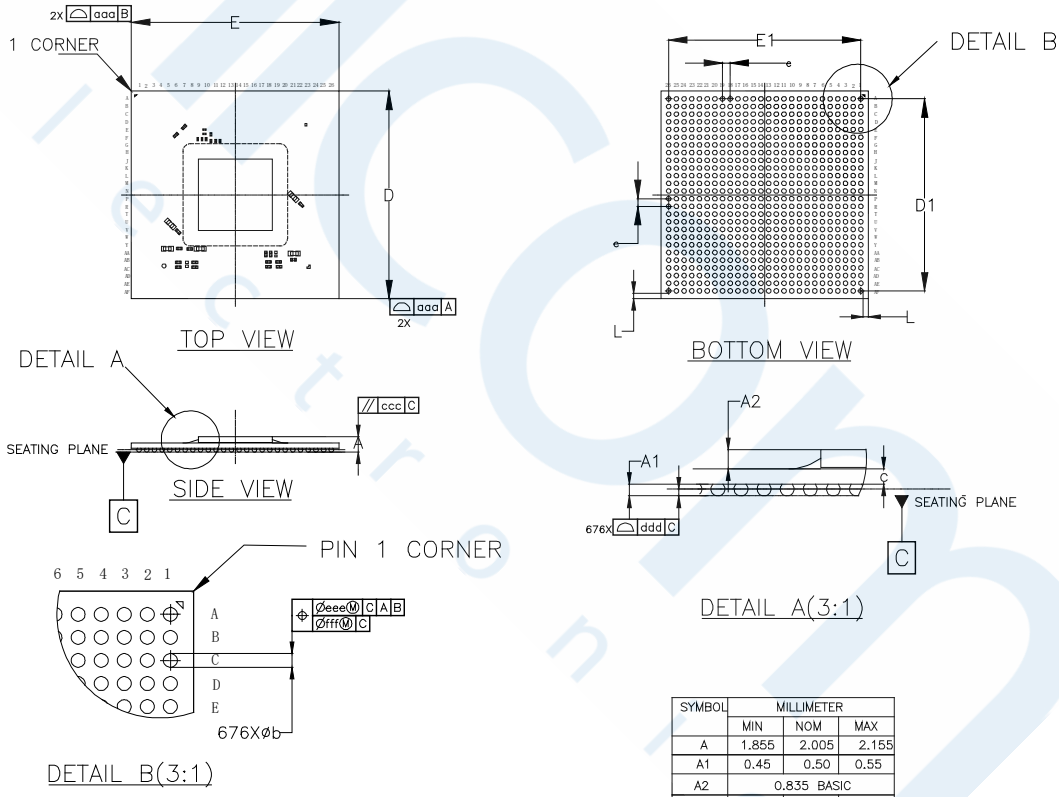
Table 3-9 Other Pins in GW5AT-60 UG324S

VCCIO1	E17,G15,J14
VCCIO2	J17,M15,R17
VCCIO3	R12,U14
VCCIO4	P9,U9
VCCIO5	R6,U4
VCCIO9	R2,G4,E2,M4,J2,J5
VCCIO10	F8,C3
VCCIO11	B15,G12
VCCIO12/VCCIO6/VCCIO7/ VCCIO8/VCCX/VDDHA_Q0	P10,M9,D14,B1,P14,G10,J12,D4,K7,B17,P5
V_EFUSE	R4
VDD12_MIPI	H9,J10,K9,J8,M12,G7,K11,L8,M7,L10,H11
VDDA_Q0	E11,B7,B11,D10
VSS	A1,A11,A18,A7,A9,B13,B5,B9,C10,C12,C14,C16, C4,C6,D8,E13,E15,F11,F9,G17,G2,G5,H10,H8,J1 1,J15,J4,J9,K10,K8,L11,L9,M17,M2,M6,N13,R1,R 14,R18,R9,T16,U12,U6,V1,V18

4 Package Diagram

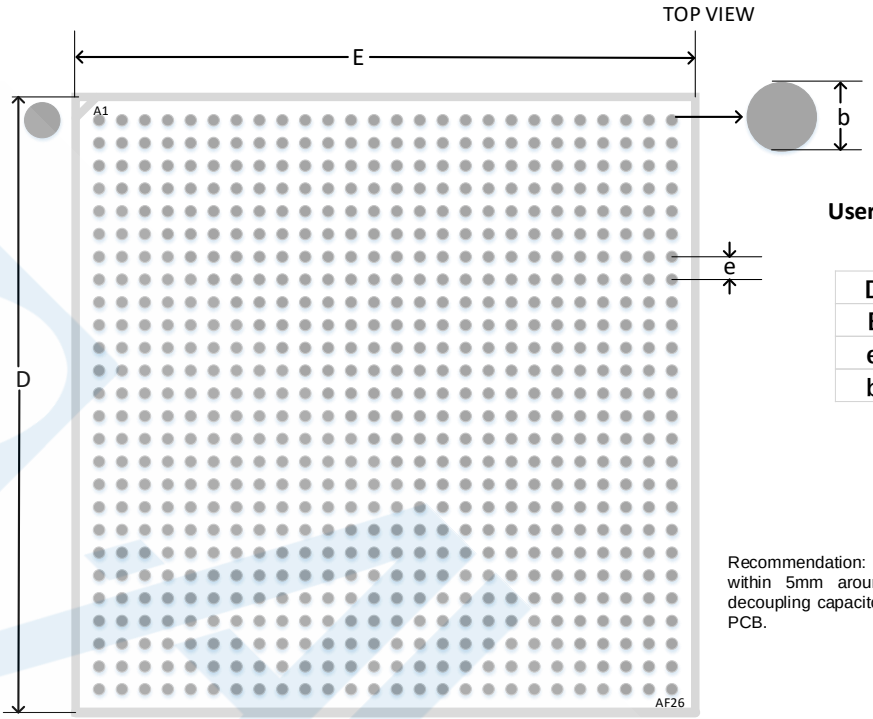
4.1 FPG676A (Flip Chip) Package Outline (27mm x 27mm, GW5AT-138)

Figure 4-1 Package Outline FPG676A (Flip Chip)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.855	2.005	2.155
A1	0.45	0.50	0.55
A2		0.835 BASIC	
c	0.60	0.67	0.74
D	26.90	27.00	27.10
D1		25.00 BASIC	
E	26.90	27.00	27.10
E1		25.00 BASIC	
L		0.70 REF	
e		1.00 BASIC	
b	0.55	0.60	0.65
aaa		0.20	
ccc		0.25	
ddd		0.20	
eee		0.25	
fff		0.10	

Figure 4-2 Recommended PCB Layout FPG676A (Flip Chip)



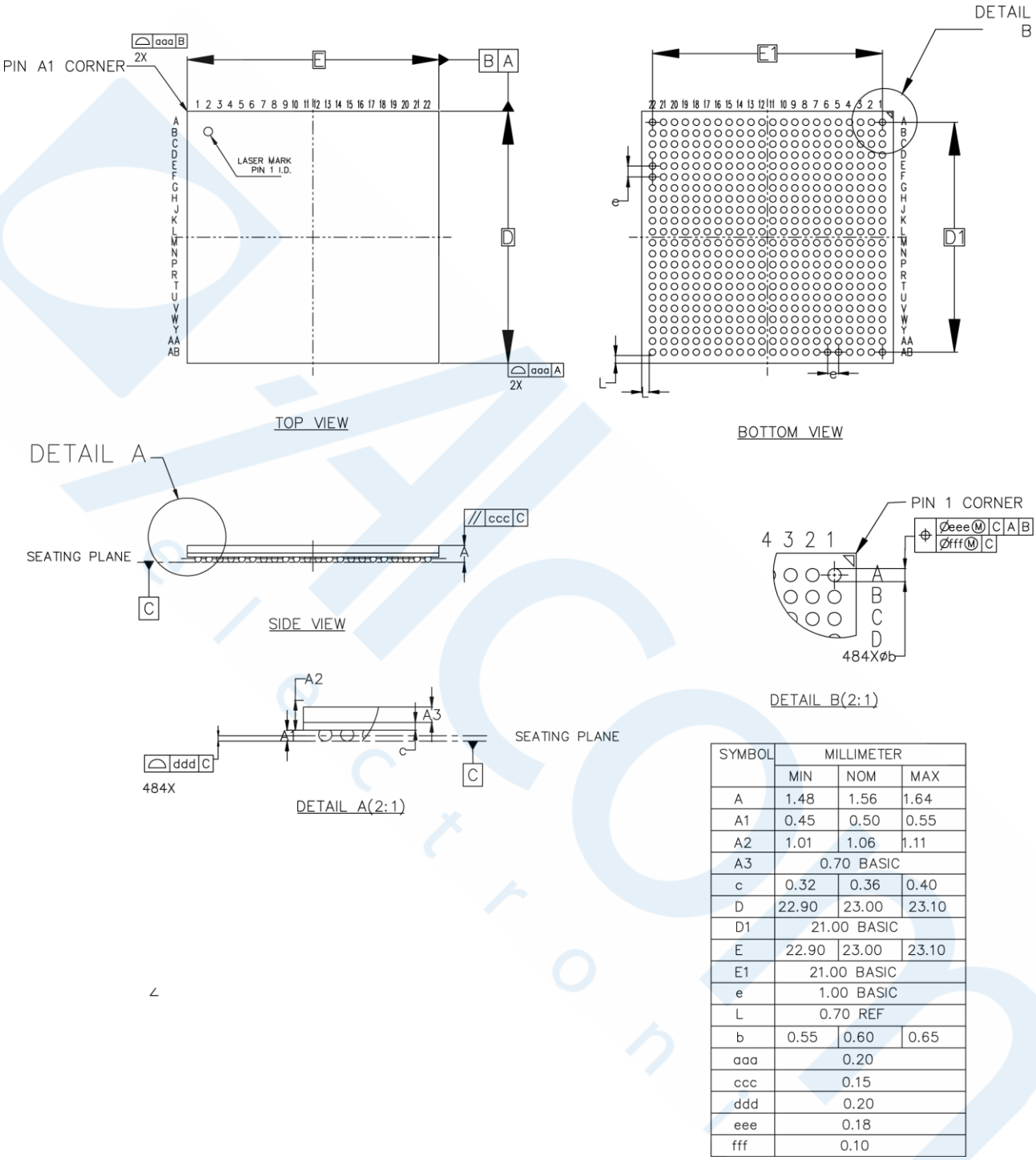
User units:mm

D	27.0
E	27.0
e	1.0
b	0.5

Recommendation: Do not place devices within 5mm around BGA, and place decoupling capacitors on the back of the PCB.

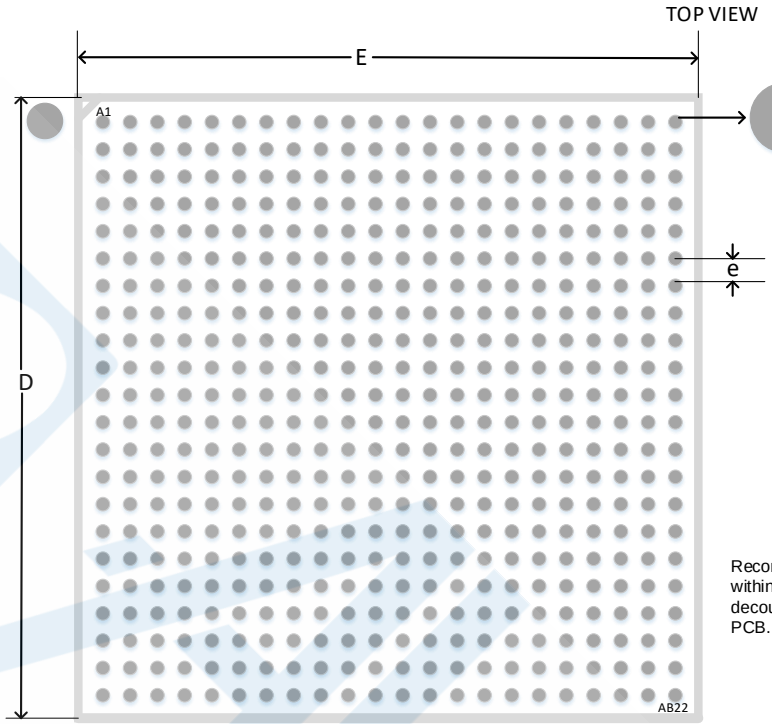
4.2 PG484A Package Outline (23mm x 23mm, GW5AT-138)

Figure 4-3 Package Outline PG484A (GW5AT-138)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.48	1.56	1.64
A1	0.45	0.50	0.55
A2	1.01	1.06	1.11
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	22.90	23.00	23.10
D1	21.00 BASIC		
E	22.90	23.00	23.10
E1	21.00 BASIC		
e	1.00 BASIC		
L	0.70 REF		
b	0.55	0.60	0.65
aaa	0.20		
ccc	0.15		
ddd	0.20		
eee	0.18		
fff	0.10		

Figure 4-4 Recommended PCB Layout PG484A (GW5AT-138)



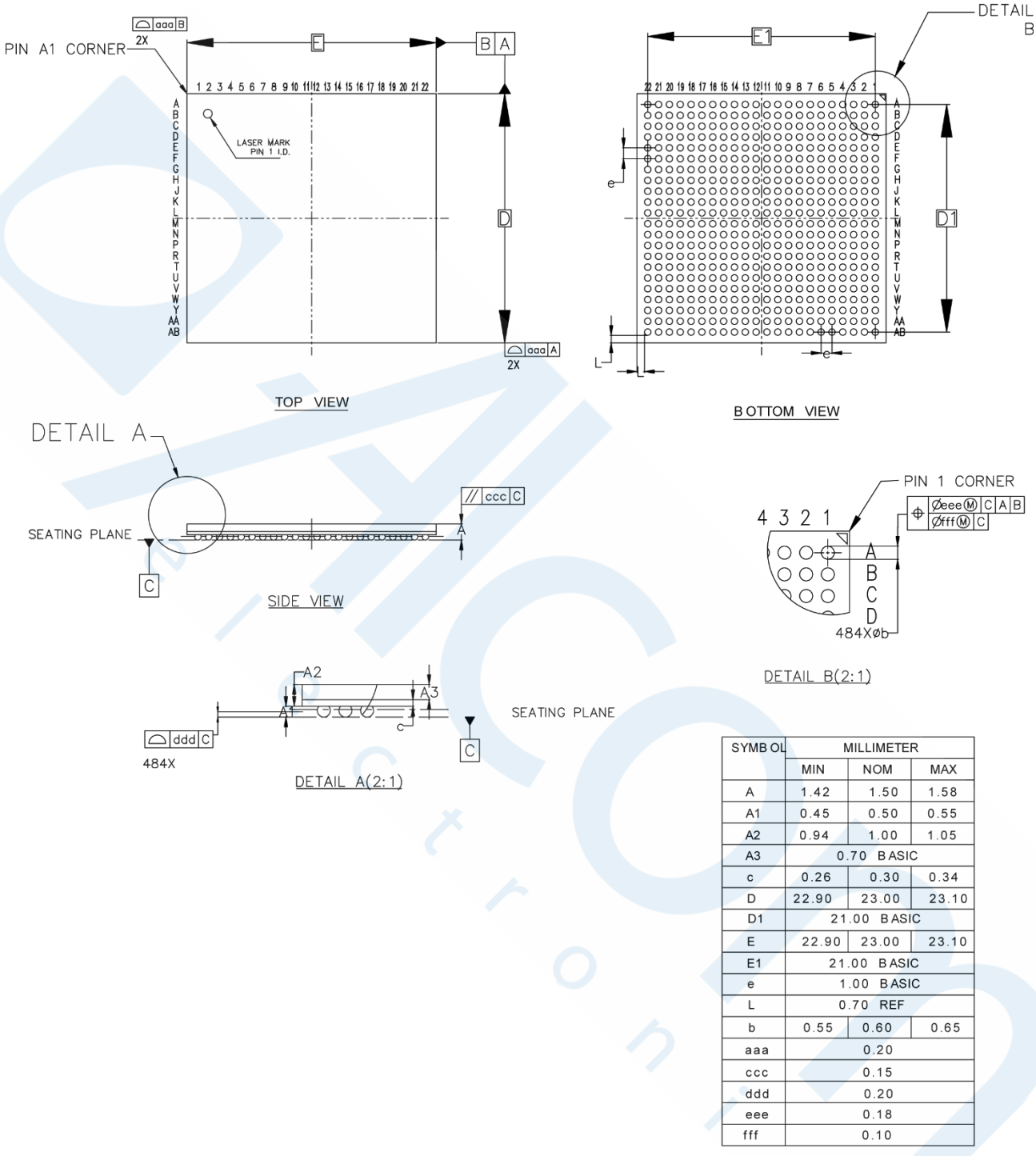
User units:mm

D	23.0
E	23.0
e	1.0
b	0.5

Recommendation: Do not place devices within 5mm around BGA, and place decoupling capacitors on the back of the PCB.

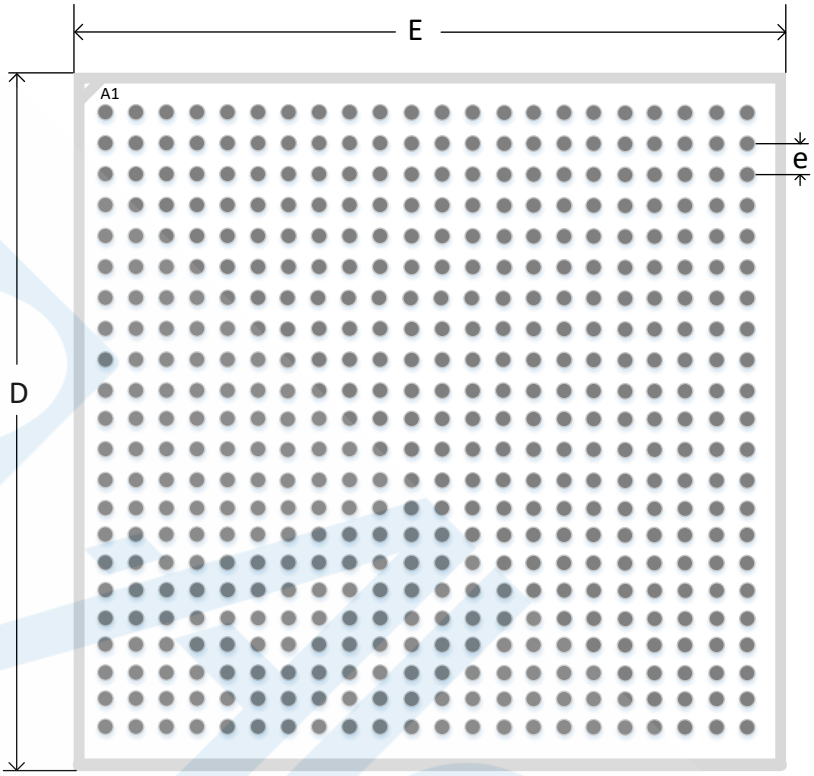
4.3 PG484A Package Outline (23mm x 23mm, GW5AT-60)

Figure 4-5 Package Outline PG484A (GW5AT-60)

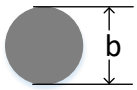


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.42	1.50	1.58
A1	0.45	0.50	0.55
A2	0.94	1.00	1.05
A3		0.70 BASIC	
c	0.26	0.30	0.34
D	22.90	23.00	23.10
D1		21.00 BASIC	
E	22.90	23.00	23.10
E1		21.00 BASIC	
e		1.00 BASIC	
L		0.70 REF	
b	0.55	0.60	0.65
aaa		0.20	
ccc		0.15	
ddd		0.20	
eee		0.18	
fff		0.10	

Figure 4-6 Recommended PCB Layout PG484A (GW5AT-60)



TOP VIEW

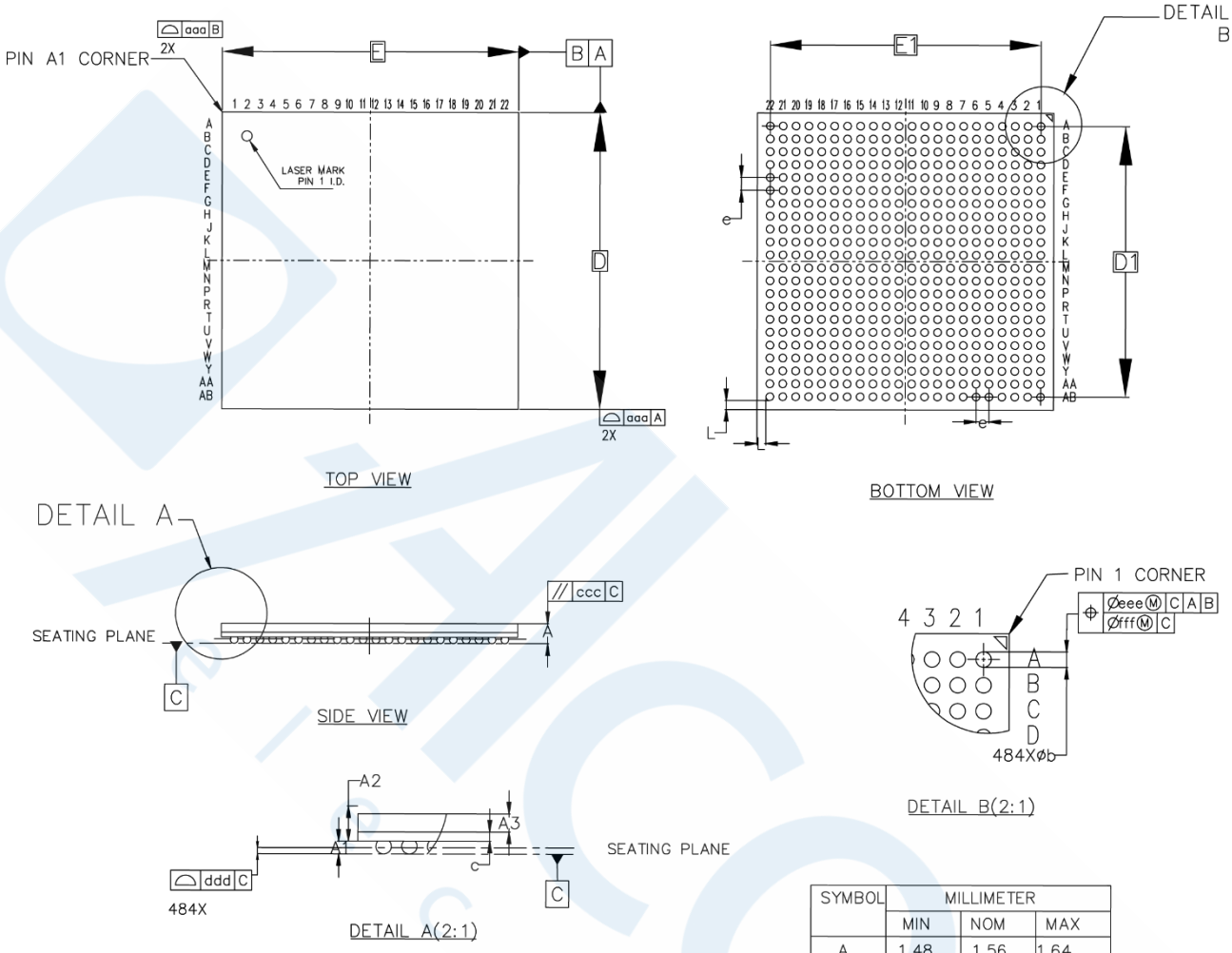


Unit:mm

D	23.00
E	23.00
e	1.00
b	0.50

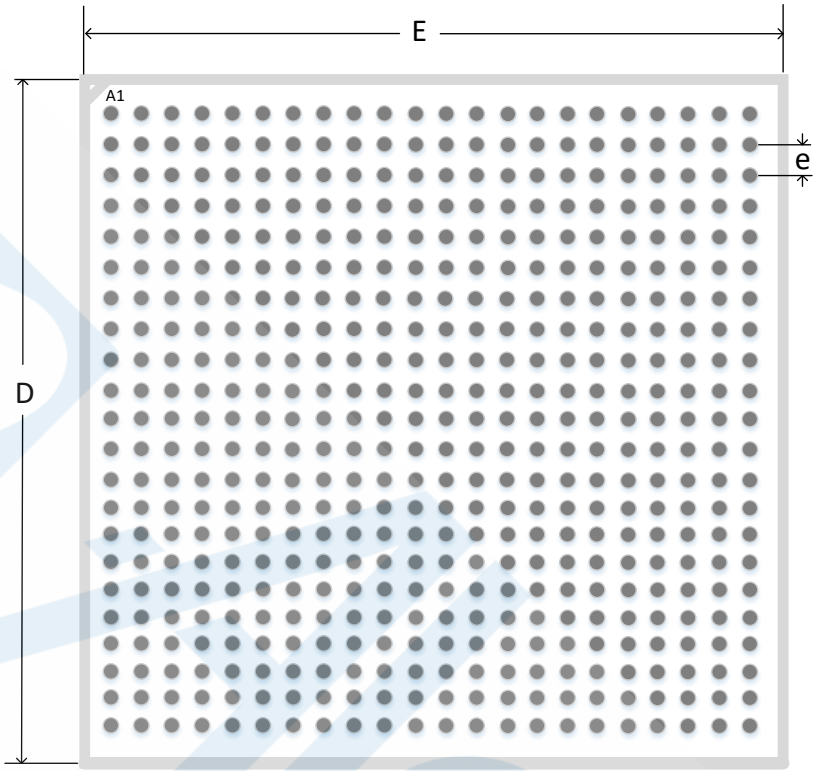
4.4 PG484 Package Outline (23mm x 23mm, GW5AT-138)

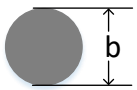
Figure 4-7 Package Outline PG484



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.48	1.56	1.64
A1	0.45	0.50	0.55
A2	1.01	1.06	1.11
A3		0.70 BASIC	
c	0.32	0.36	0.40
D	22.90	23.00	23.10
D1		21.00 BASIC	
E	22.90	23.00	23.10
E1		21.00 BASIC	
e		1.00 BASIC	
L		0.70 REF	
b	0.55	0.60	0.65
aaa		0.20	
ccc		0.15	
ddd		0.20	
eee		0.18	
fff		0.10	

Figure 4-8 Recommended PCB Layout PG484



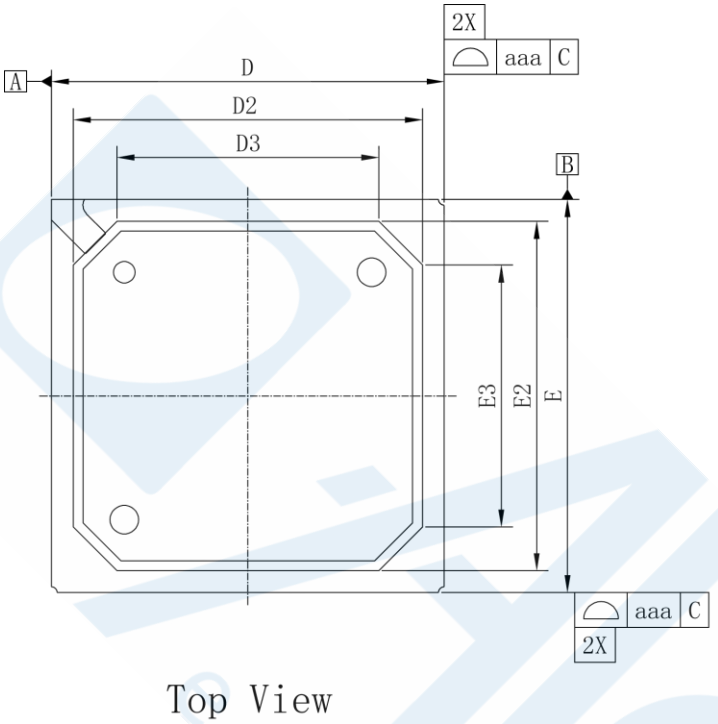


Unit:mm

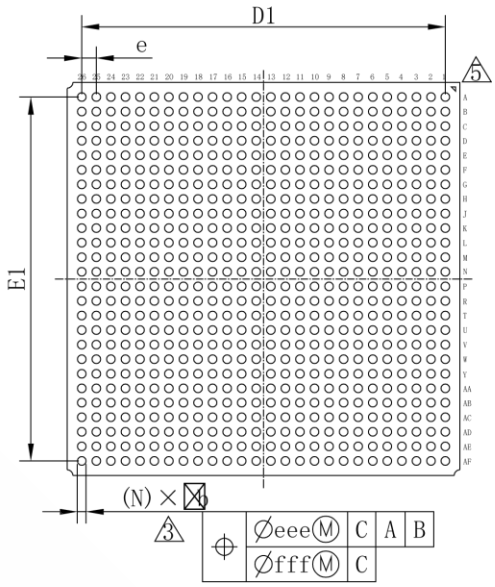
D	23.00
E	23.00
e	1.00
b	0.50

4.5 PG676A Package Outline (27mm x 27mm, GW5AT-138)

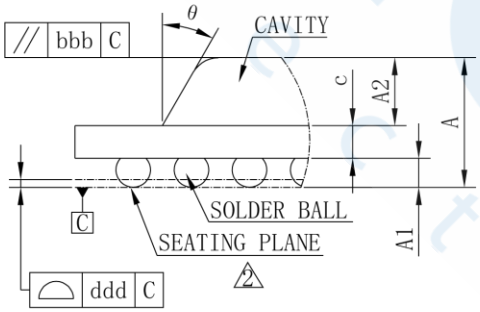
Figure 4-9 Package Outline PG676A



Top View



Bottom View



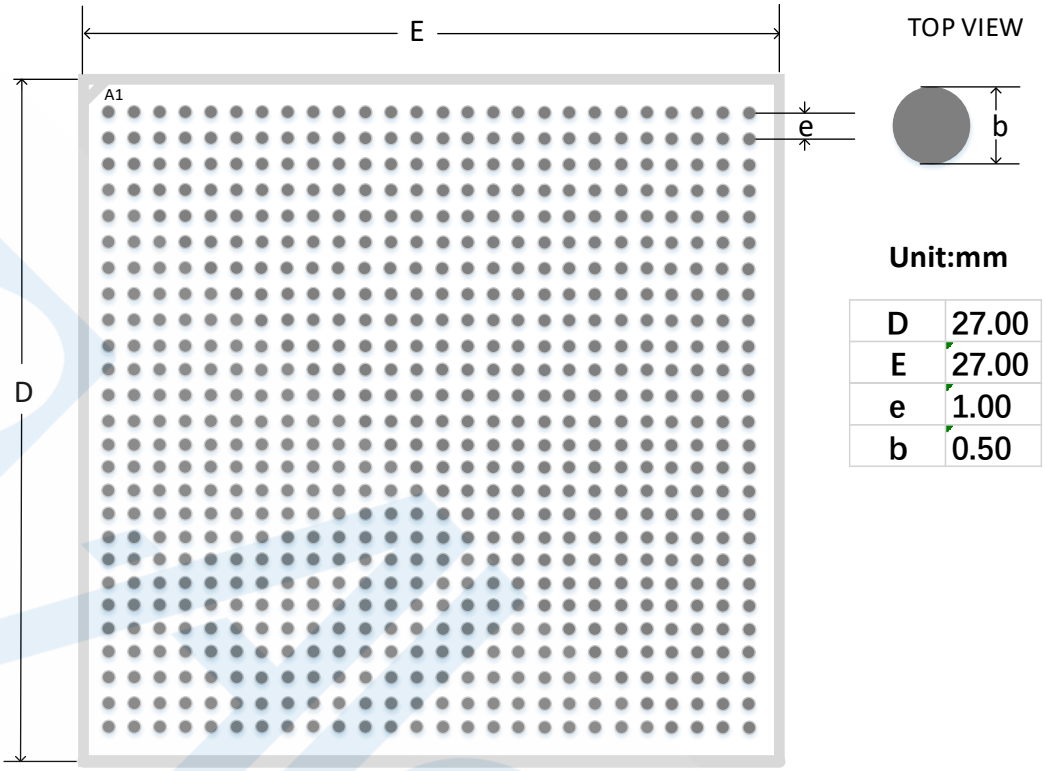
DETAIL A

10:1

Side View

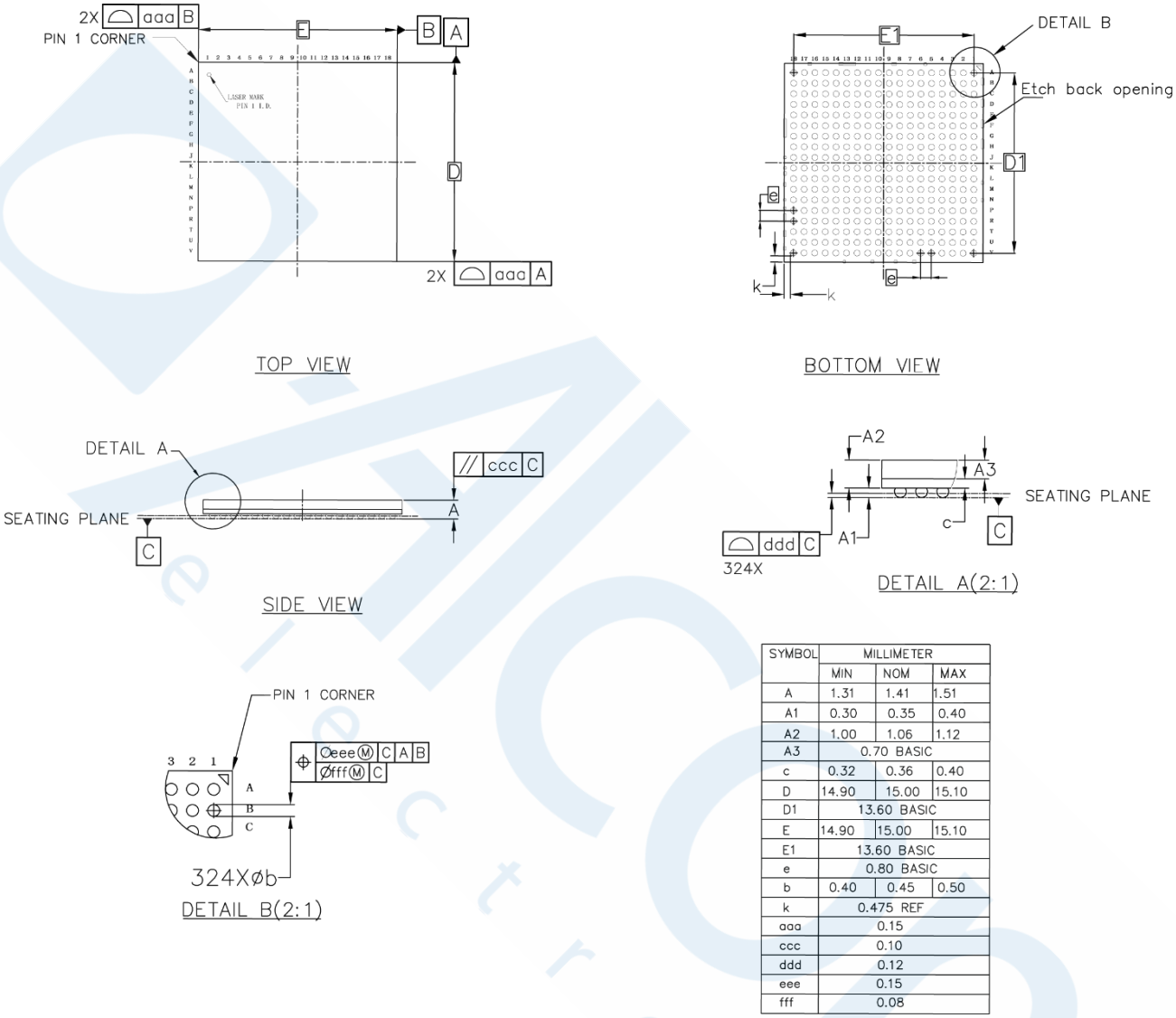
symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	2.380
A1	0.450	0.500	0.550
A2	1.120	1.170	1.220
c	0.510	0.560	0.610
D	26.800	27.000	27.200
D1	---	25.000	---
D2	23.800	24.000	24.200
D3	---	18.000	---
E	26.800	27.000	27.200
E1	---	25.000	---
E2	23.800	24.000	24.200
E3	---	18.000	---
e	---	1.000	---
b	0.550	0.600	0.650
aaa	0.200		
bbb	0.200		
ddd	0.200		
eee	0.250		
fff	0.100		
Ball Diam	0.600		
N	676		
MD/ME	26/26		

Figure 4-10 Recommended PCB Layout PG676A



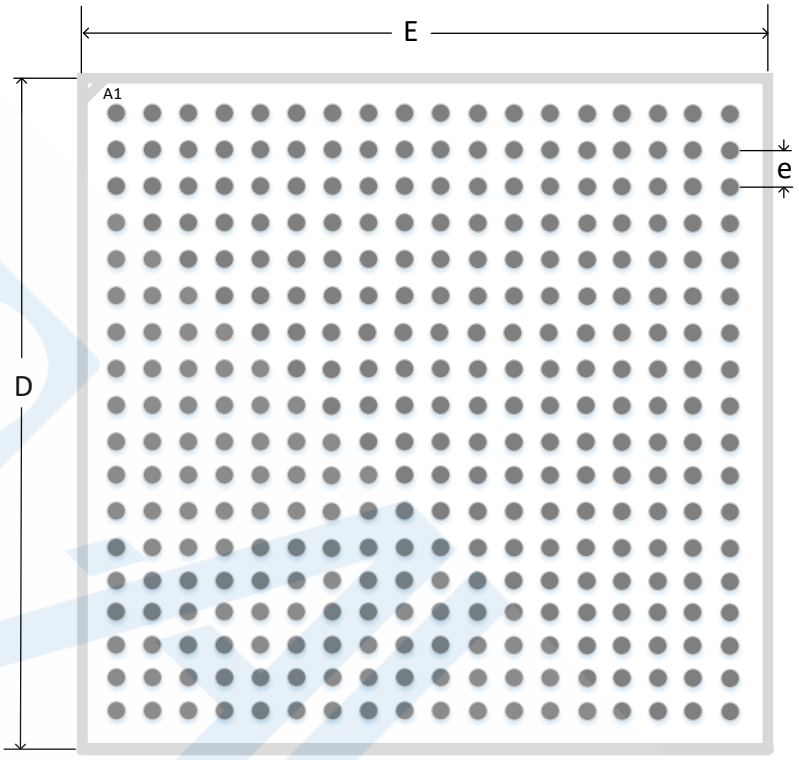
4.6 UG324A Package Outline (15mm x 15mm, GW5AT-138)

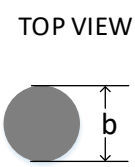
Figure 4-11 Package Outline UG324A



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.31	1.41	1.51
A1	0.30	0.35	0.40
A2	1.00	1.06	1.12
A3		0.70 BASIC	
c	0.32	0.36	0.40
D	14.90	15.00	15.10
D1		13.60 BASIC	
E	14.90	15.00	15.10
E1		13.60 BASIC	
e		0.80 BASIC	
b	0.40	0.45	0.50
k		0.475 REF	
aaa		0.15	
ccc		0.10	
ddd		0.12	
eee		0.15	
fff		0.08	

Figure 4-12 Recommended PCB Layout UG324A



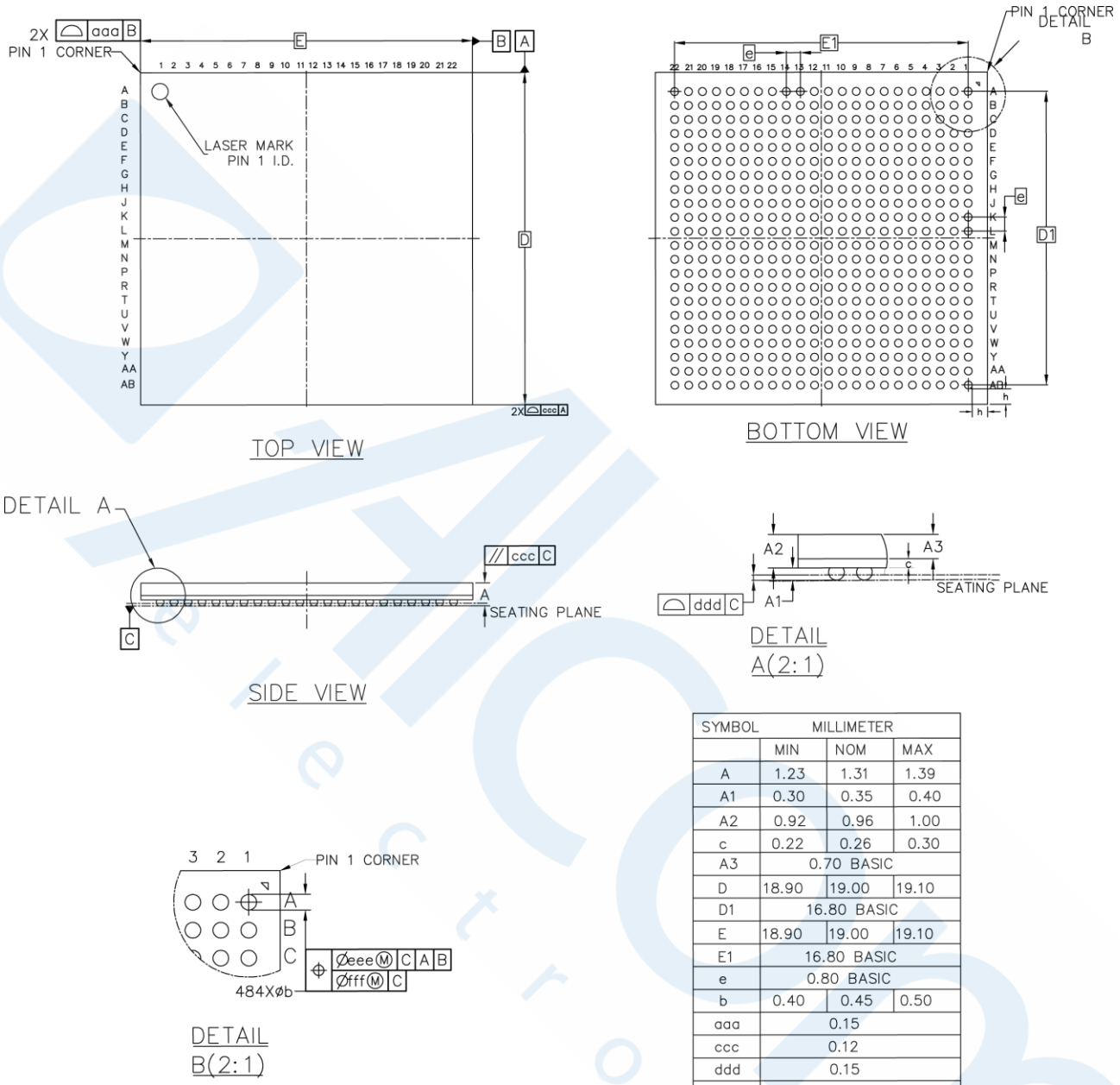


Unit:mm

D	15.00
E	15.00
e	0.80
b	0.40

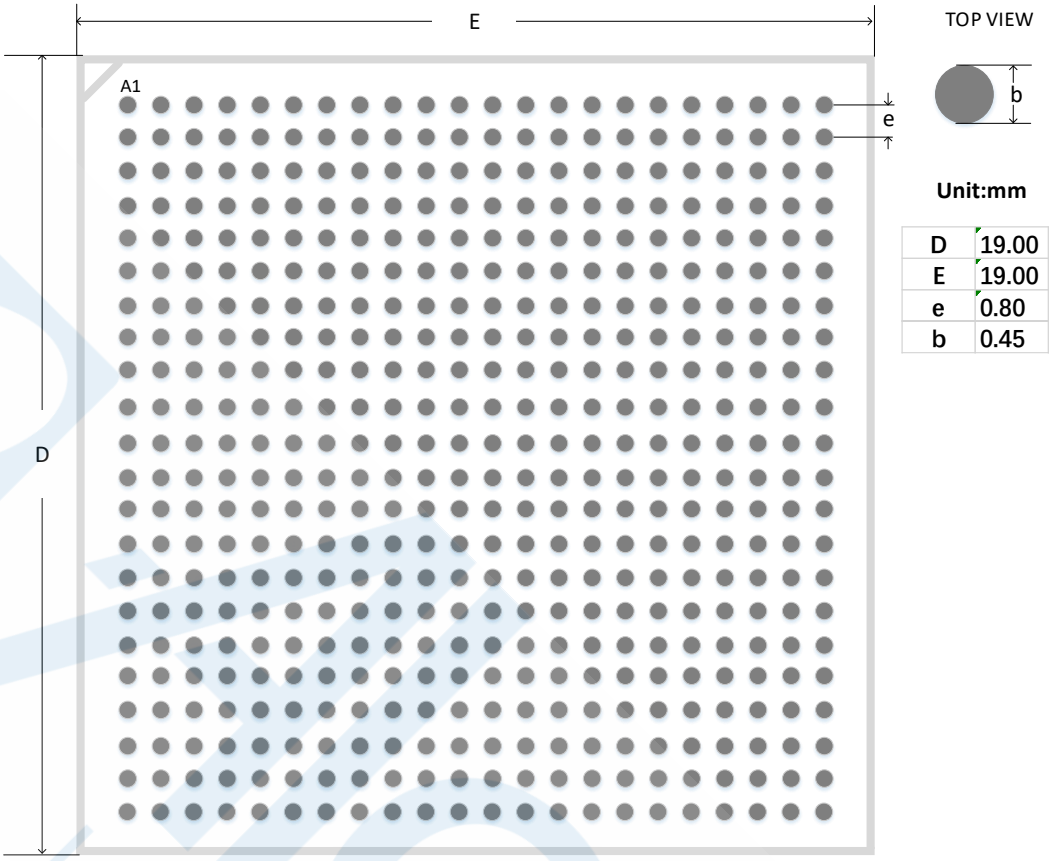
4.7 UG484 Package Outline (19mm x 19mm, GW5AT-75)

Figure 4-13 Package Outline UG484



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.23	1.31	1.39
A1	0.30	0.35	0.40
A2	0.92	0.96	1.00
c	0.22	0.26	0.30
A3	0.70 BASIC		
D	18.90	19.00	19.10
D1	16.80 BASIC		
E	18.90	19.00	19.10
E1	16.80 BASIC		
e	0.80 BASIC		
b	0.40	0.45	0.50
aaa	0.15		
ccc	0.12		
ddd	0.15		
eee	0.15		
fff	0.08		
h	0.875 REF		

Figure 4-14 Recommended PCB Layout UG484

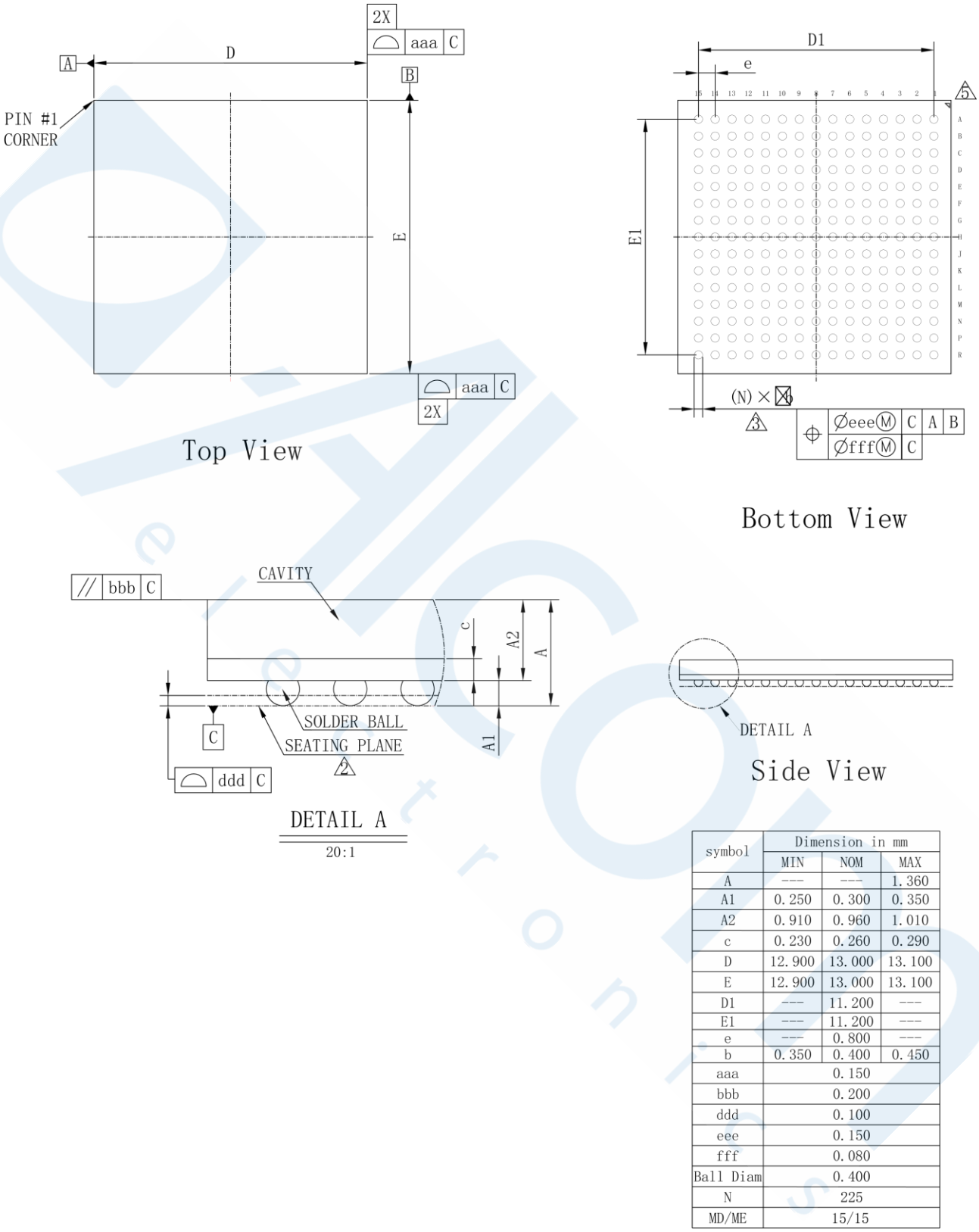


Unit:mm

D	19.00
E	19.00
e	0.80
b	0.45

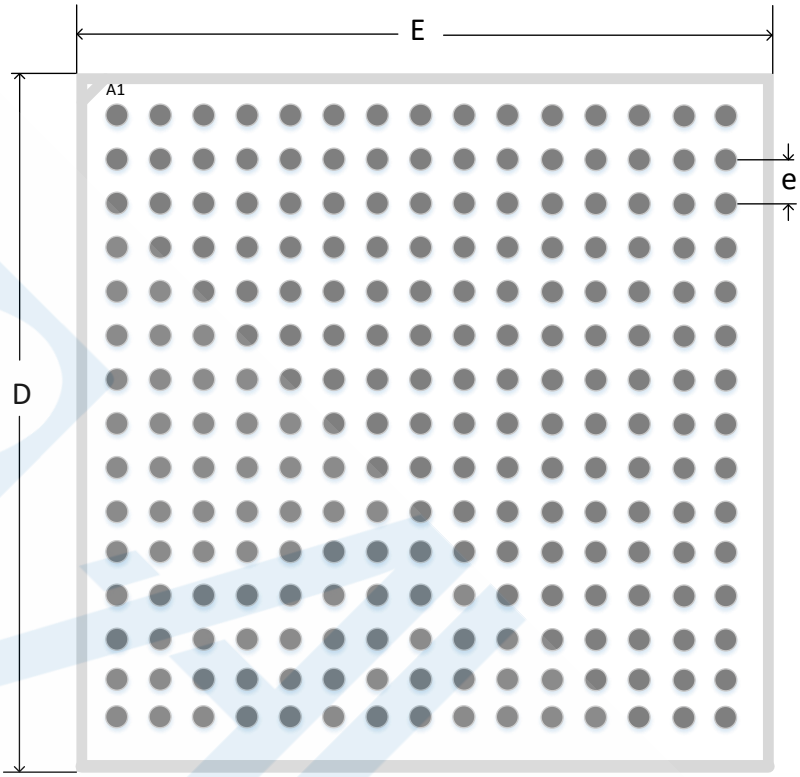
4.8 UG225 Package Outline (13mm x 13mm, GW5AT-60)

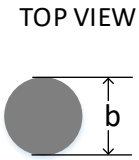
Figure 4-15 Package Outline UG225



symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.360
A1	0.250	0.300	0.350
A2	0.910	0.960	1.010
c	0.230	0.260	0.290
D	12.900	13.000	13.100
E	12.900	13.000	13.100
D1	---	11.200	---
E1	---	11.200	---
e	---	0.800	---
b	0.350	0.400	0.450
aaa	0.150		
bbb	0.200		
ddd	0.100		
eee	0.150		
fff	0.080		
Ball Diam	0.400		
N	225		
MD/ME	15/15		

Figure 4-16 Recommended PCB Layout UG225



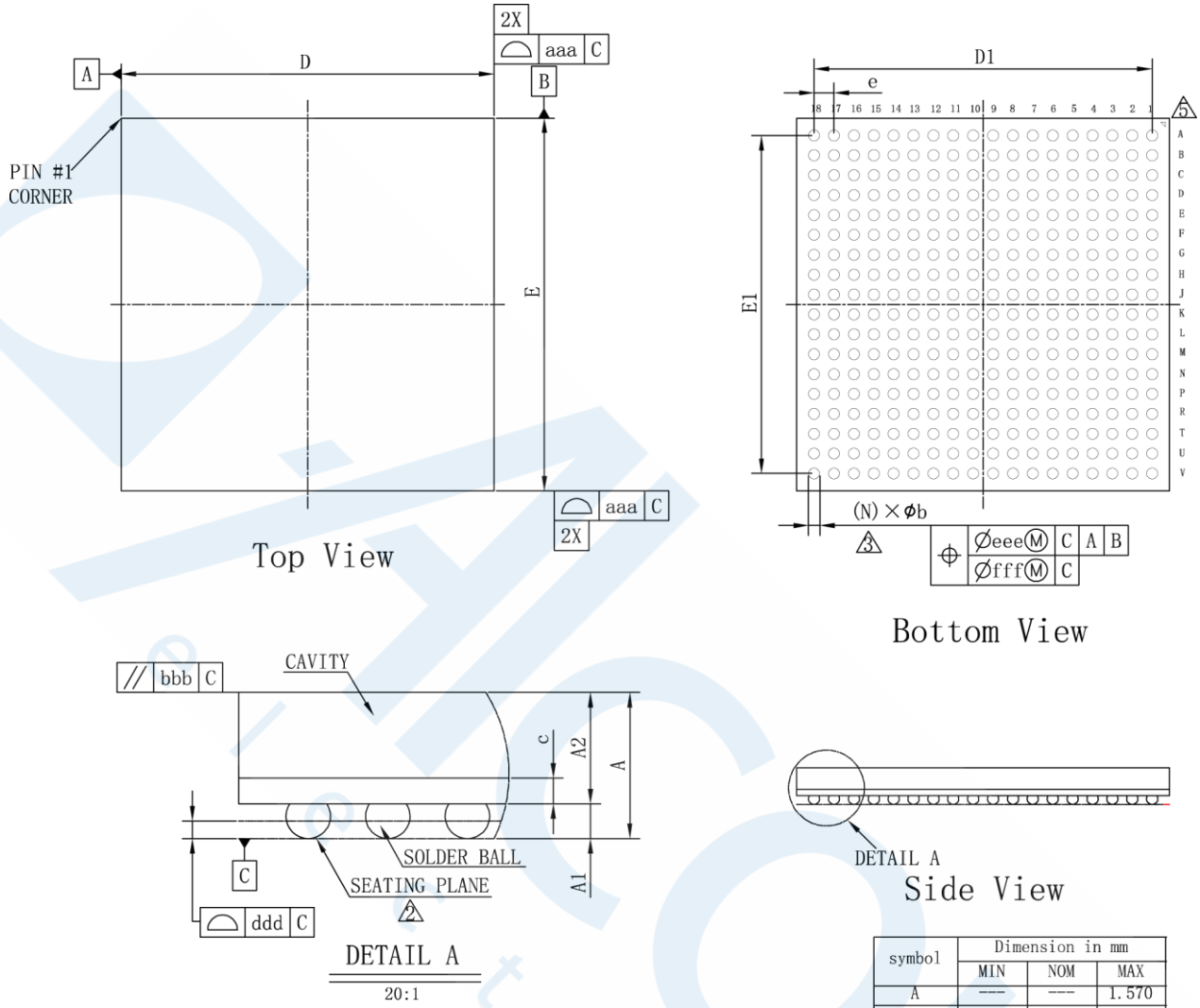


Unit:mm

D	13.00
E	13.00
e	0.80
b	0.35

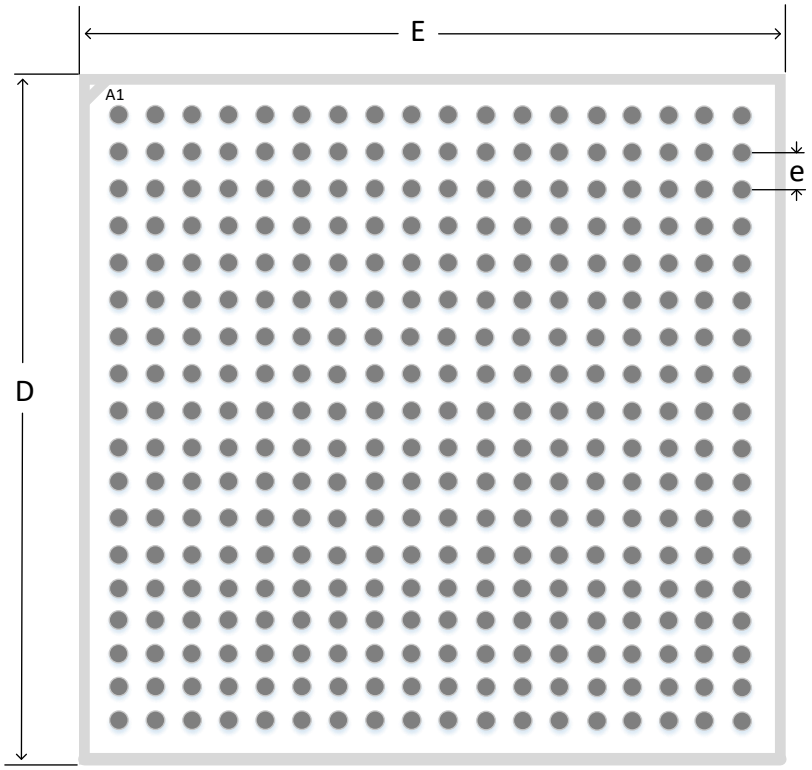
4.9 UG324S Package Outline (15mm x 15mm, GW5AT-60)

Figure 4-17 Package Outline UG324S



symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.570
A1	0.300	0.350	0.400
A2	1.070	1.120	1.170
c	0.230	0.260	0.290
D	14.900	15.000	15.100
E	14.900	15.000	15.100
D1	---	13.600	---
E1	---	13.600	---
e	---	0.800	---
b	0.400	0.450	0.500
aaa	0.150		
bbb	0.200		
ddd	0.200		
eee	0.150		
fff	0.080		
Ball Diam	0.450		
N	324		
MD/ME	18/18		

Figure 4-18 Recommended PCB Layout UG324S



Unit:mm

D	15.00
E	15.00
e	0.80
b	0.40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