GW2AN Series

The GW2AN series of FPGA products are the first generation non-volatile FPGA products of the Arora family. They offer a range of comprehensive features and rich internal resources, a high-speed LVDS interface, abundant BSRAM memory resources, and NOR Flash resources.

These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2AN series of FPGA products suitable for high-speed, low-cost applications. GOWIN continually invests the development of next-generation FPGA hardware environment through the market-oriented independent research and developments that supports the GW2AN series of FPGA products, which can be used for FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

GW2AN-55

GW2AN-55 is the first generation products of the Arora family. They offer a range of comprehensive features and rich internal resources like high-performance DSP resources, a high-speed LVDS interface, and abundant BSRAM memory resources. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make GW2AN-55 suitable for high-speed, low-cost applications. GOWINSEMI continually invests the development of next-generation FPGA hardware environment through the market-oriented independent research and developments that supports GW2AN-55, which can be used for FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- Lower power consumption
    - 55nm technology
    - EV version: Supports 1.0V core voltage;
    - LV version: Supports 1.2 V core voltage;
    - UV version: Supports5V and 3.3 V core voltage;
    - Clock dynamically turns on and off
- Multiple I/O standards

    - LVCMOS33/25/18/15/12;LVTTL33,SSTL33/25/18 I, II, SSTL15; HSTL18 I, II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE MLVDSE, LVPECLE, RSDSE
    - Input hysteresis option
    - Supports 4mA,8mA,16mA,24mA,etc. drive options
    - Slew rate option
    - Output drive strength option
    - Individual bus keeper, weak pull-up, weak pull-down, and open drain option
    -
    - Hot socket
- Abundant slices
    - Four input LUT (LUT4)
    - Double-edge flip-flops
    - Supports shift register and distributed register
- Integrate NOR Flash
- Block SRAM with multiple modes
    - Supports dual port, single port, and semi-dual port
    - Supports byte write enable
- Flexible PLLs
    - Frequency adjustment (multiply and division) and phase adjustment
    - Supports global clock
- Configuration
    - Supoprts JTAG configuration
    - Five GowinCONFIG configuration modes: SSPI, Autoboot, CPU, I^2C, SERIAL
    - Supoprts I^2C and SSPI background programing
    - Supports JTAG and SSPI programming SPI Flash directly and other modes programming SPI Flash via IP
    - Data stream file encryption and security bit settings

GW2AN Family Table

Device	GW2AN-9X	GW2AN-18X	GW2AN-55
LUT4	10368	20,736	54,720
Flip-Flop (FF)	10368	15,552	41,040
SSRAM(bits)	41472	41,472	109,440
BSRAM(bits)	450K	540K	2,520K
BSRAM quantity	25	30	140
NOR Flash	16M bit	16M bit	32M
PLLs	2	2	6
Global Clock	8	8	-
High Speed Clock	8	8	-
LVDS (Mb/s)	1250	1250	-
MIPI (Mb/s)	1200	1200	-
Total number of I/O banks	9	9	8
Max. I/O	384	384	608
Core voltage (EV)	1.0V	1.0V	1.0V
Core voltage (LV)	1.2V	1.2V	-
Core voltage (UV)	2.5V/3.3V	2.5V/3.3V	-

Package Options and Max I/O (* Refer to the latest datasheet for details)

Package	Pitch (mm)	Size(mm)	E-pad size (mm)	GW2AN-9X	GW2AN-18X	GW2AN-55
PG256	1.0	17 x 17	–	207(86)	207(86)	-
UG256	0.8	14 x 14	–	207(86)	207(86)	-
UG324	0.8	15 x 15	–	279(74)	279(74)	-
UG332	0.8	17 x 17	–	279(82)	279(82)	-
UG400	0.8	17 x 17	–	335(95)	335(95)	-
UG484	0.8	19 x 19	–	383(96)	383(96)	-
UG676	0.8	21 x 21	–	-	-	525（97）