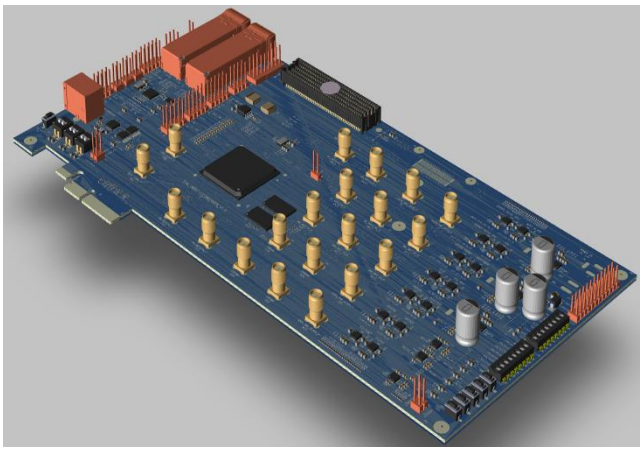
## *Arora-V 22nm High-Performance FPGA family*

Arora-V high performance FPGA family utilizing advanced 22nm SRAM technology and integrating 270Mbps-12.5Gbps high speed SerDes interfaces, PCIe 2.1 hard core with support for PCIe x1, x2, x8 modes, along with MIPI hard core single lane module at up to 2.5Gbps, and DDR3 interfacing at speeds up to 1333 Mbps.

The first device, GW5AT-138FC676, features 138K LUT logic resources, 6.4MB block RAM, 1.1MB distributed SRAM, along with advanced DSP blocks, and integrated ADC. Future family devices include 25K (non-Serdes) and 60K LUT devices.



## *Arora-V Device Package Schedule*

| Arora-V Series | Part Number | Package Compatibility | Sampling | Notes |
|---|---|---|---|---|
| *GW5AT-138 8CH Serdes* | GW5AT-LV138 FPG676A | Xilinx Artix-7 BGA676 | End-March 2023 | Flip-Chip Technology |
| | GW5AT-LV138 PG484A | Xilinx Artix-7 BGA484 | End-March 2023 | Flip-Chip Technology |
| | GW5AT LV138 UG324A | Xilinx Artix-7 BGA324 | April 2023 | Flip-Chip Technology |
| *GW5A-25 No Serdes* | GW5A-LV25 MG121N | Lattice Cross-link NX | End-March 2023 | Flip-Chip Technology |
| | GW5A-LV25 UG324S | Xilinx Spartan-6 BGA324 | End-March 2023 | Flip-Chip Technology |
| | GW5A LV25 UG256C | Altera Cyclone IV [4] BGA256 | April 2023 | Flip-Chip Technology |
| | GW5A LV25 PG256C | Altera Cyclone IV [4] BGA256 | May 2023 | Flip-Chip Technology |
| | GW5A LV25 UG256S | Xilinx Spartan-6 BGA256 | Q2 2023 | Flip-Chip Technology |
| | GW5A LV25 MG196S | Xilinx Spartan-6 MG196 | Early Q3 2023 | Flip-Chip Technology |
| *GW5AT-60 4CH Serdes* | GW5AT-LV60 PG484A | Xilinx Artix-7 BGA484 | Q4 2023 | Flip-Chip Technology |

*For more details see Arora V SRAM Based FPGA*

| Device | GW5A-25 | GW5AT-60 (SERDES) | GW5A-138 | GW5AT-138 (SERDES) |
|---|---|---|---|---|
| LUT4 | 23040 | 57600 | 138240 | 138240 |
| REG | 23040 | 57600 | 138240 | 138240 |
| SSRAM (bits) | 180K | 450K | 1105.92K | 1105.92K |
| BSRAM (bits) | 1008K | 2322K | 6120K | 6120K |
| BSRAM Quantity | 56 | 129 | 340 | 340 |
| DSP | #28 27bit x 18bit OR #28 27bit x 36bit OR #56 12bit x 12 bit | #120 27bit x 18bit | #298 27bit x 18bit OR #298 27bit x 36bit OR #596 12bit x 12 bit | #298 27bit x 18bit OR #298 27bit x 36bit OR #596 12bit x 12 bit |
| PLLs | 6 | 10 | 12 | 12 |
| Global Clock | 32 | 32 | 32 | 32 |
| High Speed Clock | 16 | 20 | 24 | 24 |
| Transceivers | 0 | 4 | 0 | 8 |
| Transceiver Speed | N/A | 270Mbps-12.5Gbps | N/A | 270Mbps-12.5Gbps |
| PCIe 2.1 Lanes | 0 | 1, x1, x2, x4 | 0 | 1, x1, x2, x4, x8 |
| LVDS Gbps | 1.25 | 1.25 | 1.25 | 1.25 |
| DDR3 Mbps | 1066 | 1333 | 1333 | 1333 |
| MIPI D PHY Hardcore | 2.5G | 2.5G | 2.5G | 2.5G |
| | 4 data lanes, 1 clock lane | 8 data lanes, 2 clock lane | 8 data lanes, 2 clock lanes | 8 data lanes, 2 clock lanes |
| ADC | 1 | 1 | 2 | 2 |
| I/O Banks | 9 | 5 | 6 | 6 |
| Max User I/O | 236 | 250 | 376 | 376 |
| Core Voltage | 0.9V/1.0V | 0.9V/1.0V | 0.9V/1.0V | 0.9V/1.0V |