



# GW2AR series of FPGA Products

## Data Sheet

DS226-2.3E, 10/11/2023

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ALLCO Electronics

## Revision History

Date	Version	Description
05/11/2018	1.1E	Initial version published.
08/01/2018	1.2E	<ul style="list-style-type: none"> <li>● PLL Structure diagram updated.</li> <li>● The description of the SystemIO status for blank chips updated.</li> </ul>
09/10/2018	1.3E	V <sub>CC02/6/7</sub> and V <sub>CCX</sub> of GW2AR-18 QN88 with SDRAM embedded are internal short circuited.
11/12/2018	1.4E	<ul style="list-style-type: none"> <li>● PSRAM added.</li> <li>● GW2AR-18 QN88P and EQ144P with PSRAM added.</li> <li>● Part Name updated.</li> </ul>
01/09/2019	1.5E	Reference manuals for memories updated.
04/01/2019	1.6E	<ul style="list-style-type: none"> <li>● Changed the operating temperature (Industrial) to junction temperature.</li> <li>● The package of EQ176 added.</li> </ul>
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05/25/2022	1.9.2E	<ul style="list-style-type: none"> <li>● Recommended I/O operating conditions updated.</li> <li>● Power supply ramp rates updated.</li> </ul>
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02/27/2023	2.2E	<ul style="list-style-type: none"> <li>● GW2AR-18 LQ144 and LQ176 removed.</li> <li>● Information on Slew Rate removed.</li> </ul>
10/10/2023	2.3E	<ul style="list-style-type: none"> <li>● Editorial updates.</li> <li>● Note about the default state of GPIOs modified.</li> <li>● 2.5.2 Memory Configuration Modes added.</li> <li>● The I/O logic output diagram and the I/O logic input diagram combined into Figure 2-5 I/O Logic Input and Output.</li> <li>● Section 2.5.6 Power up Conditions removed.</li> </ul>

Date	Version	Description
		<ul style="list-style-type: none"><li>● Table 3-3 Power Supply Ramp Rates updated.</li><li>● Note for Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions modified.</li><li>● Table 3-17 External Switching Characteristics updated.</li><li>● Figure 4-3 Package Marking Examples updated.</li></ul>



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# 1 General Description

The GW2AR series of FPGA products are the first generation products of the Arora family. The GW2AR devices are system-in-package chips with memory chips integrated into them based on the GW2A devices, featuring high-performance DSP resources, high-speed LVDS interfaces, and abundant BSRAM memory resources. These embedded resources combined with a streamlined FPGA architecture and 55nm process make the GW2AR series of FPGA products suitable for high-speed and low-cost applications.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

## 1.1 Features

- Lower power consumption
  - 55nm SRAM process
  - Core voltage: 1.0V
  - Supports dynamically turning on/off the clock
- System-in-package chips integrating SDRAMs/PSRAMs
- Multiple I/O standards
  - LVCMOS33/25/18/15/12; LVTTTL33, SSTL33/25/18 I, II, SSTL15; HSTL18 I, II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis options
  - Drive strength options
  - Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
  - Hot socketing
- High-performance DSP blocks
  - High-performance digital signal processing
  - Supports 9 x 9, 18 x 18, 36 x 36 bit multipliers and 54-bit accumulators
  - Supports cascading of multipliers
  - Supports pipeline mode and bypass mode
  - Pre-addition operation for the filter function
  - Supports barrel shifters

- Abundant basic logic cells
  - 4-input LUTs (LUT4s)
  - Supports shift registers and shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port mode, Single Port mode, and Semi-Dual Port mode
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clocks
- Configuration
  - JTAG configuration
  - Four GowinCONFIG configuration modes: SSPI, MSPI, CPU, SERIAL
  - Supports bitstream file encryption and security bit settings

## 1.2 Product Resources

Table 1-1 Product Resources

Device	GW2AR-18
LUT4s	20,736
Flip-Flops (FFs)	15,552
Shadow SRAM(SSRAM) Capacity (bits)	41,472
Block SRAM(BSRAM) Capacity(bits)	828K
Number of BSRAMs	46
SDR / DDR SDRAM(bits)	64M / 128M
PSRAM(bits)	64M
Multipliers(18 x 18 Multipliers)	48
Maximum PLLs <sup>[1]</sup>	4
I/O Banks	8
Maximum GPIOs	384
Core voltage	1.0V

**Note!**

[1] Different packages support different numbers of PLLs. Up to four PLLs can be supported.

**Table 1-2 Package-Memory Combinations**

Package	Device	Memory Type	Width	Capacity	Available PLLs
EQ144 <sup>[1]</sup>	GW2AR-18	SDR SDRAM	32 bits	64M bits	PLLL0/PLLL1/PLLR0/PLLR1
EQ144P <sup>[1][2]</sup>	GW2AR-18	PSRAM	16 bits	64M bits	
EQ144PF <sup>[1][2]</sup>	GW2AR-18	PSRAM	16 bits	64M bits	
QN88	GW2AR-18	SDR SDRAM	32 bits	64M bits	PLLL1/ PLLR1
QN88P <sup>[2]</sup>	GW2AR-18	PSRAM	16 bits	64M bits	
QN88PF <sup>[2]</sup>	GW2AR-18	PSRAM	16 bits	64M bits	
EQ176	GW2AR-18	DDR SDRAM	16 bits	128M bits	PLLL1/PLLR0/PLLR1

**Note!**

- [1]  $V_{CCPLL1}$  and  $V_{CC}$  of the EQ144/EQ144P/EQ144PF packages are internally short-circuited together. Please refer to Table 3-2 for details.
- [2] "P" indicates PSRAM; "F" indicates that some pins have been adjusted in QN88PF/EQ144PF compared with QN88P/EQ144P.

**Table 1-3 Device-Package Combinations, Maximum User I/Os, and (True LVDS Pairs)**

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW2AR-18
EQ144	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144P	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144PF	0.5	20 x 20	9.74 x 9.74	120(35)
QN88	0.4	10 x 10	6.74 x 6.74	66(22)
QN88P	0.4	10 x 10	6.74 x 6.74	66(22)
QN88PF	0.4	10 x 10	6.74 x 6.74	66(22)
EQ176	0.4	20 x 20	6 x 6	140(45)

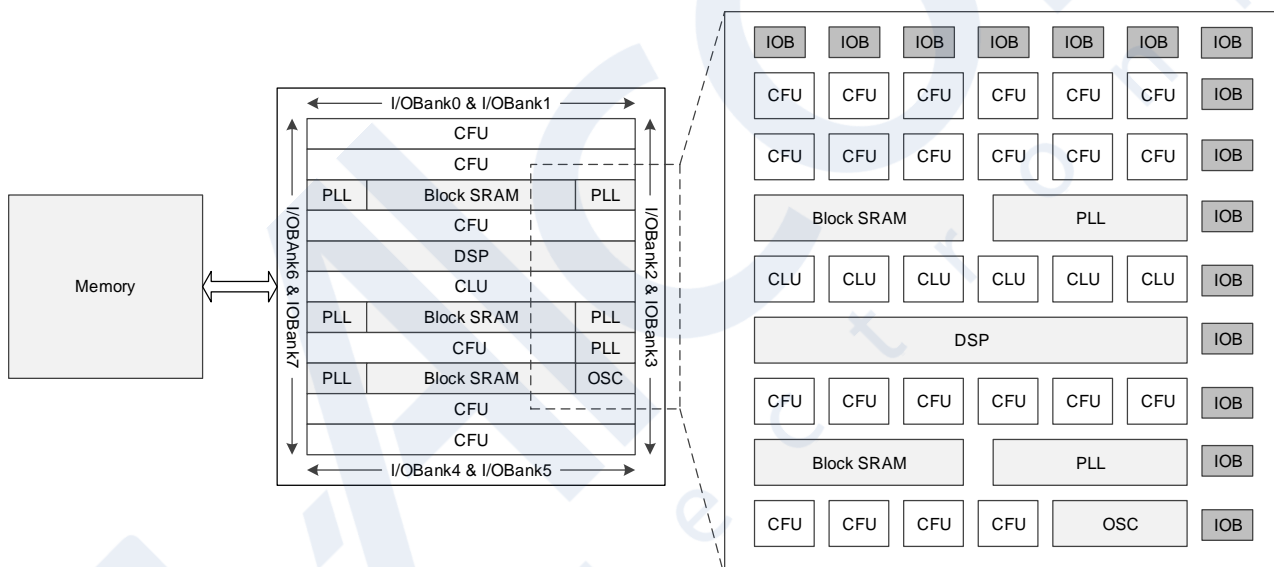
**Note!**

- [1] The package types in this manual are referred to by abbreviations, see [4.1 Part Naming](#) for more information.
- JTAGSEL\_N and JTAG pins cannot be used as GPIOs simultaneously. The number of maximum user I/Os noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as GPIOs. See [UG229, GW2AR series of FPGA Products Package and Pinout](#) for more details.

# 2 Architecture

## 2.1 Architecture Overview

Figure 2-1 Architecture Overview



As shown in Figure 2-1, the GW2AR device is a system-in-package (SIP) chip that combines the GW2A device and a memory chip. For the features of the memory chips, please refer to [2.2 Memory](#).

See Table 1-1 for more information on the resources provided. The core of the FPGA is an array of logic cells surrounded by IO blocks. Besides, BSRAMs, DSP blocks, PLLs, and an on-chip oscillator are provided.

The Configurable Function Unit (CFU) and the Configurable Logic Unit (CLU) are the two kinds of basic logic blocks that form the core of GW2AR FPGAs. Devices with different capacities have different numbers of rows and columns of CFUs/CLUs. For more information, see [2.3 Configurable Function Units](#).

The I/O resources in the GW2AR series of FPGA products are arranged around the periphery of the devices in groups referred to as

banks, which are divided into eight banks, including Bank0 - Bank7. The I/O resources support multiple I/O standards and can be used for regular mode, SDR mode, generic DDR mode, and DDR\_MEM mode. For more information, see [2.4 Input/Output Blocks](#).

BSRAMs are embedded as a row in the GW2AR series of FPGA products. Each BSRAM has a capacity of 18Kbits and supports multiple configuration modes and operation modes. For more information, see [2.5 Block SRAM](#).

The GW2AR series of FPGA products provide DSP blocks. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU. For more information, see [2.6 Digital Signal Processing](#).

The GW2AR series of FPGA products have embedded PLL resources. The PLLs can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by configuring the parameters. These FPGAs have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 2.5 MHz to 105MHz, providing clocking resources for the MSPI mode. It provides an MSPI clock source for the MSPI configuration mode with a tolerance of  $\pm 5\%$ . For more information, see [2.7 Clocks](#) and [2.11 On-chip Oscillator](#).

There are also abundant Configurable Routing Units (CRUs) that interconnect all the resources within the FPGA. For example, routing resources distributed in CFUs and IOBs interconnect resources in them. Routing resources can be automatically generated by the Gowin software. In addition, the GW2AR series of FPGA products also provide abundant dedicated clock resources, long wires (LWs), global set/reset (GSR) resources, programming options, etc. For more details, see [2.7 Clocks](#), [2.8 Long Wires](#), and [2.9 Global Set/Reset](#).

## 2.2 Memory

The GW2AR series of FPGA products in different packages have different capacities and types of memory. Please refer to [1.2 Product Resources](#) for more information.

### 2.2.1 SDR SDRAM

#### Features

- Access time: 5.4ns/5.4ns
- Clock frequency: 166 MHz
- Data width: 32bits
- Capacity: 64Mbits
- Synchronous Operation
- Internal pipelined architecture
- Four internal banks (512K x 32bits x 4 banks)
- Programmable mode
  - Column address strobe latency: 2 or 3
  - Burst lengths: 1, 2, 4, 8, or full page
  - Burst type: sequential mode or interleaved mode

- Burst-Read-Single-Write
- Burst stop function
- Byte masking function
- Auto refresh and self refresh
- 4,096 refresh cycles/64 ms
- 3.3V±0.3V power supply<sup>[1]</sup>
- LVTTTL Interface

**Note!**

[1] For more information about the power supply, please refer to Table 3-2.

**Overview**

The SDR SDRAM integrated in the GW2AR series of FPGA Products is a high-speed CMOS synchronous DRAM with a capacity of 64M bits. The SDR SDRAM consists of four banks with each bank containing 512K x 32 bits. Each bank is organized as 2048 rows x 256 columns x 32 bits. Burst accesses are supported. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The SDRAM provides read or write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto pre-charge function may be enabled to provide a self-timed row pre-charge that is initiated at the end of the burst sequence. Both the auto-refresh and self-refresh functions are easy to use. Besides, by using a programmable mode register, the system can choose the most suitable modes to maximize its performance.

The supply voltage for the SDR SDRAM interface is 3.3V, and the I/O Bank voltage that connects to the SDR SDRAM needs to be 3.3V. For more details, please refer to Table 3-2.

The IP Core Generator integrated in the Gowin Software supports a SDR SDRAM controller IP that can interface to both embedded and external SDRAMs. This controller IP can be used for the SDRAM power-up initialization, activation, auto-refresh, etc. For more information, please refer to [IPUG279, Gowin SDRAM Controller User Guide](#).

## 2.2.2 DDR SDRAM

**Features**

- Clock frequency: 250MHz/ 200MHz
- Data width: 16bits
- Capacity: 128M bits
- Differential clock input: CLK and ~CLK
- Bi-directional DQS
- Synchronous Operation
- Internal pipelined architecture
- Four internal banks, 2M x 16 bits for each bank
- Programmable Mode and Extended Mode registers
  - Column address strobe latency: 2, 2.5, 3
  - Burst lengths: 2, 4, 8
  - Burst type: sequential mode or interleaved mode

- Byte masking function
- DM Write Latency = 0
- Auto refresh and self refresh
- 4,096 refresh cycles/64 ms
- Pre-charge power down & active power down
- 2.5V±0.2V power supply<sup>[1]</sup>
- SSTL\_2 interface

**Note!**

[1] For more information about the power supply, please refer to Table 3-2.

**Overview**

The DDR SDRAM integrated in the GW2AR series of FPGA products is a high-speed CMOS synchronous DRAM with a capacity of 128M bits. The DDR SDRAM consists of four banks with each bank containing 2M x16 bits. Data outputs occur at the rising edges of both CLK and ~CLK. Burst accesses are supported. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. Read or write burst lengths of 2, 4, or 8 are supported. An auto pre-charge function may be enabled to provide a self-timed row pre-charge that is initiated at the end of the burst sequence. Both the auto-refresh and self-refresh functions are easy to use. Besides, by using a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance.

The supply voltage for the DDR SDRAM interface is 2.5V, and the I/O Bank voltage that connects to the DDR SDRAM needs to be 2.5V. For more details, please refer to Table 3-2.

The IP Core Generator integrated in the Gowin Software supports a DDR controller IP that can interface to both embedded and external SDRAMs. This controller IP can be used for the DDR power-up initialization, read calibration, auto-refresh, etc. For more information, please refer to [IPUG507, Gowin DDR Memory Interface IP User Guide](#).

## 2.2.3 PSRAM

**Features**

- Clock frequency: 166MHz, DDR332
- Double Data Rate
- Data width: 16bits
- Read-write data strobe (RWDS)
- Temperature compensated refresh
- Partial array self-refresh (PASR)
- Hybrid sleep mode
- Deep power down(DPD)
- Drive strengths: 35, 50, 100, and 200 Ohm
- Burst access
- Burst lengths: 16/32/64/128
- Status/control registers
- 1.8V power supply<sup>[1]</sup>

**Note!**

[1] For more information about the power supply, please refer to Table 3-2.

The supply voltage for the PSRAM interface is 1.8V, and the I/O Bank voltage that connects to the PSRAM needs to be 1.8V. For more details, please refer to Table 3-2.

The IP Core Generator integrated in the Gowin Software supports a PSRAM controller IP that can interface to both embedded and external PSRAMs. This controller IP can be used for the PSRAM power-up initialization, read calibration, etc. For more information, please refer to [IPUG525, Gowin HyperRAM & PSRAM Memory Interface IP User Guide](#).

## 2.3 Configurable Function Units

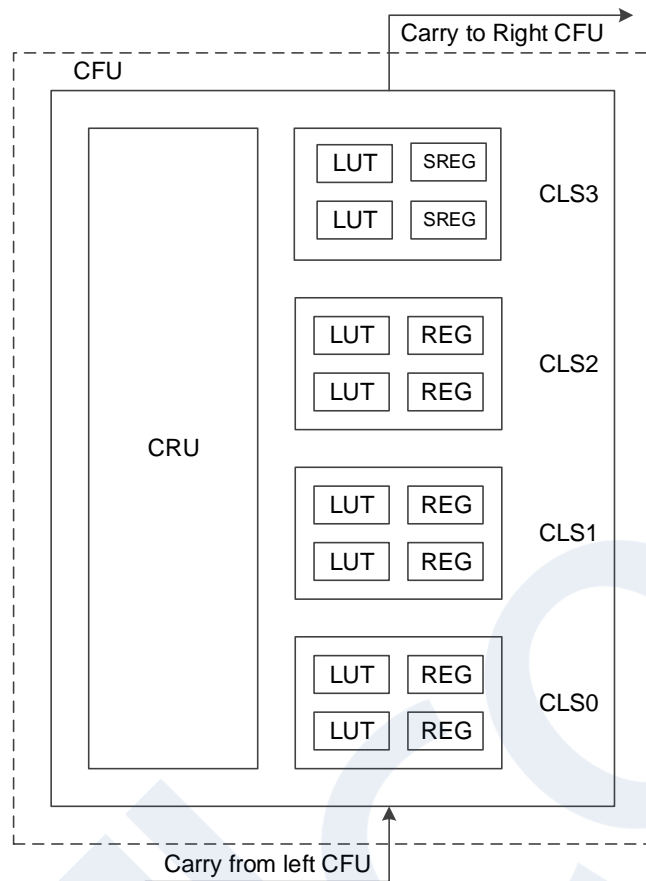
Configurable Function Units (CFUs) and/or Configurable Logic Units (CLUs) are the basic cells for the core of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs). Each of the three CLSs contains two 4-input LUTs and two registers, and the other one only contains two 4-input LUTs, as shown in Figure 2-2.

The CLSs in the CLUs cannot be configured as SRAMs, but can be configured as basic LUTs, ALUs, and ROMs. The CLSs in the CFUs can be configured as basic LUTs, ALUs, SRAMs, and ROMs according to application scenarios.

For more information on the CFUs, see [UG288, Gowin Configurable Function Unit \(CFU\) User Guide](#).



Figure 2-2 CFU Structure View

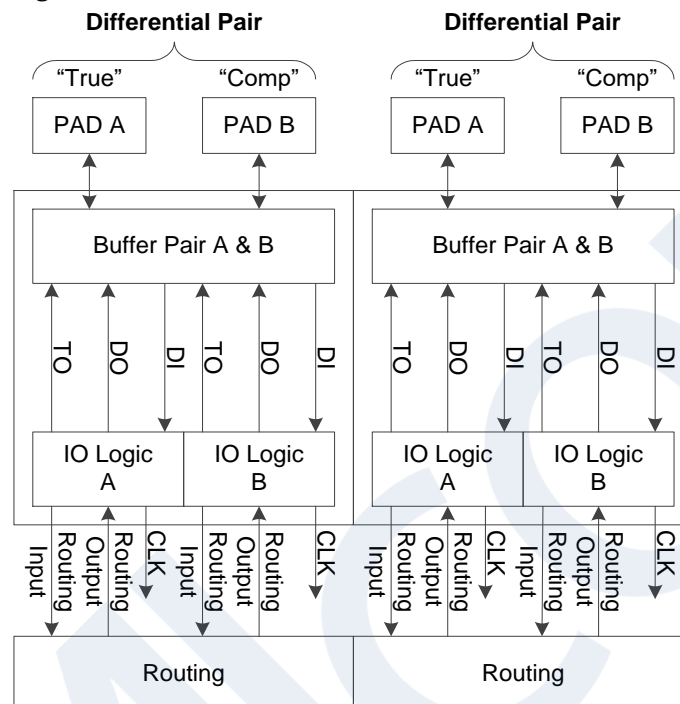
**Note!**

The SREGs need special patch support. Please contact Gowin's technical support or local office for this patch.

## 2.4 Input/Output Blocks

The Input/Output Block (IOB) in the GW2AR series of FPGA products consists a buffer pair, IO logic, and corresponding routing units. As shown below, each IOB connects to two pins (marked as A and B), which can be used as a differential pair or as two single-ended inputs/outputs.

Figure 2-3 IOB Structure View



The features of the IOB include:

- $V_{CCIO}$  supplied with Each bank
- LVCMOS, PCI, LVTTTL, LVDS, SSTL, HSTL, etc.
- Input hysteresis options
- Drive strength options
- Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
- Hot socketing
- IO logic supports basic mode, SDR mode, DDR mode, etc.

2.4.1 - 2.4.3 describe I/O standards, I/O logic, and I/O logic modes.

For more information about the IOB, please refer to [UG289, Gowin Programmable IO \(GPIO\) User Guide](#).

### 2.4.1 I/O Standards

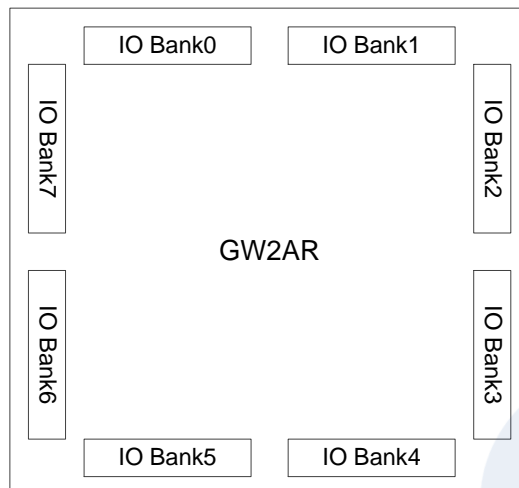
There are eight I/O Banks in the GW2AR series of FPGA products, as shown in Figure 2-4. Each bank has its own I/O power supply  $V_{CCIO}$ .  $V_{CCIO}$  can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V.

$V_{CCX}$  and  $V_{CCIO}$  that power the SDR SDRAM need to be set to 3.3V, see [2.2.1 SDR SDRAM](#).

$V_{CCX}$  and  $V_{CCIO}$  that power the DDR SDRAM need to be set to 2.5V, see [2.2.2 DDR SDRAM](#).

To support SSTL, HSTL, etc., Each bank also has one independent voltage source ( $V_{REF}$ ) as the reference voltage. You can choose to use the internal  $V_{REF}$  ( $0.5 \times V_{CCIO}$ ) or the external  $V_{REF}$  input via any IO from the bank.  $V_{CCX}$  supports 2.5V and 3.3V.

**Figure 2-4 I/O Bank Distribution View of GW2AR**



Different banks in the GW2AR series of FPGA Products support different on-die termination settings, including single-ended resistors and differential resistors. Single-ended resistors are set for SSTL/HSTL input/output and are supported in Bank2/3/6/7. Differential resistors are set for LVDS input and are only supported in Bank 0/1, see [UG289, Gowin Programmable IO User Guide](#) for more details.

**Note!**

During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O states are controlled by user programs and constraints. The states of configuration-related I/Os differ depending on the configuration mode.

For the  $V_{CCIO}$  requirements of different I/O standards, see Table 2-1 and

Table 2-2.

**Table 2-1 Output I/O Standards and Configuration Options**

I/O standard (output)	Single-ended /Differential	Bank $V_{CCIO}(V)$	Drive Strength (mA)	Supports Hysteresis options?	Needs $V_{REF}$ ?	Typical Applications
LVTTTL33	Single-ended	3.3	4,8,12,16,24	Yes	No	Universal interface
LVC MOS33	Single-ended	3.3	4,8,12,16,24	Yes	No	Universal interface
LVC MOS25	Single-ended	2.5	4,8,12,16	Yes	No	Universal interface
LVC MOS18	Single-ended	1.8	4,8,12	Yes	No	Universal interface
LVC MOS15	Single-ended	1.5	4,8	Yes	No	Universal interface
LVC MOS12	Single-ended	1.2	4,8	Yes	No	Universal interface

I/O standard (output)	Single-ended /Differential	Bank V <sub>CCIO</sub> (V)	Drive Strength (mA)	Supports Hysteresis options?	Needs V <sub>REF</sub> ?	Typical Applications
SSTL25_I	Single-ended	2.5	8	No	Yes	Memory interface
SSTL25_II	Single-ended	2.5	8	No	Yes	Memory interface
SSTL33_I	Single-ended	3.3	8	No	Yes	Memory interface
SSTL33_II	Single-ended	3.3	8	No	Yes	Memory interface
SSTL18_I	Single-ended	1.8	8	No	Yes	Memory interface
SSTL18_II	Single-ended	1.8	8	No	Yes	Memory interface
SSTL15	Single-ended	1.5	8	No	Yes	Memory interface
HSTL18_I	Single-ended	1.8	8	No	Yes	Memory interface
HSTL18_II	Single-ended	1.8	8	No	Yes	Memory interface
HSTL15_I	Single-ended	1.5	8	No	Yes	Memory interface
PCI33	Single-ended	3.3	N/A	Yes	No	PC and embedded system
LVPECL33E	Differential	3.3	16	No	No	High-speed data transmission
MLVDS25E	Differential	2.5	16	No	No	LCD timing driver interface and column driver interface
BLVDS25E	Differential	2.5	16	No	No	Multi-point high-speed data transmission
RSDS25E	Differential	2.5	8	No	No	High-speed point-to-point data transmission
LVDS25E	Differential	2.5	8	No	No	High-speed point-to-point data transmission
LVDS25	Differential	2.5/3.3	3.5/2.5/2/1.25	No	No	High-speed point-to-point data transmission
RSDS	Differential	2.5/3.3	2	No	No	High-speed point-to-point data transmission
MINILVDS	Differential	2.5/3.3	2	No	No	LCD timing driver interface and column driver interface

I/O standard (output)	Single-ended /Differential	Bank V <sub>CCIO</sub> (V)	Drive Strength (mA)	Supports Hysteresis options?	Needs V <sub>REF</sub> ?	Typical Applications
PPLVDS	Differential	2.5/3.3	3.5	No	No	LCD row/column driver
SSTL15D	Differential	1.5	8	No	No	Memory interface
SSTL25D_I	Differential	2.5	8	No	No	Memory interface
SSTL25D_II	Differential	2.5	8	No	No	Memory interface
SSTL33D_I	Differential	3.3	8	No	No	Memory interface
SSTL33D_II	Differential	3.3	8	No	No	Memory interface
SSTL18D_I	Differential	1.8	8	No	No	Memory interface
SSTL18D_II	Differential	1.8	8	No	No	Memory interface
HSTL18D_I	Differential	1.8	8	No	No	Memory interface
HSTL18D_II	Differential	1.8	8	No	No	Memory interface
HSTL15D_I	Differential	1.5	8	No	No	Memory interface

Table 2-2 Input I/O Standards and Configuration Options

I/O standard (input)	Single-ended /Differential	Bank V <sub>CCIO</sub> (V)	Supports Hysteresis Options?	Needs V <sub>REF</sub> ?
LVTTL33	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVC MOS33	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVC MOS25	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVC MOS18	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVC MOS15	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVC MOS12	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single-ended	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single-ended	2.5/3.3	No	Yes
SSTL25_II	Single-ended	2.5/3.3	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
SSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
SSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL15_I	Single-ended	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single-ended	3.3	Yes	No
LVDS	Differential	2.5/3.3	No	No
RS DS	Differential	2.5/3.3	No	No

I/O standard (input)	Single-ended /Differential	Bank V <sub>CCIO</sub> (V)	Supports Hysteresis Options?	Needs V <sub>REF</sub> ?
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No

## 2.4.2 I/O Logic

Figure 2-5 shows the I/O logic input and output of the GW2AR series of FPGA products.

Figure 2-5 I/O Logic Input and Output

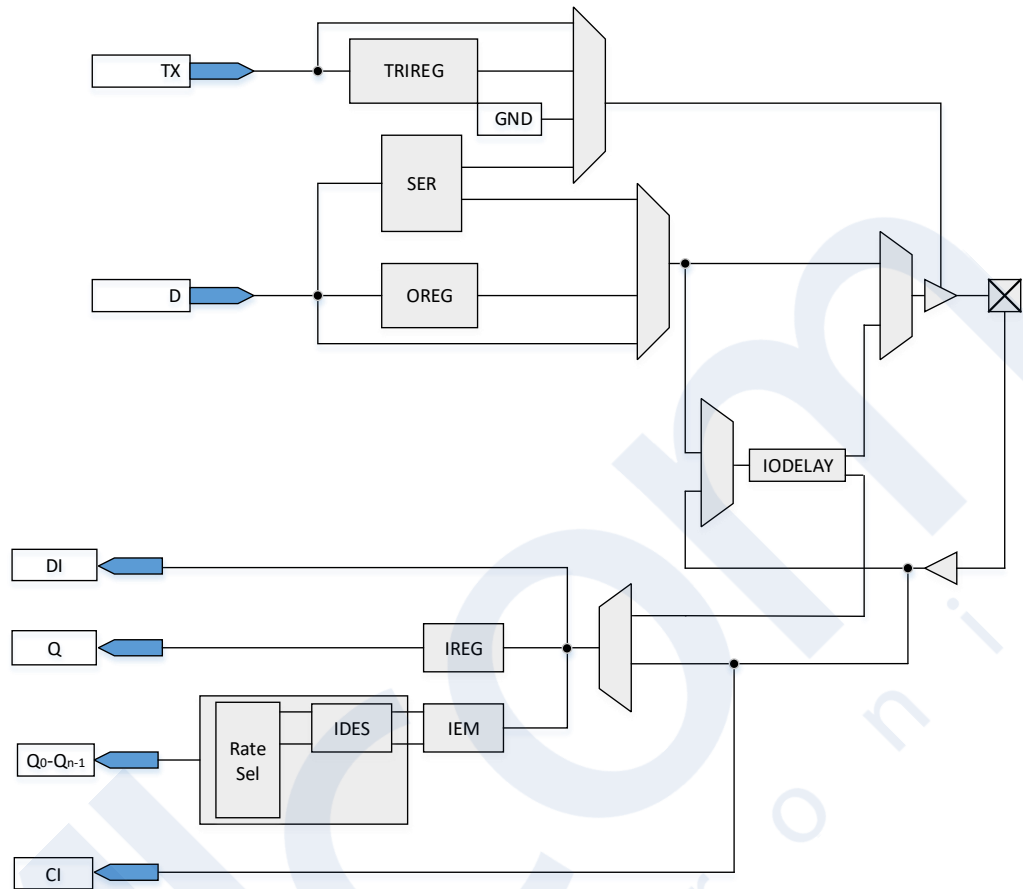


Table 2-3 Port Description

Port	I/O	Description
C <sub>I</sub> [1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to <a href="#">UG115, GW2AR-18 Pinout</a> .
DI	Input	IO port low-speed input signal input into the fabric directly.
Q	Output	IREG output signal in the SDR module.
Q <sub>0</sub> -Q <sub>n-1</sub>	Output	IDES output signal in the DDR module.

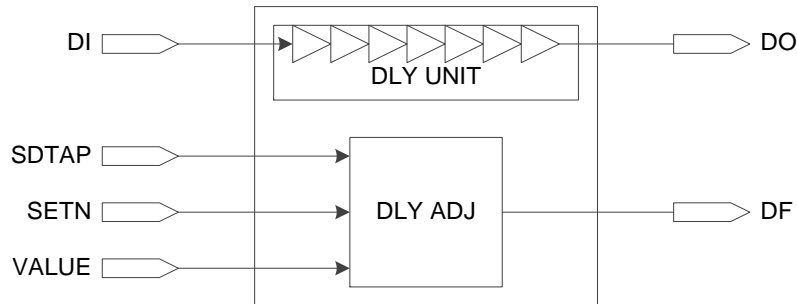
**Note!**

When CI is used as GCLK input, DI, Q, and Q<sub>0</sub>-Q<sub>n-1</sub> cannot be used as I/O input and output.

Descriptions of the I/O logic modules of the GW2AR series of FPGA products are presented below.

**IODELAY**

See Figure 2-6 for an overview of the IODELAY module. Each I/O of the GW2AR series of FPGA products has an IODELAY module, providing a total of 128(0~127) steps of delay, with one step of delay time being about 18ps.

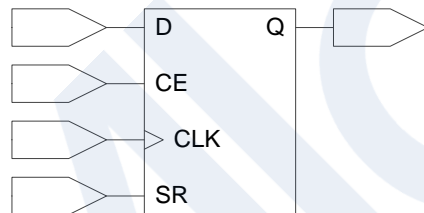
**Figure 2-6 IODELAY Diagram**

There are two ways to control the delay:

- Static control.
- Dynamic control: can be used with the IEM module to adjust the dynamic sampling window. The IODELAY module cannot be used for both input and output at the same time.

### I/O Register

See Figure 2-7 for the I/O register in the GW2AR series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and one tristate register (TRIREG).

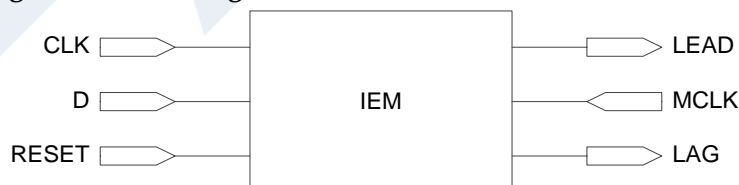
**Figure 2-7 I/O Register Diagram**

#### Note!

- CE can be programmed as either active low (0: enable) or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.
- SR can be programmed as either synchronous/asynchronous SET/RESET or disabled.
- The register can be programmed as a register or a latch.

### IEM

The IEM(Input Edge Monitor) module is used to sample data edges and is used in generic DDR mode, as shown in Figure 2-8.

**Figure 2-8 IEM Diagram**

### Deserializer(DES) and Clock Domain Transfer

This series of FPGA products provide a simple deserializer(DES) for input I/O logic to support advanced I/O protocols. The clock domain



transfer module of the input clock in DES provides the ability to safely switch the external sampling clock(strobe) to the internal continuous running clock. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- The internal continuous clock is used instead of the discontinuous DQS for data sampling. This feature applies to the DDR memory interface.
- For the DDR3 memory interface standard, align the data after read-leveling.
- In generic DDR mode, when DQS.RCLK is used for sampling, the clock domain transfer module also needs to be used.

Each DQS provides WADDR and RADDR signals for the clock domain transfer module in the same group.

### SER

This series of FPGA products provide a simple serializer(SER) for output I/O logic to support advanced I/O protocols.

## 2.4.3 I/O Logic Modes

The I/O Logic of the GW2AR series of FPGA products supports several operation modes. In each operation mode, the I/O (or I/O differential pair) can be configured as output, input, INOUT or tristate output (output signal with tristate control).

## 2.5 Block SRAM

### 2.5.1 Introduction

The GW2AR series of FPGA products provide abundant block SRAM resources. These memory resources are distributed as blocks throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). Each BSRAM block occupies 3 CFU locations. The capacity of each BSRAM can be up to 18,432 bits (18K bits). There are five operation modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, ROM mode, and FIFO mode.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. The features of BSRAMs include:

- Up to 18,432 bits per BSRAM
- Clock frequency up to 380MHz (230MHz in Read-before-write mode)
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port mode
- Provides parity bits
- Supports ROM Mode
- Data widths from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode

- Byte Enable function for double-byte and above data
- Normal read and write mode
- Read-before-write mode
- Write-through mode

For more information on the BSRAMs, see [UG285, Gowin BSRAM & SSRAM User Guide](#).

## 2.5.2 Memory Configuration Modes

BSRAMs in the GW2AR series of FPGA products support various data widths, see Table 2-4.

**Table 2-4 Memory Size Configuration**

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	ROM Mode
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

### Single Port Mode

The single port mode supports 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In single port mode, writing to or reading from one port at one clock edge is supported. During the write operation, the written data will be transferred to the output of the BSRAM. When the output register is bypassed, the new data will show up at the same write clock rising edge.

For more information on single port mode, please refer to [UG285, Gowin BSRAM & SSRAM User Guide](#).

### Dual Port Mode

The dual port mode supports 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode). The applicable operations are as follows:

- Two independent read operations
- Two independent write operations
- An independent read operation and an independent write operation

#### Note!

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address.

For more information on dual port mode, please refer to [UG285,](#)

## Gowin BSRAM & SSRAM User Guide.

### Semi-Dual Port Mode

The semi-dual port mode supports 2 read modes (bypass mode and pipeline mode) and 1 write mode (normal mode). Semi-dual port mode supports simultaneous read and write operations in the form of writing to port A and reading from port B.

#### Note!

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address.

For more information on semi-dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

### ROM Mode

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization is completed during the device power-on process.

Each BSRAM can be configured as one 16Kbits ROM. For more information on ROM mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

## 2.5.3 Mixed Data Width Configuration

The BSRAMs in the GW2AR series of FPGA products support mixed data width operations. In dual port mode and semi-dual port mode, the data widths for read and write can be different, see Table 2-5 and Table 2-6.

Table 2-5 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

#### Note!

"\*" denotes the modes supported.

Table 2-6 Semi-dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512 x 32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

**Note!**

"\*" denotes the modes supported.

## 2.5.4 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

## 2.5.5 Synchronous Operation

- All the input registers of BSRAMs support synchronous write.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypass-able.

## 2.5.6 BSRAM Operation Modes

The BSRAM supports five different operations, including two read modes (Bypass mode and Pipeline mode) and three write modes (Normal mode, Write-Through mode, and Read-before-Write mode).

### Read Mode

The following two read modes are supported.

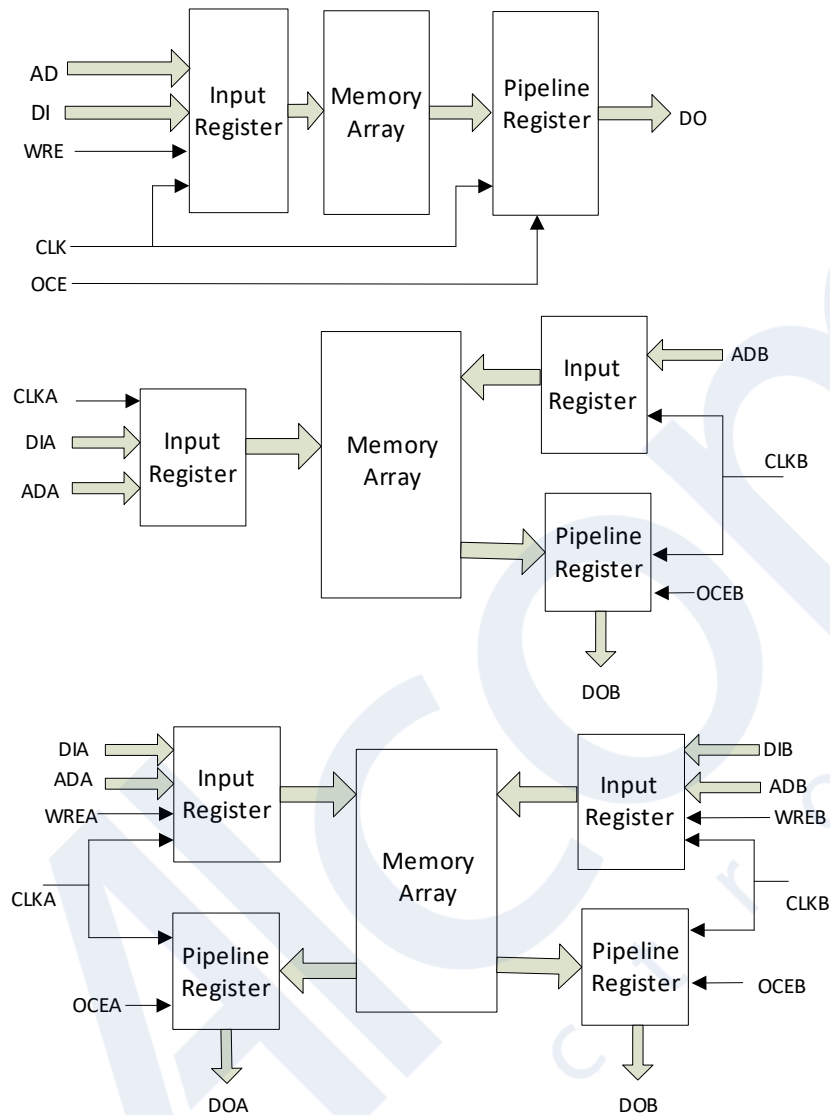
#### PIPELINE MODE

When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

#### BYPASS MODE

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

**Figure 2-9 Pipeline Mode in Single Port Mode, Dual Port Mode, and Semi-dual Port Mode**



## Write Mode

### NORMAL MODE

In this mode, when you write data to one port, the output data of this port does not change. The written data will not appear at the read port.

### WRITE-THROUGH MODE

In this mode, when you write data to one port, the written data will appear at the output of this port.

### READ-BEFORE-WRITE MODE

In this mode, when you write data to one port, the written data will be stored in the memory according to the address, and the original data in this address will appear at the output of this port.

### 2.5.7 Clock Mode

Table 2-7 lists the clock modes in different BSRAM modes:

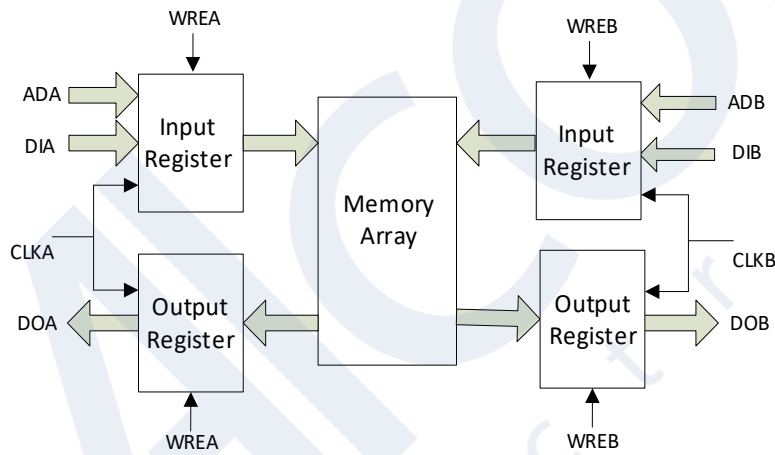
**Table 2-7 Clock Modes in Different BSRAM Modes**

Clock Mode	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

#### Independent Clock Mode

Figure 2-10 shows the independent clock operation in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

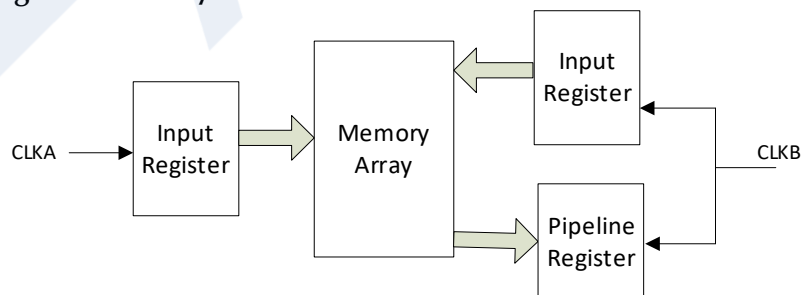
**Figure 2-10 Independent Clock Mode**



#### Read/Write Clock Mode

Figure 2-11 shows the read/write clock operation in semi-dual port mode with one clock at each port. The write clock (CLKA) controls data inputs, write addresses and read/write enable signals of Port A. The read clock (CLKB) controls data outputs, read addresses, and read enable signals of Port B.

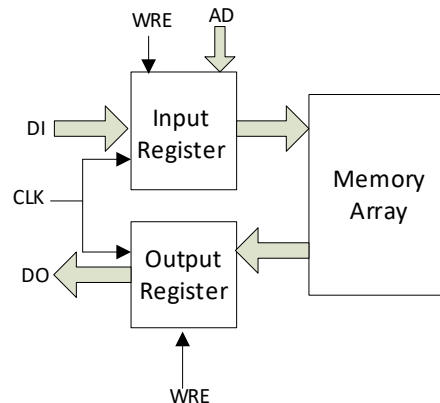
**Figure 2-11 Read/Write Clock Mode**



### Single Port Clock Mode

Figure 2-12 shows the clock operation in single port mode.

Figure 2-12 Single Port Clock Mode



## 2.6 Digital Signal Processing

### 2.6.1 Introduction

GW2AR devices provide abundant DSP resources. Gowin's DSP solutions can address high-performance digital signal processing needs such as FIR and FFT designs. The DSP resources have the advantages of stable timing performance, high resource utilization, and low power consumption.

The DSP resources offer the following functions:

- Multipliers with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data widths
- Barrel shifters
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

#### Macro

The DSP blocks are distributed throughout the FPGA array in the form of rows. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

### Pre-adder

Each DSP macro contains two pre-adders for implementing pre-addition, pre-subtraction, and shifting.

The pre-adders are located at the first stage with two input ports:

- Parallel 18-bit input B or SIB
- Parallel 18-bit input A or SIA

Each input port supports pipeline mode and bypass mode.

Gowin's pre-adders can be used independently as function blocks, which support 9-bit and 18-bit width.

### Multiplier

The multipliers are located after the pre-adders. The multipliers can be configured as  $9 \times 9$ ,  $18 \times 18$ ,  $36 \times 18$ , or  $36 \times 36$ . Register mode and bypass mode are supported in both input and output ports. The configuration modes that a macro supports include:

- One  $18 \times 36$  multiplier
- Two  $18 \times 18$  multipliers
- Four  $9 \times 9$  multipliers

Two macros can form one  $36 \times 36$  multiplier.

### Arithmetic Logic Unit

Each DSP macro contains one 54-bit ALU, which can further enhance multipliers' functions. Register mode and bypass mode are supported in both input and output ports. The functions include:

- Addition/subtraction operations of multiplier output data/0, data A, and data B
- Addition/subtraction operations of multiplier output data/0, data B, and carry C
- Addition/subtraction operations of data A, data B, and carry C

## 2.6.2 DSP Operation Modes

Based on the two control signals (ALUSEL[6:0] and ALUMODE[3:0]), the DSP blocks can be configured as different operation modes.

- Multiplier mode
- Multiply accumulator mode
- Multiply-add accumulator mode

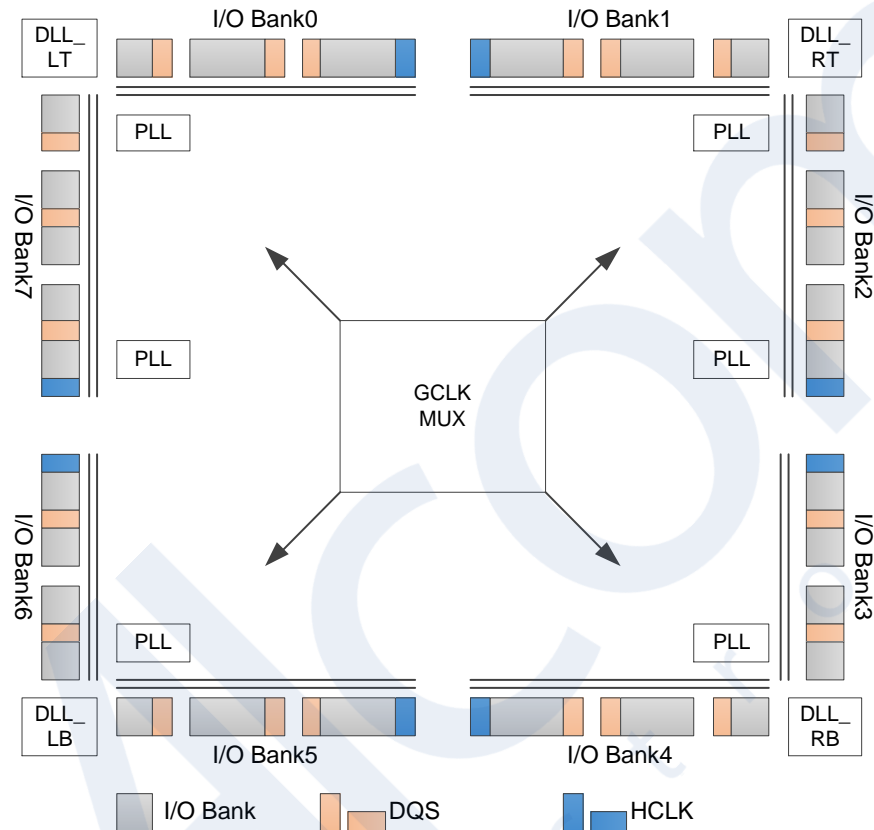
For more information on the DSP resources, see [UG287, Gowin Digital Signal Processing \(DSP\) User Guide](#).



## 2.7 Clocks

The clock resources and wiring are critical for high-performance applications in FPGA. The GW2AR series of FPGA products provide global clocks (GCLKs) which connect to all the registers directly. In addition, high-speed clocks (HCLKs), PLLs, DQSSs, etc. are provided.

Figure 2-13 GW2AR Clock Resources



### 2.7.1 Global Clocks

The Global Clock (GCLK) resources are distributed in the device as four quadrants. Each quadrant provides eight GCLKs. The clock sources of GCLKs include dedicated clock input pins and CRUs, and better clock performance can be achieved by using the dedicated clock input pins.

### 2.7.2 Phase-locked Loop

The PLL (Phase-locked Loop) is one kind of feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

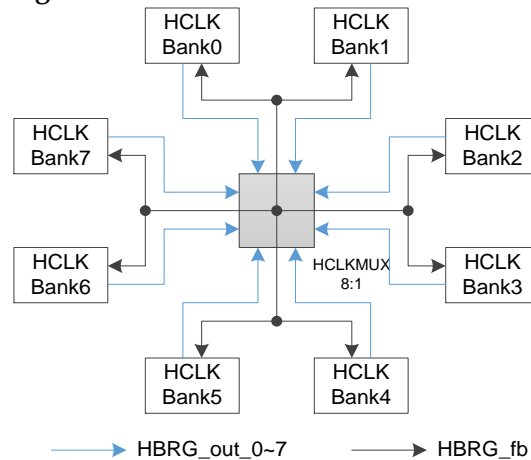
PLLs in the GW2AR series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

### 2.7.3 High-speed Clocks

The high-speed clocks (HCLKs) can support high-performance data

transmission of I/Os and are mainly suitable for source synchronous data transmission protocols, see Figure 2-14.

**Figure 2-14 GW2AR HCLK Distribution**



As shown in Figure 2-14, there is an 8:1 HCLKMUX module in the middle of the HCLK. HCLKMUX can send the HCLK signal in any bank to any other bank, which makes the use of HCLK more flexible.

The function modules that are available for the HCLK resources include:

- DHCEN: A dynamic enable module for the high-speed clocks. Its function is similar to DQCE. It is used to turn on/off the high-speed clock signal dynamically.
- CLKDIV/ CLKDIV2: A frequency division module for the high-speed clocks. Each bank has a CLKDIV. It is used to generate a frequency-divided clock with the same phase as the input clock, which is used in the IO logic mode.
- DCS: A dynamic selector for the high-speed clocks.
- DLLDLY: A dynamic delay adjustment module, used for the clock signals input via the dedicated clock pins.

## 2.7.4 DDR Memory Interface Clock Management(DQS)

The DQS module of the GW2AR series of FPGA products provides the following features to support the clock requirements of the DDR memory interface:

- Receives DQS inputs, sorts out waveforms and shifts 1/4 phase
- Provides read/write pointers for the input buffer
- Provides a data valid signal for internal logic
- Provides DDR output clock signals
- Supports DDR3 write voltage control

The DQS module supports multiple modes for different I/O interfaces.

For more information on the GCLKs, HCLKs, and DQSs, see [UG286](#).

Gowin Clock User Guide.

## 2.8 Long Wires

As a supplement to the CRU, the GW2AR series of FPGA products provide another kind of routing resource - the long wire, which can be used for clock, clock enable, set/reset, or other high fan out signals.

## 2.9 Global Set/Reset

The GW2AR series of FPGA products offer a dedicated global set/reset (GSR) network that connects directly to the device's internal logic and can be used as asynchronous/synchronous set or asynchronous/synchronous reset, with the registers in the CFUs and I/Os being able to be configured independently.

## 2.10 Programming & Configuration

The GW2AR series of FPGA products support SRAM configuration, and the configuration data needs to be re-downloaded upon each power-up. Of course, you can also save the configuration data in an external Flash. After power-up, the GW2AR device loads the configuration data from the external Flash to the SRAM.

Besides JTAG, the GW2AR series of FPGA products also support GOWINSEMI's own GowinCONFIG configuration modes: SSPI, MSPI, CPU, SERIAL. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

## 2.11 On-chip Oscillator

The GW2AR series of FPGA products have an embedded programmable on-chip clock oscillator which provides a clock source for the MSPI configuration mode. See Table 2-8 for the output frequencies. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is used to get the output clock frequency:

$$f_{\text{out}}=250\text{MHz}/\text{Param.}$$

**Note!**

“Param” should be even numbers from 2 to 128.

**Table 2-8 Output Frequency Options of the On-chip Oscillator**

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz <sup>[1]</sup>	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz <sup>[2]</sup>

**Note!**

- [1] The default frequency is 2.5MHz.
- [2] 125MHz is not suitable for the MSPI configuration mode.

# 3 AC/DC Characteristics

## Note!

Please ensure that you use Gowin's devices within the recommended operating conditions and ranges. Data beyond the working conditions and ranges are for reference only. Gowin does not guarantee that all devices will operate normally beyond the operating conditions and ranges.

## 3.1 Operating Conditions

### 3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V <sub>CC</sub>	Core voltage	-0.5V	1.1V
V <sub>CCPLL</sub>	PLL Voltage	-0.5V	1.1V
V <sub>CCIO</sub>	I/O bank voltage	-0.5V	3.75V
V <sub>CCX</sub>	Auxiliary voltage	-0.5V	3.75V
-	I/O voltage applied <sup>[1]</sup>	-0.5V	3.75V
Storage Temperature	Storage temperature	-65°C	+150°C
Junction Temperature	Junction temperature	-40°C	+125°C

## Note!

[1] Overshoot and undershoot of -2V to (V<sub>IHMAX</sub> + 2)V are allowed for a duration of <20 ns.

### 3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V <sub>CC</sub>	Core voltage	0.95V	1.05V
V <sub>CCPLLx</sub>	Left PLL Voltage	0.95V	1.05V
V <sub>CCPLLRx</sub>	Right PLL Voltage	0.95V	1.05V
V <sub>CCIOx</sub>	I/O bank voltage	1.14V	3.6V
V <sub>CCX</sub>	Auxiliary voltage	2.7V	3.6V
T <sub>JCOM</sub>	Junction temperature (commercial operation)	0°C	+85°C
T <sub>JIND</sub>	Junction temperature (industrial operation)	-40°C	+100°C

**Note!**

For more information on the power supplies, please refer to [UG115, GW2AR-18 Pinout](#).

### 3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
V <sub>CC</sub> Ramp	Power supply ramp rates for V <sub>CC</sub>	0.1mV/μs	-	10mV/μs
V <sub>CCIO</sub> /V <sub>CCX</sub> Ramp	Power supply ramp rates for V <sub>CCIO</sub> and V <sub>CCX</sub>	0.01mV/μs	-	100mV/μs

**Note!**

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 3-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

### 3.1.4 Hot Socketing Specifications

Table 3-4 Hot Socketing Specifications

Name	Description	Condition	I/O Type	Max.
I <sub>HS</sub>	Input or I/O leakage current	$0 < V_{IN} < V_{IH}(MAX)$	I/O	150 $\mu$ A
I <sub>HS</sub>	Input or I/O leakage current	$0 < V_{IN} < V_{IH}(MAX)$	TDI, TDO, TMS, TCK	120 $\mu$ A

### 3.1.5 POR Specifications

Table 3-5 POR Parameters

Name	Description	Name	Min.	Max.
POR Voltage	Power on reset ramp up trip point	VCC	0.7V	0.88V
		VCCX	2.1V	2.6V
		VCCIO	0.85V	0.98V

## 3.2 ESD performance

Table 3-6 GW2AR ESD - HBM

Device	GW2AR-18
EQ144/EQ144P/EQ144PF	HBM>1,000V
QN88/QN88P/QN88PF	HBM>1,000V
EQ176	HBM>1,000V

Table 3-7 GW2AR ESD - CDM

Device	GW2AR-18
EQ144/EQ144P/EQ144PF	CDM>500V
QN88/QN88P/QN88PF	CDM>500V
EQ176	CDM>500V

## 3.3 DC Characteristics

### 3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

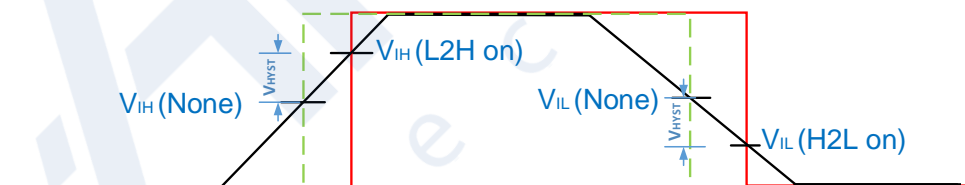
Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I <sub>IL</sub> , I <sub>IH</sub>	Input or I/O leakage	$V_{CCIO} < V_{IN} < V_{IH}(MAX)$	-	-	210 $\mu$ A
		$0V < V_{IN} < V_{CCIO}$	-	-	10 $\mu$ A
I <sub>PU</sub>	I/O Active Pull-up Current	$0 < V_{IN} < 0.7V_{CCIO}$	-30 $\mu$ A	-	-150 $\mu$ A
I <sub>PD</sub>	I/O Active Pull-down Current	$V_{IL}(MAX) < V_{IN} < V_{CCIO}$	30 $\mu$ A	-	150 $\mu$ A
I <sub>BHLS</sub>	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}(MAX)$	30 $\mu$ A	-	-
I <sub>BHHS</sub>	Bus Hold High Sustaining Current	$V_{IN} = 0.7V_{CCIO}$	-30 $\mu$ A	-	-
I <sub>BHLO</sub>	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	-	-	150 $\mu$ A

Name	Description	Condition	Min.	Typ.	Max.
IBHHO	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	-	-	-150 $\mu$ A
V <sub>BHT</sub>	Bus Hold Trip Points	-	V <sub>IL</sub> (MAX)	-	V <sub>IH</sub> (MIN)
C1	I/O Capacitance	-	-	5pF	8pF
V <sub>HYST</sub>	Hysteresis for Schmitt Trigger inputs	V <sub>CCIO</sub> =3.3V, Hysteresis=L2H <sup>[1],[2]</sup>	-	240mV	-
		V <sub>CCIO</sub> =2.5V, Hysteresis=L2H	-	140mV	-
		V <sub>CCIO</sub> =1.8V, Hysteresis=L2H	-	65mV	-
		V <sub>CCIO</sub> =1.5V, Hysteresis=L2H	-	30mV	-
		V <sub>CCIO</sub> =3.3V, Hysteresis=H2L <sup>[1],[2]</sup>	-	200mV	-
		V <sub>CCIO</sub> =2.5V, Hysteresis=H2L	-	130mV	-
		V <sub>CCIO</sub> =1.8V, Hysteresis=H2L	-	60mV	-
		V <sub>CCIO</sub> =1.5V, Hysteresis=H2L	-	40mV	-
		V <sub>CCIO</sub> =3.3V, Hysteresis=HIGH <sup>[1],[2]</sup>	-	440mV	-
		V <sub>CCIO</sub> =2.5V, Hysteresis=HIGH	-	270mV	-
		V <sub>CCIO</sub> =1.8V, Hysteresis=HIGH	-	125mV	-
		V <sub>CCIO</sub> =1.5V, Hysteresis=HIGH	-	70mV	-

**Note!**

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see [SUG935, Gowin Design Physical Constraints User Guide](#).
- [2] Enabling the L2H (low to high) option means raising V<sub>IH</sub> by V<sub>HYST</sub>; enabling the H2L (high to low) option means lowering V<sub>IL</sub> by V<sub>HYST</sub>; enabling the HIGH option means enabling both L2H and H2L options, i.e. V<sub>HYST</sub>(HIGH) = V<sub>HYST</sub>(L2H) + V<sub>HYST</sub>(H2L). The diagram is shown below.



### 3.3.2 Static Current

Table 3-9 Static Current

Name	Description	Device	Typ.
I <sub>CC</sub>	V <sub>CC</sub> current (V <sub>CC</sub> =1V)	GW2AR-18	70mA
I <sub>CCX</sub>	V <sub>CCX</sub> current (V <sub>CCX</sub> =3.3V)	GW2AR-18	15mA
I <sub>CCIO</sub>	V <sub>CCIO</sub> current (V <sub>CCIO</sub> =3.3V)	GW2AR-18	<2mA

**Note!**

Test conditions: room temperature, speed grade C8/I7.



### 3.3.3 Recommended I/O Operating Conditions

Table 3-10 Recommended I/O Operating Conditions

Name	Output $V_{CCIO}$ (V)			Input $V_{REF}$ (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTTL33	3.135	3.3	3.6	-	-	-
LVC MOS33	3.135	3.3	3.6	-	-	-
LVC MOS25	2.375	2.5	2.625	-	-	-
LVC MOS18	1.71	1.8	1.89	-	-	-
LVC MOS15	1.425	1.5	1.575	-	-	-
LVC MOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

### 3.3.4 Single-ended I/O DC Characteristics

Table 3-11 Single-ended I/O DC Characteristics

Name	$V_{IL}$		$V_{IH}$		$V_{OL}$ (Max)	$V_{OH}$ (Min)	$I_{OL}^{[1]}$ (mA)	$I_{OH}^{[1]}$ (mA)							
	Min	Max	Min	Max											
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	$V_{CCIO}-0.4V$	4	-4							
							8	-8							
							12	-12							
							16	-16							
					24	-24									
					0.2V	$V_{CCIO}-0.2V$	0.1	-0.1							
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	$V_{CCIO}-0.4V$	4	-4							
							8	-8							
							12	-12							
							16	-16							
										0.2V	$V_{CCIO}-0.2V$	0.1	-0.1		
LVCMOS18	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	3.6V	0.4V	$V_{CCIO}-0.4V$	4	-4							
							8	-8							
							12	-12							
												0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
					LVCMOS15	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	3.6V	0.4V	$V_{CCIO}-0.4V$	4	-4		
8	-8														
												0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
LVCMOS12	-0.3V	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	3.6V						0.4V	$V_{CCIO}-0.4V$	2	-2		
					4	-4									
												0.2V	$V_{CCIO}-0.2V$	0.1	-0.1
					PCI33	-0.3V	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	3.6V	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5		
SSTL33_I	-0.3V	$V_{REF}-0.2V$	$V_{REF}+0.2V$	3.6V	0.7	$V_{CCIO}-1.1V$	8	-8							
SSTL25_I	-0.3V	$V_{REF}-0.18V$	$V_{REF}+0.18V$	3.6V	0.54V	$V_{CCIO}-0.62V$	8	-8							
SSTL25_II	-0.3V	$V_{REF}-0.18V$	$V_{REF}+0.18V$	3.6V	NA	NA	NA	NA							
SSTL18_II	-0.3V	$V_{REF}-0.125V$	$V_{REF}+0.125V$	3.6V	NA	NA	NA	NA							
SSTL18_I	-0.3V	$V_{REF}-0.125V$	$V_{REF}+0.125V$	3.6V	0.40V	$V_{CCIO}-0.40V$	8	-8							
SSTL15	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	0.40V	$V_{CCIO}-0.40V$	8	-8							
HSTL18_I	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	0.40V	$V_{CCIO}-0.40V$	8	-8							
HSTL18_II	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	NA	NA	NA	NA							
HSTL15_I	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	0.40V	$V_{CCIO}-0.40V$	8	-8							
HSTL15_II	-0.3V	$V_{REF}-0.1V$	$V_{REF}+0.1V$	3.6V	NA	NA	NA	NA							

**Note!**

[1] The total DC current limit(sourced and sunk current) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than  $n \cdot 8\text{mA}$ , where  $n$  represents the number of IOs bonded out from a bank.

### 3.3.5 Differential I/O DC Characteristics

Table 3-12 Differential I/O DC Characteristics  
LVDS

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
$V_{INA}, V_{INB}$	Input Voltage	-	0	-	2.4	V
$V_{CM}$	Input Common Mode Voltage	-	0.05	-	2.35	V
$V_{THD}$	Differential Input Threshold	Minimum Input Swing	$\pm 100$	-	$\pm 600$	mV
$I_{IN}$	Input Current	Power On or Power Off	-	-	$\pm 10$	$\mu\text{A}$
$V_{OH}$	Output High Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	-	-	1.6	V
$V_{OL}$	Output Low Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	0.9	-	-	V
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100\Omega$	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Between High and Low	-	-	-	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100\Omega$	1.125	1.2	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ Between High and Low	-	-	-	50	mV
$I_S$	Short-circuit current	$V_{OD} = 0\text{V}$ outputs short-circuited	-	-	15	mA

## 3.4 Switching Characteristics

### 3.4.1 CFU Switching Characteristics

Table 3-13 CFU Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
$t_{LUT4\_CFU}$	LUT4 delay	-	0.337	ns
$t_{LUT5\_CFU}$	LUT5 delay	-	0.694	ns
$t_{LUT6\_CFU}$	LUT6 delay	-	1.005	ns
$t_{LUT7\_CFU}$	LUT7 delay	-	1.316	ns
$t_{LUT8\_CFU}$	LUT8 delay	-	1.627	ns
$t_{SR\_CFU}$	Set/Reset to Register output	-	0.93	ns
$t_{CO\_CFU}$	Clock to Register output	-	0.38	ns

### 3.4.2 BSRAM Switching Characteristics

Table 3-14 BSRAM Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
$t_{COAD\_BSRAM}$	Clock to output from read address/data	-	2.55	ns
$t_{COOR\_BSRAM}$	Clock to output from output register	-	0.28	ns

### 3.4.3 DSP Switching Characteristics

Table 3-15 DSP Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
$t_{COIR\_DSP}$	Clock to output from input register	-	2.40	ns
$t_{COPR\_DSP}$	Clock to output from pipeline register	-	1.20	ns
$t_{COOR\_DSP}$	Clock to output from output register	-	0.42	ns

### 3.4.4 Gearbox Switching Characteristics

Table 3-16 Gearbox Timing Parameters  
TBD

### 3.4.5 Clock and I/O Switching Characteristics

Table 3-17 External Switching Characteristics

Name	Description	Device	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
Pin-LUT-Pin Delay <sup>(1)</sup>	Pin(IOxA) to Pin(IOxB) delay	GW2A(2AR)-18	-	3.83	-	4.59	ns
T <sub>HCLKdly</sub>	HCLK tree delay	GW2A(2AR)-18	-	0.82	-	0.98	ns
T <sub>GCLKdly</sub>	GCLK tree delay	GW2A(2AR)-18	-	1.77	-	2.12	ns

**Note!**

Test condition: V<sub>CCIO</sub>= 3.3V, V<sub>CCX</sub>=3.3V.

### 3.4.6 On-chip Oscillator Switching Characteristics

Table 3-18 On-chip Oscillator Parameters

Name	Description	Min.	Typ.	Max.
f <sub>MAX</sub>	Output Frequency (0 to +85°C)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100°C)	100MHz	125MHz	150MHz
t <sub>DT</sub>	Output Clock Duty Cycle	43%	50%	57%
t <sub>OPJIT</sub>	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

### 3.4.7 PLL Switching Characteristics

Table 3-19 PLL Parameters

Device	Speed Grade	Name	Min.	Max.
GW2AR-18	C8/I7 A6	CLKIN	3MHz	500MHz
		PFD	3MHz	500MHz
		VCO	500MHz	1250MHz
		CLKOUT	3.90625 MHz	625 MHz
	C7/I6	CLKIN	3MHz	400MHz
		PFD	3MHz	400MHz
		VCO	400MHz	1000MHz
		CLKOUT	3.125MHz	500MHz

## 3.5 Configuration Interface Timing Specification

The GW2AR series of FPGA products support multiple GowinCONFIG modes: MSPI, SSPI, SERIAL, CPU. For more information, please refer to [UG290, Gowin FPGA Products Programming and Configuration User Guide](#).

# 4 Ordering Information

## 4.1 Part Naming

### Note!

- For more information about the packages, please refer to [1.2 Product Resources](#).
- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in Gowin’s part name marking for one device. GOWIN devices are screened using industrial standards, so the same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100°C, and the maximum temperature of the commercial grade is 85°C. Therefore, if the chip meets speed grade 8 in commercial grade applications, its speed grade will be 7 in industrial grade applications.

Figure 4-1 Part Naming Examples - ES

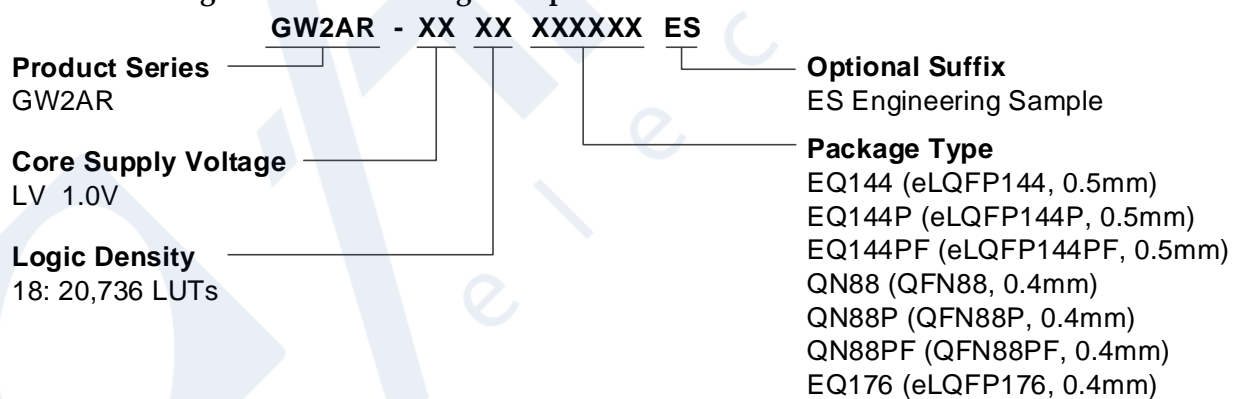
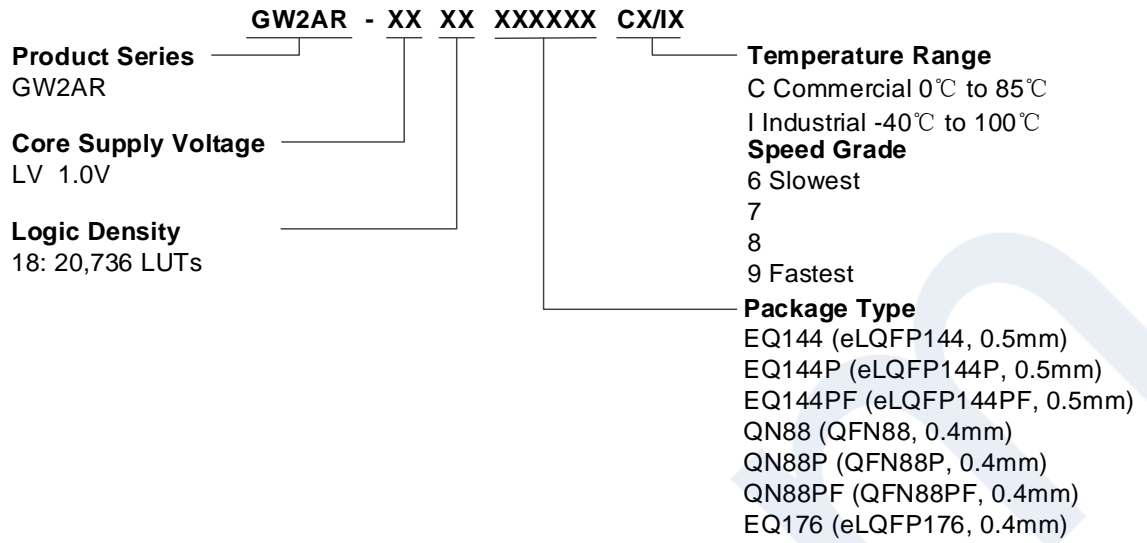


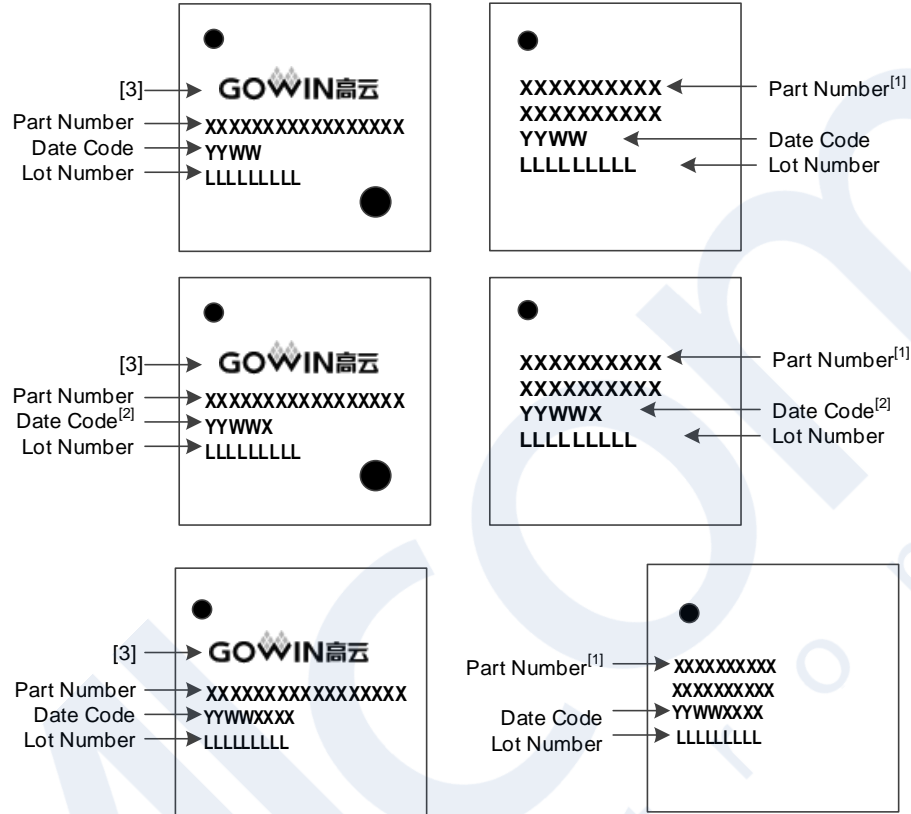
Figure 4-2 Part Naming Examples - Production



## 4.2 Package Markings

Gowin's devices have markings on their surfaces, as shown in Figure 4-3.

Figure 4-3 Package Marking Examples



### Note!

- [1] The first two lines in the right figure(s) above are both the "Part Number".
- [2] The Date Code followed by an "X" is for X version devices.
- [3] Whether the package marking bears the Gowin Logo or not depends on the package type, package size, and Part Number length. The above figure are only examples of the package markings.



# 5 About This Guide

## 5.1 Purpose

This data sheet describes the features, resources, architecture, AC/DC characteristics, and ordering information of the GW2AR series of FPGA products, making it easier to understand and use Gowin's devices.

## 5.2 Related Documents

The latest documents are available at [www.gowinsemi.com](http://www.gowinsemi.com).

- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [UG290, Gowin FPGA Products Programming and Configuration User Guide](#)
- [UG229, GW2AR series of FPGA Products Package and Pinout Manual](#)
- [UG115, GW2AR-18 Pinout](#)

## 5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 5-1.

**Table 5-1 Terminology and Abbreviations**

Terminology and Abbreviations	Full Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
CS	WLCSP(Wafer-Level Chip Scale Package)
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable
DSP	Digital Signal Processing
EQ	ELQFP(E-pad Low-profile Quad Flat Package)
FPGA	Field Programmable Gate Array
GPIO	Gowin Programable IO
IOB	Input/Output Block
LQ	LQFP(Low-profile Quad Flat Package)
LUT4	4-input Look-up Table
LUT5	5-input Look-up Table
LUT6	6-input Look-up Table
LUT7	7-input Look-up Table
LUT8	8-input Look-up Table
MG	MBGA(Micro Ball Grid Array Package)
PG	PBGA(Plastic Ball Grid Array Package)
PLL	Phase-locked Loop
QN	QFN(Quad Flat No-lead)
REG	Register
SDP	Semi Dual Port 16K BSRAM
SDRAM	Synchronous Dynamic RAM
SIP	System in Package
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing
UG	UBGA(Ultra Ball Grid Array Package)

## 5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)



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