Preliminary

GW5AST series of FPGA Product

Data Sheet

DS1104-1.0E, 6/29/2023

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Revision History

Date	Version	Description
6/29/2023	1.0E	Preliminary version published.

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1 General Description

GOWINSEMI GW5AST series of FPGA Products are the 5th-generation of Arora family, with abundant internal resources, a new-architecture and high-performance DSP supporting AI operations, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, it integrates self-developed DDR3, 12.5Gbps SERDES supporting multiple protocols, RiscV AE350_SOC, and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility designs.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

1.1 Features

- Lower power consumption
  - 22nm SRAM process
  - Core Power (LV version): 0.9V / 1.0V
  - Supports dynamic on/off of clock
- Abundant basic logic cells
  - GW5AST-138 provides up to 138K LUT4s
  - Supports shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port, Single Port, and Semi Dual Port
  - Supports bytes write enable
  - Supports ECC detection and error correction
- Supports multiple transmission protocols such as 270 Mbps to 12.5G bps custom SERDES protocols and 10G Ethernet, etc.
- Supports PCIe 2.0 hard core
  - Supports x1, x2, x4, x8 lanes
  - Supports Root Complex and End Point

- Supports MIPI D-PHY RX hard core
  - Supports MIPI DSI and MIPI CSI-2 RX
  - Up to 2.5 Gbps per MIPI lane
  - Supports up to eight data lanes and two clock lanes, with the max. transmission speed up to 20Gbps
- GPIO supports MIPI D-PHY RX
  - GPIO can be configured as MIPI DSI and MIPI CSI-2 RX interfaces
  - Up to 1.5 Gbps per MIPI lane
- High performance DSP blocks with a new architecture
  - High performance digital signal processing
  - Supports 27 x 18, 12 x 12, 27 x 36 multiplier and 48-bit accumulator
  - Supports cascading of multipliers
  - Supports pipeline mode and bypass mode
  - Pre-addtion operation for filter function
  - Supports barrel shifter
- RiscV AE350_SOC
- A new and flexible X-channel oversampling ADC with high accuracy, no external voltage source required
  - 60dB SNR
  - 1kHz Signal Bandwidth
- Supports various SDRAM interfaces, up to DDR3 1333 Mb/s
- Multiple I/O standards
  - Hysteresis option for input signals
  - Supports drive strengths of 4mA, 8mA,12mA, 16mA, 24mA, etc.

    Note!

    [1] 24mA is only supported by GW5AST-138.
  - Individual Bus Keeper, Pull-up, Pull-down, and Open Drain options
  - Hot Socket
- 16 global clocks, 6/12 high-performance PLLs, 16/24 high speed clocks
- Configuration and Programming
  - JTAG configuration
  - Four GowinConfig configuration modes: SSPI, MSPI, CPU, SERIAL
  - Supports programming the SPI Flash directly in JTAG and SSPI

modes; For other modes, you can program the SPI Flash using IP
- Supports background upgrade
- Supports bitstream file encryption and security bit settings
- Support configuration memory soft error recovery (CMSER)
- Supports OTP. Offers a unique 64-bit DNA identifier for each device

1.2 Product Resources

Table 1-1 Product Resources

Device	GW5AST-138
LUT4	138240
Flip-Flop (REG)	138240
Distributed Static Random Access Memory SSRAM(Kb)	1080
Block Static Random Access Memory BSRAM(Kb)	6120
Number of BSRAMs Number of BSRAM	340
DSP（27-bit x 18-bit）	298
Maximum phase locked loop[1](PLLs)	12
Global Clocks	16
High-speed Clocks	24
Transceivers	8
Transceivers Rate	270Mbps - 12.5Gbps
PCIe 2.0	1, x1, x2, x4, x8 PCIe 2.0
LVDS Gbps	1.25
DDR3 Mbps	1333
MIPI DPHY hard core	2.5Gbps (RX) 8 data lanes 2 clock lanes
Hard-core Processor	RiscV AE350_SOC
ADC	2
Number of GPIO banks	6
Maximum number of I/Os	376
Core voltage	0.9V/1.0V

Note!

[1] Different packages support different numbers of PLLs.

Table 1-2 Package Information and Maximum Number of User I/Os

Package	Pitch (mm)	Size (mm)	GW5AST-138
FPG676A (FC)	1.0	27 x 27	312 (150)

Package	Pitch (mm)	Size (mm)	GW5AST-138
PG484A	1.0	23 x 23	297 (143)
PG676A	1.0	27 x 27	312（150）

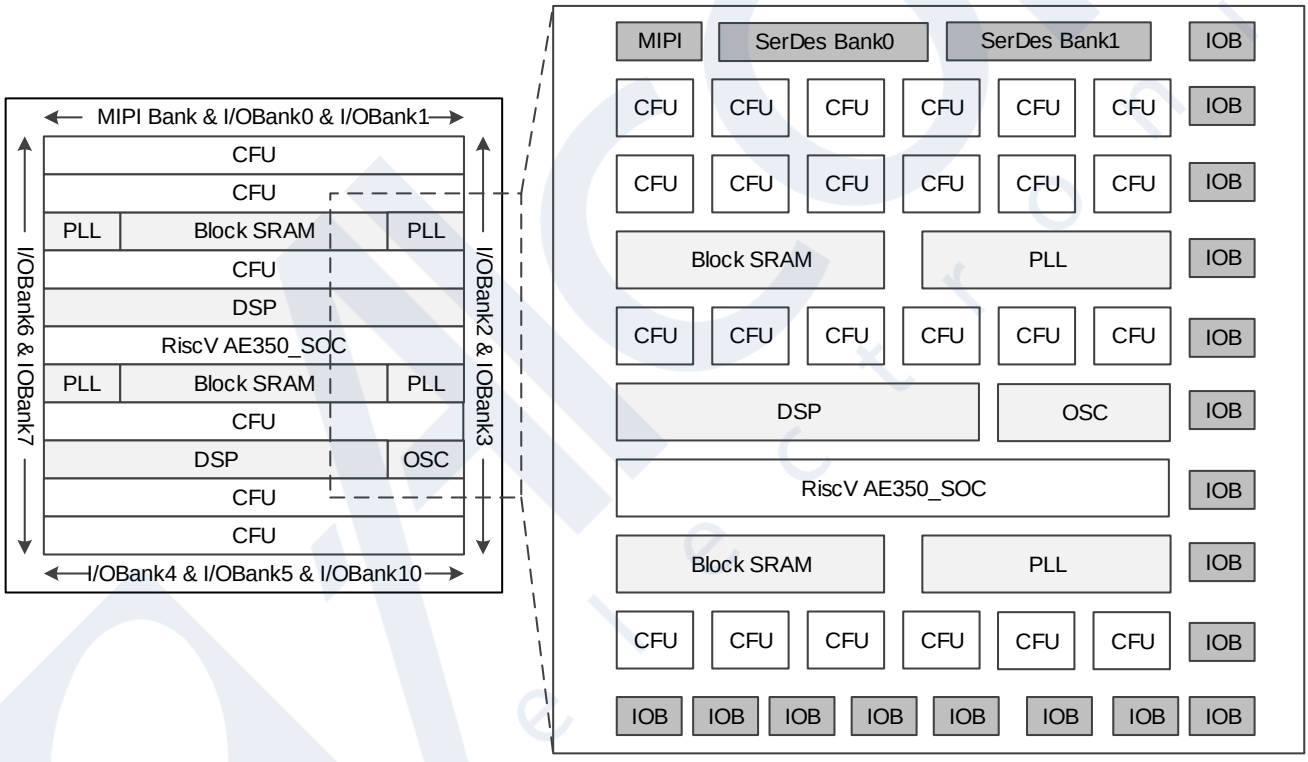
Note!

[1] The package types in this data sheet are written with abbreviations. See 4.1Part Name for further information.

2 Architecture

2.1 Architecture Overview

Figure 2-1 Architecture Diagram



Take GW5AST-138 as an example, see Figure 2-1 for an overview of the architecture of the GW5AST series of FPGA Products. Please refer to Table 1-1 for device internal resources. The core of the device is an array of Configurable Logic Units (CFU) surrounded by IO blocks. Besides, BSRAMs, DSP blocks, Gigabit Transceiver, MIPI D-PHY, ADC, PLLs, and on chip oscillators are provided.

Configurable Function Unit (CFU) is the base cell for the array of the GW5AST series of FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see

2.2 Configurable Function Units.

The I/O resources in the GW5AST series of FPGA Products are arranged around the periphery of the devices in groups referred to as banks. I/O resources support multiple I/O standards, and support regular mode, SRD mode, generic DDR mode, and DDR_MEM mode. For more detailed information, see 2.3 Input/Output Blocks.

The BSRAM is embedded as a row in GW5AST series of FPGA Products. Each BSRAM has a maximum capacity of 36Kbits and consists of two 18Kbits BSRAMs. It supports multiple configuration modes and operation modes. For more detailed information, see 2.4 Block SRAM (BSRAM).

GW5AST series of FPGA Products are embedded with a brand-new DSP, which can meet the high-performance digital signal processing requirements. For details, refer to 2.5 DSP Blocks..

GW5AST series of FPGA Products include Gigabit Transceiver Quads, each of which supports up to 4 transceivers. For details, refer to 2.6Gigabit Transceiver.

GW5AST series of FPGA Products provide a MIPI D-PHY hardcore supporting the “MIPI Alliance Standard for D-PHY Specification(V1.2)”. For details, see 2.8 MIPI D-PHY.

GW5AST series of FPGA Products provide a hardcore processor RiscV AE350_SOC. For details, see 2.9 RiscV AE350_SOC

GW5AST series of FPGA Products integrate a new and flexible oversampling ADC. For details, see 2.10 ADC.

GW5AST series of FPGA Products have embedded PLL resources. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. This series of FPGAs also have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 1.67 MHz to 105MHz, providing clocking resources for the MSPI mode. The on-chip clock oscillator also provides programmable user clocks. For more information, see 2.14 On Chip Oscillator.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW5AST series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more details, see 2.12 Global Set/Reset (GSR), and 2.13 Programming & Configuration.

2.2 Configurable Function Units

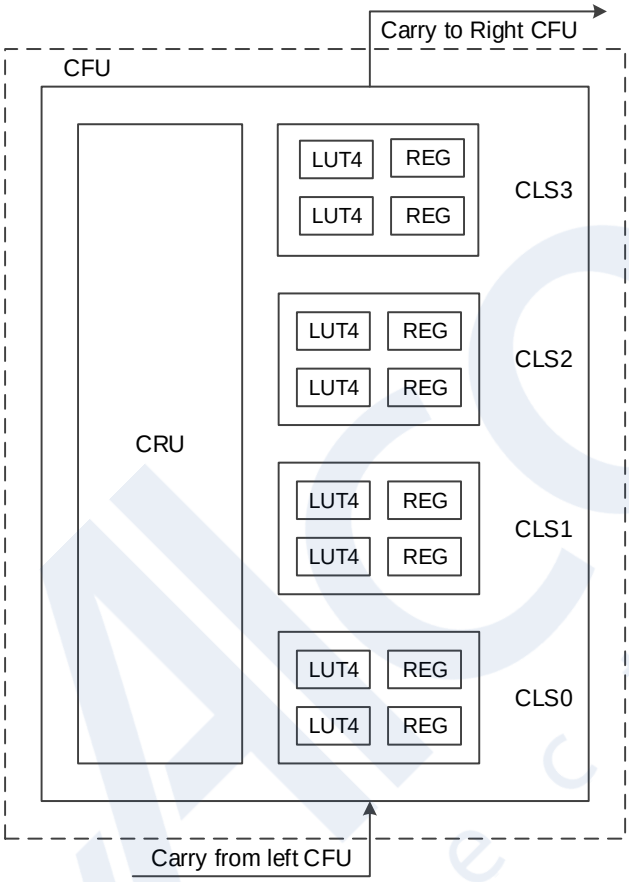
Configurable Function Units (CFUs) are the basic cells for the array of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs). Each CLS includes two 4 input look-

up-tables (LUTs) and two registers (REGs), as shown in Figure 2-2 .

CLSs in the CFUs can be configured as basic look-up tables, arithmetic logic units, static random access memories, and read only memories according to application scenarios.

For more details, please see *UG303, Arora V Configurable Function Unit (CFU) User Guide*.

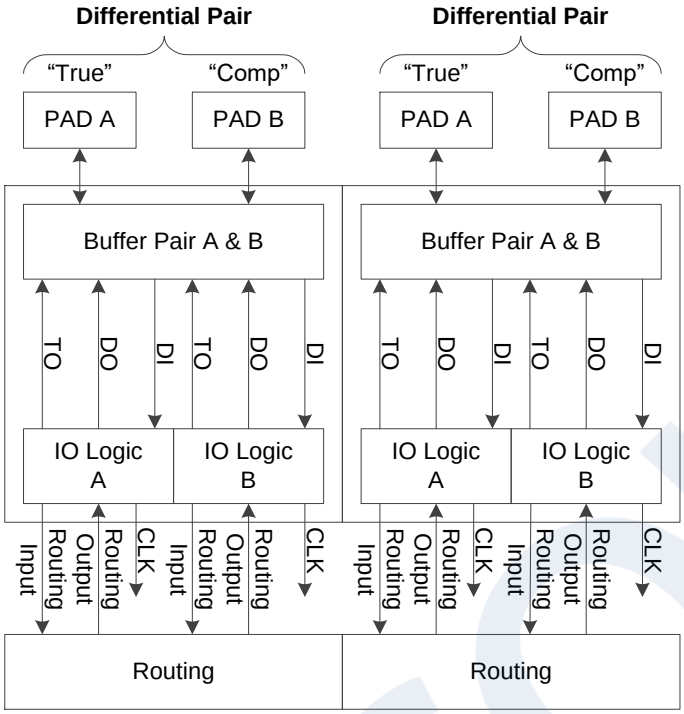
Figure 2-2 CFU Structure View



2.3 Input/Output Blocks

The IOB in the GW5AST series of FPGA Products includes IO buffer, IO logic, and its routing unit. As shown in Figure 2-3 , each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as a single end input/output.

Figure 2-3 IOB Structure View



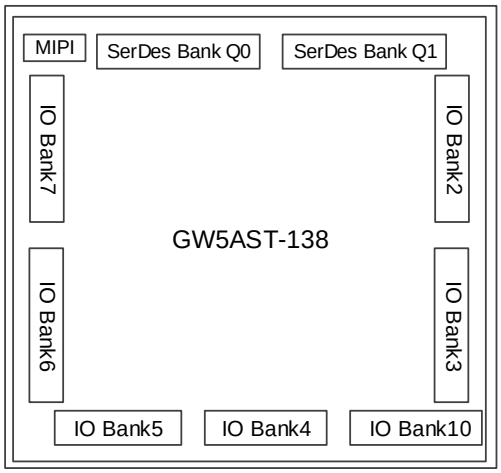
IOB Features:

- V_{CCIO} supplied with each bank
- All banks support True differential input
- Supports multiple levels: LVCMOS, PCI, LVTTL, SSTL, HSTL, LVDS, Mini_LVDS, RSDS, PPDS, BLVDS
- Input hysteresis option
- Output drive strength option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports SDR mode, DDR mode, etc.

2.3.1 I/O Buffer

GW5AST-138 has six GPIO Banks (Bank2~7), two SerDes Banks and a Bank for configuration (Bank 10), as shown in Figure 2-4Figure . Bank 10 can also be used as an I/O Bank.

Figure 2-4 Bank Distribution View of GW5AST-138



Each Bank has its independent I/O power supply V_{CCIO}. V_{CCIO} can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, 1.2V, or 1V.

Note!

GW5AST-138: To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as the reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.675V, 0.75V, 0.9V, and (33%,42%,50%,58%)Vcco) or the external reference voltage using any IO from the bank.

The auxiliary voltage V_{CCX} of GW5AST-138 devices supports 1.8V.

Different banks in the GW5AST series of FPGA Products support different on-chip resistor settings, including single-ended resistor and differential resistor. Single-ended resistor is set for SSTL/HSTL I/O. Differential resistor is set for LVDS/PPDS/ RSDS input. For more details, refer to *UG304, Arora V Programmable IO (GPIO) User Guide* .

Note!

Before and during configuration, all GPIOs of the device have weak pull-up by default. The default I/O state is None after configuration is complete and it can be configured via the Gowin software. The status of configuration-related I/Os differs depending on the configuration mode.

For the different I/O standards and configuration options, please refer to Table 2-1 and Table 2-2.

Table 2-1 Output I/O Standards and Configuration Options (GW5AST-138)

I/O output standard	Single-ended/ Differential	Bank V_{CCIO} (V)	Drive Strength (mA)	Typical Applications
LVDS25	Differential(TLVDS)	2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
BLVDS25		2.5/3.3	3.5/2.5/4.5/6	Multi-point high-speed data transmission
RSDS		2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
MINILVDS		2.5/3.3	3.5/2.5/4.5/6	LCD timing driver interface and column driver interface
PPLVDS		2.5/3.3	3.5/2.5/4.5/6	LCD row/column driver
LVDS25E	Differential	2.5	8/4/12/16/24	High-speed point-to-point data transmission
BLVDS25E		2.5	8/4/12/16/24	Multi-point high-speed data transmission
MLVDS25E		2.5	8/4/12/16/24	LCD timing driver interface and column driver interface
RSDS25E		2.5	8/4/12/16/24	High-speed point-to-point data transmission
LVPECL33E		3.3	8/4/12/16/24	Universal interface
HSUL12D		1.2	8，4，12	LPDDR2
HSUL12D_I		1.2	8，4，12	LPDDR2
HSTL15D_I		1.5	8/4/12/16	Memory interface
HSTL15D_II[4]		1.5	8/4/12/16	Memory interface
HSTL18D_I		1.8	8/4/12/16	Memory interface
HSTL18D_II		1.8	8/4/12/16	Memory interface
SSTL135D		1.35	8/4/12	Memory interface
SSTL15D		1.5	8/4/12/16	Memory interface
SSTL18D_I		1.8	8/4/12/16/24	Memory interface
SSTL18D_II		1.8	8/4/12/16/24	Memory interface
LPDDRD		1.8	8/4/12/16/24	LPDDR and Mobile DDR
LVCMOS10D		1.0E	4	Universal interface
LVCMOS12D		1.2	4/8	Universal interface
LVCMOS15D		1.5	4/8/12	Universal interface

I/O output standard	Single-ended/ Differential	Bank V_{CCIO} (V)	Drive Strength (mA)	Typical Applications
LVCMOS18D		1.8	4/8/12/16/24	Universal interface
LVCMOS25D		2.5	4/8/12/16/24	Universal interface
LVCMOS33D		3.3	8/4/12/16/24	Universal interface
HSUL12	Single-ended	1.2	8/4/12	Memory interface
HSTL12_I		1.2	8/4/12	Memory interface
HSTL15_I		1.5	8/4/1216	Memory interface
HSTL15_ II		1.5	8/4/12/16	Memory interface
HSTL18_I		1.8	8/4/12/16/24	Memory interface
HSTL18_II		1.8	8/4/12/16/24	Memory interface
SSTL135		1.35	8/4/12	Memory interface
SSTL15		1.5	8/4/12/16	Memory interface
SSTL18_I		1.8	8/4/12/16/24	Memory interface
SSTL18_II		1.8	8/4/12/16/24	Memory interface
LVCMOS10		1.0E		Universal interface
LVCMOS12		1.2	4/8	Universal interface
LVCMOS15		1.5	4/8/12	Universal interface
LVCMOS18		1.8	4/8/12/16/24	Universal interface
LVCMOS25		2.5	4/8/12/16/24	Universal interface
LVCMOS33/LVTTL33		3.3	8/4/12/16/24	Universal interface
LPDDR		1.8	8/4/12/16/24	LPDDR and Mobile DDR
PCI33		3.3	8/4/12/16/24	PC and embedded system

Table 2-2 Input I/O Standards and Configuration Options (GW5AST-138)

I/O Input Standard	Single-ended/ Differential	Bank V_{CCIO} (V)	Hysteresis	Need V_{REF}
MIPI	Differential	1.2	No	No
ADC_in		2.5/1.0/1.2/1.5/1.8/3.3	No	No
LVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
BLVDS25		2.5/1.0/1.2/1.5/1.8/3.3	No	No
RSDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
MINILVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
PPLVDS		2.5/1.0/1.2/1.5/1.8/3.3	No	No
HSUL12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL12D_I		1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL15D_I		1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL15D_II		1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No

I/O Input Standard	Single-ended/ Differential	Bank V_{CCIO} (V)	Hysteresis	Need V_{REF}
HSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL135D		1.35/1.0/1.2/1.5/1.8/2.5/3.3	No	No
SSTL15D		1.5/1.0/1.2/1.8/2.5/3.3	No	No
SSTL18D_I		1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL18D_II		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LPDDRD		1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVCMOS10D		1.0/1.2/1.5/1.8/2.5/3.3	No	No
LVCMOS12D		1.2/1.0/1.5/1.8/2.5/3.3	No	No
LVCMOS15D		1.5/1.0/1.2/1.8/2.5/3.3	No	No
LVCMOS18D		1.8/1.0/1.2/1.5/2.5/3.3	No	No
HSUL12	Single-ended	1.2	Yes	No
HSTL12_I		1.2	Yes	No
HSTL15_I		1.5	Yes	No
HSTL15_II		1.5	Yes	No
HSTL18_I		1.8	Yes	No
HSTL18_II		1.8	Yes	No
SSTL135		1.35	Yes	No
SSTL15		1.5	Yes	No
SSTL18_I		1.8	Yes	No
SSTL18_II		1.8	Yes	No
LVCMOS10		1.0E	Yes	No
LVCMOS10UD12		1.2	Yes	No
LVCMOS10UD15		1.5	Yes	No
LVCMOS10UD18		1.8	Yes	No
LVCMOS10UD25		2.5	Yes	No
LVCMOS10UD33		3.3	Yes	No
LVCMOS12		1.2	Yes	No
LVCMOS15		1.5	Yes	No
LVCMOS15OD10		1.0E	Yes	No
LVCMOS15OD12		1.2	Yes	No
LVCMOS15UD18		1.8	Yes	No
LVCMOS15UD25		2.5	Yes	No
LVCMOS15UD33		3.3	Yes	No
LVCMOS18		1.8	Yes	No
LVCMOS18OD10		1.0E	Yes	No
LVCMOS18OD12		1.2	Yes	No
LVCMOS18OD15		1.5	Yes	No
LVCMOS18UD25		2.5	Yes	No

I/O Input Standard	Single-ended/ Differential	Bank V_{CCIO} (V)	Hysteresis	Need V_{REF}
LVCMOS18UD33		3.3	Yes	No
LVCMOS25		2.5	Yes	No
LVCMOS25UD33		3.3	Yes	No
LVCMOS33/LVTTL33		3.3	Yes	No
LVCMOS33OD25		2.5	Yes	No
LPDDR		1.8	Yes	No
PCI33		3.3	Yes	No
VREF1_DRIVER		1.8/1.2/1.35/1.5	No	Yes

2.3.2 I/O Logic

Figure 2-5 shows the I/O logic output of GW5AST series of FPGA Products.

Figure 2-5 I/O Logic Output

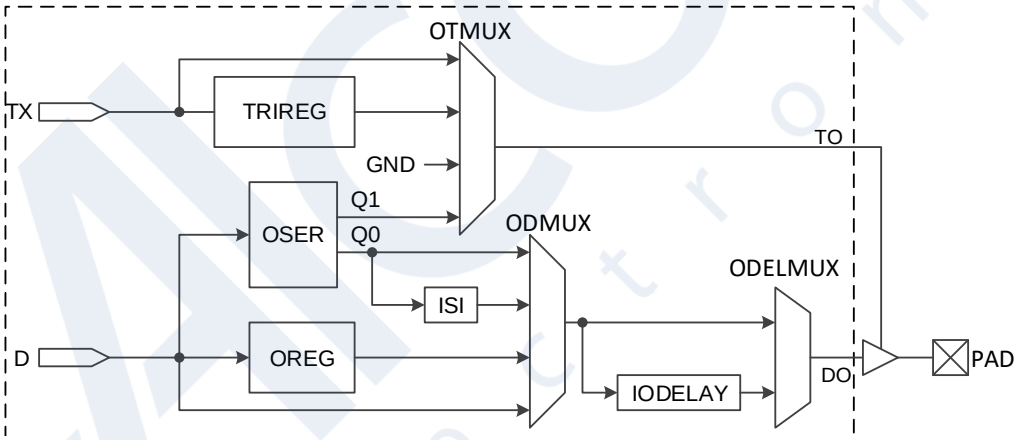
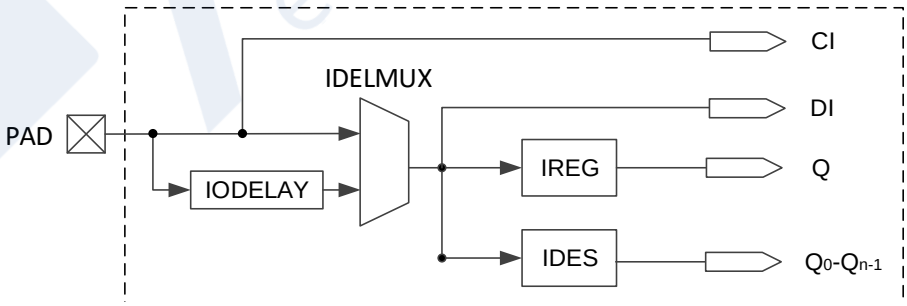


Figure 2-6 shows the I/O logic input of the GW5AST series of FPGA Products.

Figure 2-6 I/O Logic Input

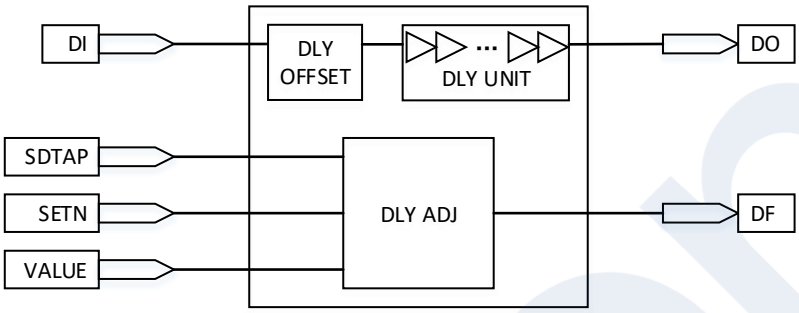


Descriptions of the I/O logic modules of GW5AST series of FPGA Products are presented below.

Delay Modules

See Figure 2-7 for an overview of the IODELAY. Each I/O of GW5AST includes IODELAY, providing a total of 256 (0~255) delays, with a single-step delay time of about 15.5ps. The total IODELAY time is DLYOFFSET+DLY UNIT*SDTAP.

Figure 2-7 IODELAY



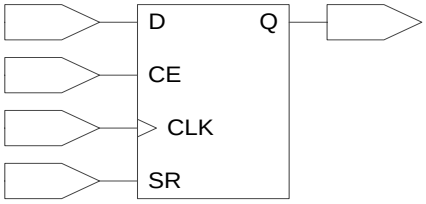
There are three ways to control the delay:

- Static control.
- Dynamic control, which can be combined with logic function circuits to achieve dynamic delay adjustment.
- Adaptive control.

I/O Register

See Figure Figure 2-8 for the I/O register in GW5AST series of FPGA Products. Each I/O of the GW5AST series of FPGA Products provides one input register (IREG), one output register (OREG), and one tristate Register (TREG).

Figure 2-8 Diagram of I/O registers



Note!

- CE can be either active ow (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The registers can be programmed as registers(DFFs) or latches.

De-serializer DES and Serializer SER

The GW5AST series of FPGA Products support serialization and deserialization of various ratios, as shown in the following table:

Table 2-3 DES /SER Ratios Supported by the GW5AST series of FPGA Products

	Ratios Supported
Input logic	1:2 / 1:4 / 1:7 / 1:8 / 1:10 / 1:14 / 1:16 / 1:32
Output logic	2:1 / 4:1/ 7:1 / 8:1 / 10:1 / 16:1

2.3.3 I/O Logic Modes

The I/O Logic in GW5AST series of FPGA Products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

For further details about the I/O logic modes, refer to *UG304, Arora V Programmable IO (GPIO) User Guide* .

2.4 Block SRAM (BSRAM)

2.4.1 Introduction

GW5AST series of FPGA Products provide abundant block SRAM resources. These memory resources are distributed throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). Up to 36Kbits can be configured for each BSRAM. There are five operation modes: Single Port mode, Dual Port mode, Semi Dual Port mode, Semi Dual Port mode with ECC function, and ROM mode.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM’s features:

- Up to 18Kbits per BSRAM
- Clock frequency up to 380MHz
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi Dual Port Mode
- Supports ECC detection and error correction Function
- Supports ROM Mode
- Data width up to 72bits
- Dual Port and Semi-Dual Port support independent clocks and independent data width
- Read mode supports Register Output and Bypass Output
- Write mode supports Normal mode and write-through mode

2.4.2 Configuration Mode

BSRAMs in the GW5AST series of FPGA Products support various data widths. See Table 2-4.

Table 2-4 Memory Size Configuration

Capacity	Single Port Mode	Dual Port Mode	Semi Dual Port Mode	Semi Dual Port Mode with ECC Function	Read Only Mode
16Kbits	16K x 1	16K x 1	16K x 1	–	16K x 1
	8K x 2	8K x 2	8K x 2	–	8K x 2
	4K x 4	4K x 4	4K x 4	–	4K x 4
	2K x 8	2K x 8	2K x 8	–	2K x 8
	1K x 16	1K x 16	1K x 16	–	1K x 16
	512 x 32	–	512 x 32	–	512 x 32
18Kbits	2K x 9	2K x 9	2K x 9	–	2K x 9
	1K x 18	1K x 18	1K x 18	–	1K x 18
	512 x 36	–	512 x 36	–	512 x 36
36Kbits	–	–	–	512 x 72	–

Single Port Mode

In the single port mode, BSRAM can write to or read from one port at one clock edge. It supports 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode). In Normal-Write Mode, the written data will be stored in the internal memory array. In Write–through Mode, the written data will not only be stored in the internal memory array, but also be written to the output of BSRAM. When the output register is bypassed, the new data will show at the same write clock rising edge.

For more information on single port mode, please refer to *UG300, Arora V BSRAM & SSRAM User Guide*.

Dual Port Mode

BSRAM supports Dual Port mode. It supports 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode). The applicable operations are as follows:

- Two independent read, reading data from any given address.
- Two independent write, writing data to any address that is different.
- An independent read and an independent write at different clock frequencies.

Note!

- In Dual-port mode, Port A and Port B can read from or write to the same address. Null or repeated reads do not damage the storage module.
- In Dual-port mode, when Port A and Port B write to the same address at the same time, the dual ports writing fail at the same time.
- When Port A reads, Port B writes, and they access the same address, the write port succeeds, but the read port fails, and the output data is unknown. BSRAM contents are the values from the write port.

Dual Port supports independent read/write clocks and independent read/write data width. For more information on dual port mode, please refer to *UG300, Arora V BSRAM & SSRAM User Guide*.

Semi Dual Port Mode

Semi-dual ports support independent read/write operations in the form of A port write-only ("Normal mode") and B port read-only. When Port A reads, Port B writes, and they access the same address, the write port succeeds, but the read port fails, and the output data is unknown. BSRAM contents are the values from the write port.

Semi-dual Port supports independent read/write clocks and independent read/write data width. For more information on semi dual port mode, please refer to *UG300, Arora V BSRAM & SSRAM User Guide*.

Semi Dual Port Mode with ECC Function

Semi-dual ports with ECC Function support independent read/write operations in the form of A port write-only and B port read-only. Independent read/write data width is also supported. This mode provides ECC function. For more information on this mode, please refer to *UG300, Arora V BSRAM & SSRAM User Guide*.

Read Only Mode

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For more information on read only mode, please refer to *UG300, Arora V BSRAM & SSRAM User Guide*.

2.4.3 Data Width Configuration

BSRAMs in the GW5AST series of FPGA Products support independent data width for read/write operations. In Dual Port mode, Semi Dual Port mode, and Semi Dual Port mode with ECC function, the data width for read/write operations can be different. For the data width supported by Port A and Port B, see Table 2-5, Table 2-6, and Table 2-7.

Table 2-5 Read/Write Data Width Configuration in Dual Port Mode

Capacity	Port B	Port A						
		16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16Kbits	16K x 1	Yes	Yes	Yes	Yes	Yes	N/A	N/A
	8K x 2	Yes	Yes	Yes	Yes	Yes	N/A	N/A
	4K x 4	Yes	Yes	Yes	Yes	Yes	N/A	N/A
	2K x 8	Yes	Yes	Yes	Yes	Yes	N/A	N/A
	1K x 16	Yes	Yes	Yes	Yes	Yes	N/A	N/A
18Kbits	2K x 9	N/A	N/A	N/A	N/A	N/A	Yes	Yes
	1K x 18	N/A	N/A	N/A	N/A	N/A	Yes	Yes

Table 2-6 Read/Write Data Width Configuration in Semi Dual Port Mode

Capacity	Port B	Port A										
		16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x 32	2K x 9	1K x 18	512 x 36	1K x 36	512 x 72
16Kbits	16K x 1	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A
	8K x 2	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A
	4K x 4	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A
	2K x 8	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A
	1K x 16	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A
	512 x 32	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A
18Kbits	2K x 9	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes	Yes	N/A	N/A
	1K x 18	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes	Yes	N/A	N/A

Table 2-7 Read/Write Data Width Configuration in Semi Dual Port Mode with ECC Function

Capacity	Port B	Port A	
			512 x 72
36Kbits	512 x 72	N/A	*

2.4.4 ECC

The BSRAM of GW5AST-138 has a built-in ECC hardcore module,

which is mainly used for data detection and correction during data transfer and storage. ECC features are as follows:

- ECC error detection and correction only supported in SDP 512 x 64 mode
- Supports 1-bit error correction and 2-bit error alarm in 64-bit SRAM data
- 72-bit ECC module contains 64-bit data bits and 8-bit parity bits;
- Bit 31 and bit 63 support 1-bit and 2-bit error injection

2.4.5 Byte-enable

BSRAMs in the GW5AST series of FPGA Products support the byte-enable function. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The byte enable function is for write only and is available at bit widths of 16/18 and 32/36. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte parameter options can be used to control the BSRAM write operation.

2.4.6 Synchronous Operation

- All the input registers of BSRAM support synchronous write.
- The output register can be used as a pipeline register to improve design performance.
- The output registers are bypass-able.

2.4.7 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

2.4.8 BSRAM Operation Modes

BSRAM supports four different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and two write operations (Normal Mode and Write-through Mode).

Read Mode

Read data from the BSRAM via output registers or without using the registers.

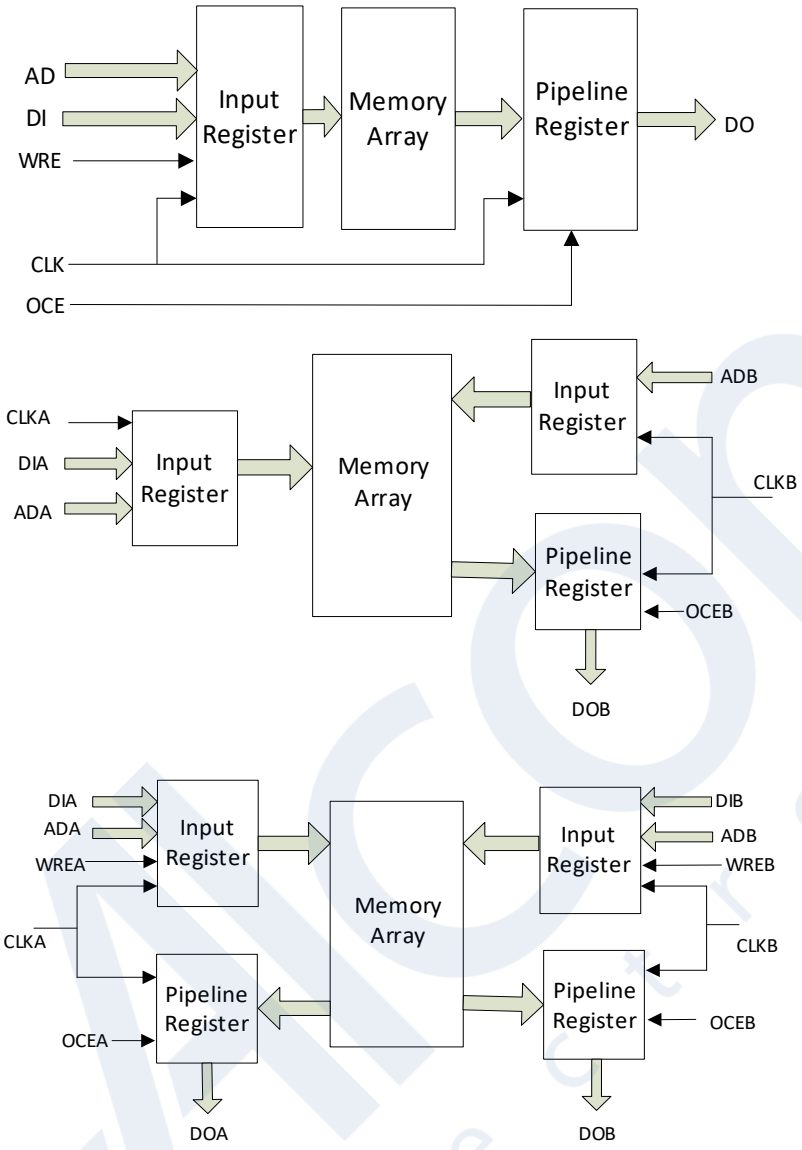
PIPELINE MODE

When reading data, the data is synchronously read out via the output register according to the clock beat. This mode supports up to 72-bit data width.

BYPASS MODE

In this mode, the output register is not used. When reading data, the data is directly sent to the output port.

Figure 2-9 Pipeline Mode in Single Port, Dual Port, and Semi-Dual Port Mode



Write Mode

NORMAL MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

2.4.9 Clock Operations

Table 2-8 lists the clock operations in different BSRAM modes:

Table 2-8 Clock Operations in Different BSRAM Modes

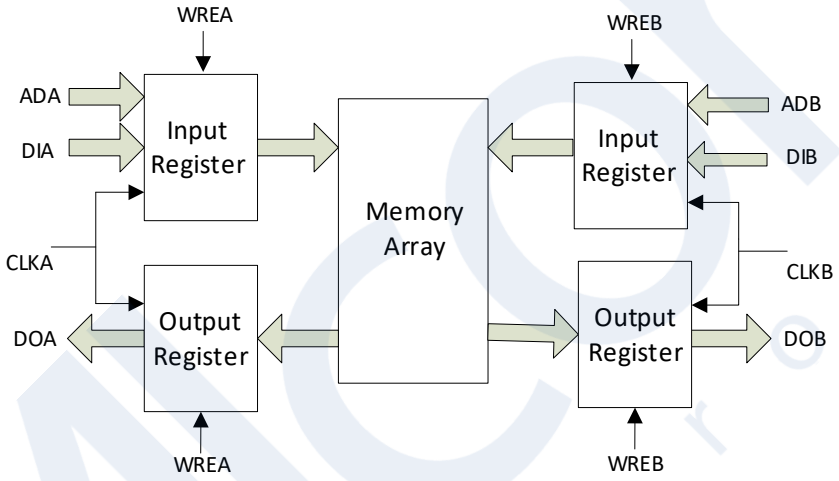
Clock Operations	BSRAM Mode

	Dual Port Mode	Semi Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 2-10 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

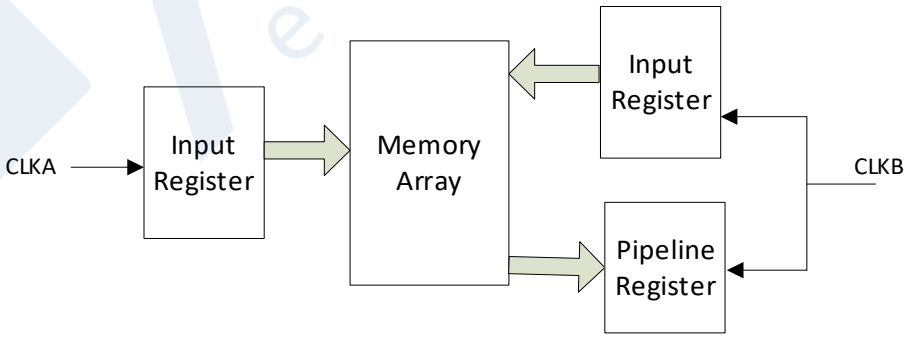
Figure 2-10 Independent Clock Mode



Read/Write Clock Operation

Figure 2-11 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

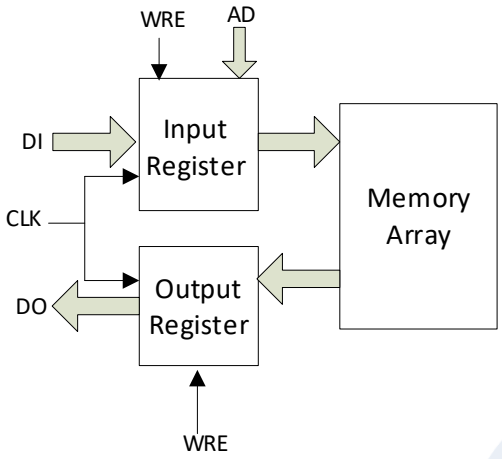
Figure 2-11 Read/Write Clock Mode



Single Port Clock Mode

Figure 2-12 shows the clock operation in single port mode.

Figure 2-12 Single Port Clock Mode



2.5 DSP Blocks

GW5AST series of FPGA Products provide brand new DSP resources. This DSP solution can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high resource utilization, and low power consumption.

The features of DSP are as follows.

- Can be configured as 12 x 12, 27 x 28, and 27 x 36 signed multipliers
- 48-bit ALU
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Supports pipeline mode and bypass mode.
- All operands for arithmetic operation are signed numbers

Each DSP consists of three main parts:

- Input multiplexer and input registers;
- One pre-adder, two multipliers, and pipeline registers;
- ALU, output multiplexers, and output registers.

2.5.1 PADD

Each DSP features one PADD(pre-adder) for implementing pre-addition, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs:

- 26-bit input C;

- Parallel 26-bit input A or SIA.

  Each input end supports pipeline mode and bypass mode.

2.5.2 MULT

Each DSP block has one 27 x 18 multiplier M0 and one 12 x 12 multiplier M1. The multipliers are located after the pre-adders to implement multiplication operations, and both the inputs and outputs support register mode and bypass mode.

Multiplier M0 can be configured as:

- One 27 x 18 multiplier
- One 12 x 12 multiplier
- Two DSPs can form a 27 x 36 multiplier

Multiplier M1 can only be configured as one 12 x 12 multiplier.

When multiplier M0 and multiplier M1 are both configured as a 12 x 12 multiplier and the ALU is enabled, 12 x 12 SUM mode can be achieved.

2.5.3 Arithmetic Logic Unit

Each DSP has one four-input 48-bit ALU, which can further enhance MULT's functions. Register mode and bypass mode are supported both in the inputs and outputs. The ALU supports the addition/subtraction operations of multiplier M0 output, multiplier M1 output (48bit operand D), ALU cascade input CASI and ALU output feedback, or static PRE_LOAD value.

2.5.4 Operating Mode

Based on control signals, DSP can be configured as different operation modes. Operation Modes:

- Multiplier
- Accumulator
- MULTADDALU

For more information on DSP Blocks, see *UG305, Arora V Digital Signal Processing (DSP) User Guide*.

2.6 Gigabit Transceivers

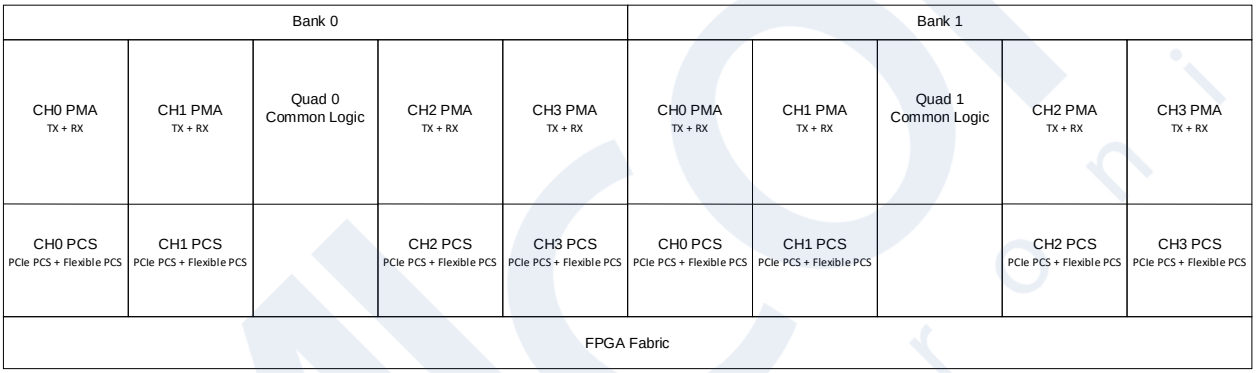
GW5AST-138 supports two Transceiver Quads. Each Quad supports up to four transceivers, and each transceiver is comprised of one TX and one RX, with the data rate raging from 270Mbps to 12.5Gbps, and supports flexible PMA and PCS.

Take GW5AST-138 as an example, Figure 2-13 shows the structure view of Transceiver Quad. The protocols supported are as follows:

- PCI Express, V2.0 (2.5 Gbps /5.0 Gbps)
- 10 Gigabit Attachment Unit Interface (XAUI) (3.125Gbps)
- RXAUI (Reduced XAUI) (6.25Gbps)

- CEI-6G-SR (6.375Gbps)
- SATA Rev3.2 (6Gbps/3Gbps/1.5Gbps) (need soft IP support)
- Serial GMII(SGMII) (1.25Gbps)
- CPRI (need soft IP support; soft IP available)
- JESD204B (need soft IP support; soft IP available)
- Rapid-IO (need soft IP support; soft IP available)
- 1000Base-X (need soft IP support; soft IP available)
- 10G-Base-R (need soft IP support; soft IP available)
- SDI-Tx/Rx (need soft IP support; soft IP available)
- SLVS-EC(Rx) (need soft IP support; soft IP available)

Figure 2-13 Gigabit Transceiver Architecture View



PMA

- Each Quad shares two PLLS (one is LC PLL, the other is ring oscillator PLL)
- Transmitter through tracking of spread reference clock.
- Lane driver with programmable transmitter equalization with 1 tap pre-cursor and 1 tap post-cursor to improve signal integrity.
- Voltage mode/current mode lane driver with board AC coupling.
- Programmable continuous time linear equalizer (CTLE) with auto-adaption.
- Receiver CDR track SSC data and tolerance +/- 5000ppm variation.
- Beacon signaling generation and detection for PCI Express.

PCS

- Dedicated hard PCIe PCS
- Flexible PCS to support PCS customization
- 8b/10b encoder/decoder
- Supports TX channel bonding
- Supports RX channel bonding and CTC

- Utilize IF FIFO to simply user system design
- Supports flexible parallel data widths of 8/10/16/20/32/40/64/80 bits

2.7 PCI Express (PCIe) Controller

GW5AST include one integrated block for PCI Express technology. It allows custom FPGA-to-FPGA communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fiber Channel HBAs (Host Bus Adapter), to the FPGA.

Features of the PCIe integrated block are as follows:

- Dedicated hard core IP, Compliant to the PCI Express Base Specification 2.0
- Supports x1, x2, x4, x8 lanes
- Supports Root Complex and End Point
- Supports Gen1 (2.5Gb/s), Gen2 (5Gb/s)
- Up to six BARs, resizable
- Lane reversal
- Lane reversal
- Supports CrossLink connection mode
- Supports Multicast
- Supports ARI (Alternative Routing-ID Interpretation)
- Supports IDO (ID-based Ordering)
- Retimer (extension device) presence detection
- Supports TPH (TLP Processing Hints)
- Supports ACS (Access Control Services)
- Supports DPC (Downstream Port Containment)
- Supports PTM (Precision Time Measurement)
- Supports Autonomous link speed/width change
- Supports advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC (ECRC) Advanced Error Reporting and ECRC features
- Configurable parameters: channel width, maximum payload size, FPGA logical interface speeds, reference clock frequency, base address register decoding and filtering, etc.

For further information about PCIe Controller, please refer to *IPUG1020，Arora V PCIe Controller User Guide.*

2.8 MIPI D-PHY

2.8.1 MIPI D-PHY RX(GW5AST-138)

GW5AST-138 provides a MIPI D-PHY RX hardcore supporting the “MIPI Alliance Standard for D-PHY Specification(V1.2)”. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays. The main features are as follows:

- High Speed RX at up to 20 Gbps (eight data lanes).
- One MIPI Quad supports up to four data lanes and one clock lane.
- Bidirectional Low-power (LP) mode at up to 10Mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric’s user interface
- Supports MIPI DSI and MIPI CSI-2 link layers

For more information on Gowin MIPI D-PHY RX, pleae refer to *UG296, Arora V Hardened MIPI D-PHY User Guide.*

2.9 RiscV AE350_SOC

TBD

2.10 ADC

The GW5AST series of FPGA Products integrate a new flexible analog interface as a temperature and power sensor. When combined with the programmable logic capability of the FPGA, the sensor can address the data acquisition and monitoring requirements for temperature and power monitoring.

Highlights of the sensor architecture include:

- On-chip reference, no off-chip voltage reference required
- 60dB SNR
- 10-bit oversampling @ 2MHz
- 1kHz Signal Bandwidth
- two dedicated analog channels, able to detect input signals from GPIO at the same time
- On-chip temperature (±4°C max error) and voltage (±1% max error) sensors
- Continuous access to ADC measurements

The sensor optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails.

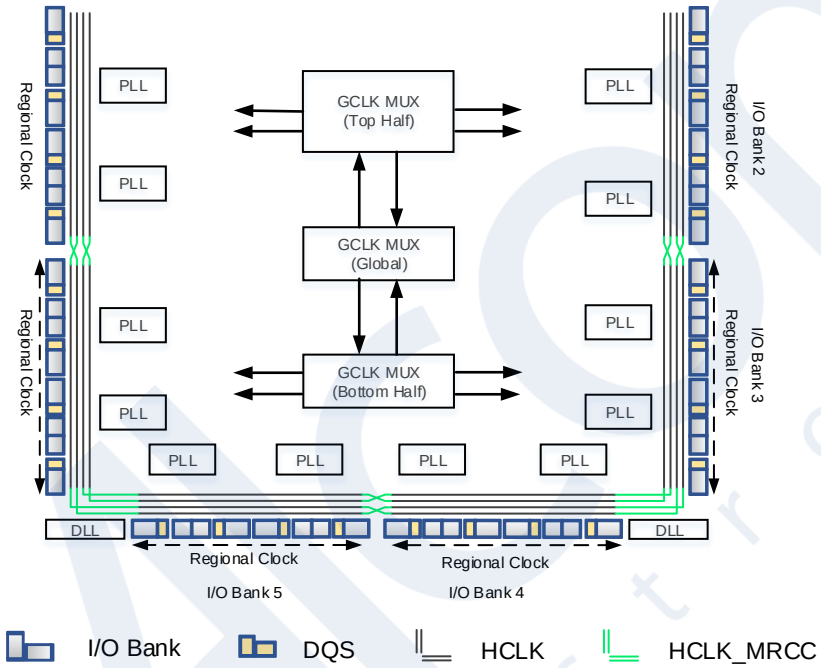
The most recent measurement results (together with maximum and minimum readings) are stored in dedicated registers for access at any time via the user interface.

For more information on ADC, see *UG299, Arora V Analog to Digital Converter (ADC) User Guide*.

2.11 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. GW5AST series of FPGA Products provide the global clock network (GCLK) which connects to all the registers directly. In addition to the GCLK, PLL, HCLK, DDR memory interface, and DQS, etc. are also provided.

Figure 2-14 Clock resource



Please refer to 2.11.1 ~ 2.11.4 for a brief introduction. For further detailed information on the GCLK, HCLK, DDR memory interface, and DQS, see *UG306, Arora V Clock User Guide*.

2.11.1 Global Clock

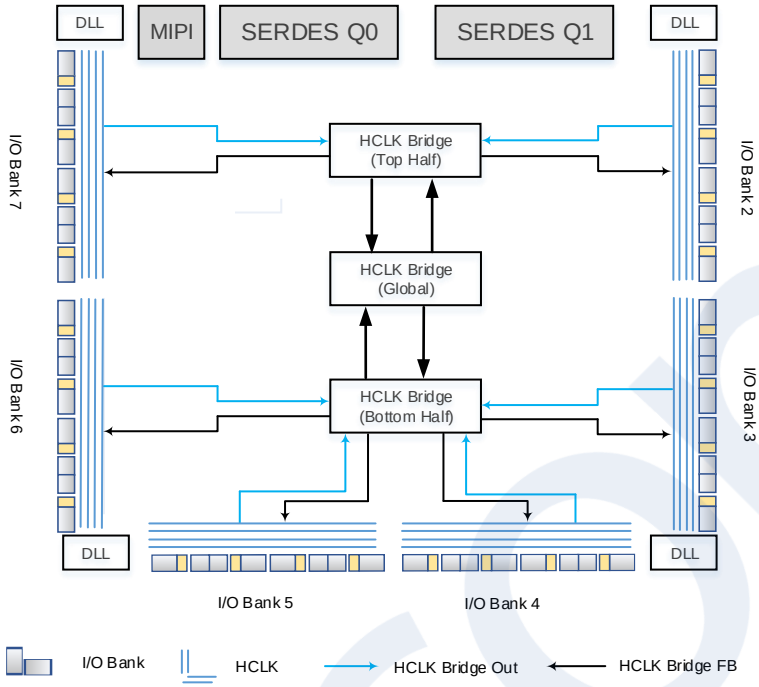
GW5AST series FPGA products provide 16 global clocks. The clock source of GCLK comes from dedicated clock pins, PLL output, SERDES clock, HCLK output and common wiring resources. Dedicated clock input pins offer better clock performance and enable global driving.

2.11.2 HCLK

HCLK is the high-speed clock with low jitter and low skew. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. One bank supports 4 HCLKs, as

shown in Figure 2-15.

Figure 2-15 GW5AST HCLK Distribution



HCLK can provide users with the function modules as follows:

- Dynamic high-speed clock enable module. Able to dynamically turn on/off the high-speed clock signal.
- High speed clock frequency division module, generating a divided clock of the input clock. Used in the IO logic mode.
- Dynamic high speed clock selector.
- Dynamic delay adjustment module, producing the clock signal for the dedicated clock pin input.
- The HCLK bridge module is able to send HCLK clock signals to any of the Banks. In addition, the HCLK clock signal can span to the clock tree of the adjacent IO Bank after entering from the IO Bank.

Note!

For high speed signals of the same source, it is recommended to put them in the same IO Bank to achieve a minimum skew between signals.

2.11.3 Phase-locked Loop

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

The PLL module of the GW5AST series FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

The features of the PLL module of the GW5AST series FPGA products are as follows:

- Supports seven clock outputs
- Integer PLL, the first clock output and feedback clock output support 1/8 fractional output division
- Supports phase shift and duty cycle adjustment
- Frequency Lock detection
- Supports spread spectrum clock generation (IP required)
- VCO frequency range: 800 MHz ~ 2000 MHz
- CLKIN frequency range: 10 MHz ~ 400 MHz.

2.11.4 DDR Memory Interface Clock Management DQS

The DQS module of the GW5AST series of FPGA Products provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase
- Provide a read / write pointer for input cache
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module supports multiple operating modes to meet the needs of different I/O interfaces.

2.11.5 Long Wire

As a supplement to CRU, the GW5AST series of FPGA products provide another routing resource- Long Wire, which is suitable for clock, clock enable, set/reset, or other high fan out signals.

2.12 Global Set/Reset (GSR)

A global set/rest (GSR) network is built in the GW5AST series of FPGA Product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

2.13 Programming & Configuration

The GW5AST series of FPGA Products support SRAM configuration. Each time the device is powered on, the bitstream needs to be downloaded to configure the device. Of course, you can also save the configuration data in an external Flash. After power-up, the GW5AST device loads configuration data from the external Flash into the SRAM.

Besides JTAG, the GW5AST series of FPGA Products also support GOWINSEMI's own GowinCONFIG configuration mode: SSPI, MSPI, CPU, SERIAL. The FPGAs also support background programming,

datastream file encryption and security bit setting, SEU detection and error correction, and OTP. For more information, please refer to *UG704, Arora V FPGA Products Programming and Configuration User Guide*.

Background Upgrade

GW5AST series of FPGAs support background upgrade by JTAG/SSPI/QSSPI or UserLogic, that is, the device supports programming the embedded Flash or the external Flash without affecting the existing working state, the device can work normally according to the original configuration during the programming process. And after the programming is completed, trigger RECONFIG_N with a low level to complete the online upgrade. This feature applies to the applications requiring long online time and irregular upgrades.

Bitstream File Encryption & Security Bit Setting

GW5AST series of FPGA Products support bitstream data encryption with 128-bit AES encryption algorithm. At the same time, GOWINSEMI adds CRC and sets security bits in the bitstream file of FPGA products by default in order to guarantee the safe and accurate transmission of configuration data. During the data configuration process, the input data is verified in real time for errors, and the device cannot be woken up by incorrect data. After the configuration of the bitstream with security bit is complete, data readback cannot be performed.

CMSER

The configuration SRAM of GW5AST series of FPGA products supports configuration memory soft error recovery (CMSER), which are mainly used for data detection and correction of the FPGA configuration data and are disabled by default. The features are as follows:

- Supports ECC and CRC error detection and correction. Turning on the auto-on mode after wakeup according to the user configuration or using the user design logic control to turn on/off error detection and correction
- ECC supports 1-bit error location report and error correction and 2-bit error alarm per 64-bit SRAM data
- CRC supports any bit error alarm
- Supports 1-bit error injection at any position, one error per 64-bit SRAM data
- The detection and error correction function of SRAM in this storage area will be automatically turned off when the user turns on the SSRAM storage function

OTP

GW5AST series of FPGA products provide a 128-bit OTP space and support one-time programming. Bit0 ~ Bit31 is the user space, which can be used to store security and other important information. Bit32~Bit95 is the DNA space, which stores the 64-bit unique identification information of the device.

2.14 On Chip Oscillator

There is an internal oscillator in each of the GW5AST series of FPGA Products. During the configuration process, it can provide a clock for the MSPI mode. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is employed to get the output clock frequency:

f_{out}=210MHz/Param。

Note!

“Param” is the configuration parameter. It is 3 or an even number between 2 and 126.

3 AC/DC Characteristic

Note!

You should ensure GOWINSEMI® products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI® does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage	-0.5V	1.05V
V_{CCIO}	I/O Bank voltage	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	1.98V
V_{CC_REG}	Regulator voltage	-0.5V	3.75V
V_{IN}	Single-ended input	-0.4V	3.75V
	Differential input	-0.4V	2.625V
Gigabit Transceiver			
V_{ddha}	Analog high power supply	-0.5V	1.98V
V_{dda}	Analog core power supply	-0.5V	1.05V
$V_{ddd\_In0\sim 4}$	Tx power supply	-0.5V	1.05V
MIPI			
V_{dda}	Analog core power supply	-0.5V	1.05V
V_{ddx}	Analog high voltage power supply	-0.5V	1.98V
Temperature			
Storage Temperature	Storage Temperature	-65 ℃	+150℃
Junction Temperature	Junction Temperature	-40 ℃	+125℃

3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Range

Name	Description	Min.	Max.
V_{CC}	Core voltage	0.87V	1.0V
V_{CCIO}	I/O Bank voltage	1V	3.465V
V_{CCX}	Auxiliary voltage	1.71V	1.89V
V_{CC_REG}	Regulator voltage	1.14V	3.3V
Gigabit Transceiver			
V_{ddha}	Analog high power supply	1.71V	1.89V
V_{dda}	Analog core power supply	0.87V	1.0V
$V_{ddd\_In0\sim 4}$	Tx power supply	0.87V	1.0V
MIPI			
V_{dda}	Analog core power supply	0.87V	1.0V
V_{ddx}	Analog high voltage power supply	1.71V	1.89V
Temperature			
T_{JCOM}	Junction temperature Commercial operation	0 ℃	+85 ℃
T_{JIND}	Junction temperature Industrial operation	-40℃	+100℃

Note!

For the power supply information for different packages, please refer to UG982-GW5AST-138 Pinout.

3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
T_{RAMP}	Power supply ramp rates	0.02mV/μs	TBD	50mV/μs

3.1.4 Hot Socket Specifications

Table 3-4 Hot Socket Specifications

Name	Description	Condition	I/O	Max.
I_{HS}	Input or I/O leakage current	$V_{IN}=V_{IL}$ (MAX)	I/O	TBD
I_{HS}	Input or I/O leakage current	$V_{IN}=V_{IL}$ (MAX)	TDI, TDO, TMS,TCK	TBD

3.1.5 POR Specifications

Table 3-5 POR Paramrters

Name	Description	Name	Typ.
POR Voltage	Power on reset voltage	V_{CC}	0.72V
		V_{CCX}	1.5V

		V_{CCIO} (Bank10)	1.04V

3.2 ESD performance

Table 3-6 GW5AST ESD - HBM

Device	HBM
GW5AST-138	HBM > 1000V

Table 3-7 GW5AST ESD - CDM

Device	CDM
GW5AST-138	CDM > 250V

3.3 DC Characteristics

3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCIO}<V_{IN}<V_{IH}$ (MAX)	-	TBD	TBD
		$0V<V_{IN}<V_{CCIO}$	-	TBD	TBD
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCIO}$	-	TBD	TBD
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX)$<V_{IN}<V_{CCIO}$	-	TBD	TBD
C1	GPIO Capacitance	-		9pF	TBD
V_{HYST}	Hysteresis for Schmitt Trigge inputs	V_{CCIO}= 3.3V, Hysteresis=L2H	-	250	TBD
		V_{CCIO}= 2.5V, Hysteresis=L2H	-	90	TBD
		V_{CCIO}= 1.8V, Hysteresis=L2H	-	50	TBD
		V_{CCIO}= 1.5V, Hysteresis=L2H	-	40	TBD
		V_{CCIO}= 1.2V, Hysteresis=L2H		40mV	TBD
		V_{CCIO}= 3.3V, Hysteresis=H2L	-	310	TBD
		V_{CCIO}= 2.5V, Hysteresis=H2L	-	130	TBD
		V_{CCIO}= 1.8V, Hysteresis=H2L	-	50	TBD
		V_{CCIO}= 1.5V, Hysteresis=H2L	-	30	TBD
		V_{CCIO}= 1.2V, Hysteresis=H2L		30mV	TBD
		V_{CCIO}= 3.3V, Hysteresis=High	-	560	TBD
		V_{CCIO}= 2.5V, Hysteresis=High	-	220	TBD

Name	Description	Condition	Min.	Typ.	Max.
		V_{CCIO}= 1.8V, Hysteresis=High	-	100	TBD
		V_{CCIO}= 1.5V, Hysteresis=High	-	70	TBD
		V_{CCIO}= 1.2V, Hysteresis=High		70mV	TBD

3.3.2 Static Current

Table 3-9 Static Current

Name	Description	LV/UV	Device	Typ.[1]
I_{CC}	Core Current	LV	GW5AST-138	100 mA
I_{CCX}	V_{CCX} current (VCCX=2.5V)	LV	GW5AST-138	9 mA
I_{CCIO}	I/O Bank current (V_{CCIO}=3.3V)	LV	GW5AST-138	5 mA
I_{CC_REG}	Static Current (Built-in Regulator)	LV	GW5AST-138	6 mA

Note!

[1] The test condition for the typical value is 25℃.

3.3.3 Recommended I/O Operating Conditions

Table 3-10 I/O Operating Conditions Recommended

Name	Output V_{CCIO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-

Name	Output V_{CCIO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E[1]	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Note!

V_{CCIO} of Banks with True LVDS is recommended to be set to 2.5 V.

3.3.4 Single ended I/O DC Characteristic

Table 3-11 Single-ended DC Characteristic

Name	V_{IL} (V)		V_{IH} (V)		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	V_{CCIO} +0.3	0.4V	V_{CCIO}- 0.4 V.	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCIO}- 0.2 V.	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	V_{CCIO} +0.3	0.4V	V_{CCIO}- 0.4 V.	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}- 0.2 V.	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} +0.3	0.4V	V_{CCIO}-0.4 V.	4	-4
							8	-8
							12	-12
					0.2V	V_{CCIO}- 0.2 V.	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}		0.4V	V_{CCIO}- 0.4 V.	4	-4

Name	V_{IL} (V)		V_{IH} (V)		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
				V_{CCIO} +0.3			8	-8
					0.2V	V_{CCIO}- 0.2 V.	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} +0.3	0.4V	V_{CCIO}- 0.4 V.	2	-2
							4	-4
					0.2V	V_{CCIO}- 0.2 V.	0.1	-0.1
LVCMOS10	-0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} +0.3	0.4V	V_{CCIO}- 0.4 V.	4	-4
PCI33	-0.3V	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} +0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	-0.5
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	V_{CCIO} +0.3	0.4V	V_{CCIO}-0.4 V.	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	V_{CCIO} +0.3	0.40V	V_{CCIO}- 0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1 V.	V_{CCIO} +0.3	0.40V	V_{CCIO}- 0.40V	8	-8
SSTL135	-0.3	V_{REF}-0.09V	V_{REF}+0.09V	V_{CCIO} +0.3	0.40V	V_{CCIO}- 0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1 V.	V_{CCIO} +0.3	0.40V	V_{CCIO}- 0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1 V.	V_{CCIO} +0.3	0.40V	V_{CCIO}- 0.40V	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1 V.	V_{CCIO} +0.3	0.40V	V_{CCIO}- 0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1 V.	V_{CCIO} +0.3	0.40V	V_{CCIO}- 0.40V	NA	NA
HSUL12	-0.3	V_{REF}-0.13V	V_{REF}+ 0.13V	V_{CCIO} +0.3	0.40	V_{CCIO}- 0.40V	0.1	-0.1

Note!

[1] The total DC current limit (sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

3.3.5 Differential I/O DC Characteristic

Table 3-12 Differential I/O DC Characteristic

Name	Description	Conditions	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage	TBD	-0.4		2.625	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.3	1.2	1.8	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	100	300	600	mV
I_{IN}	Input Current	Power On or Power Off	TBD	20	TBD	μA
V_{OH}	Output High Voltage for VOP or VOM	R_T = 100 Ω	TBD	TBD	1.675	V
V_{OL}	Output High Voltage for VOP or VOM	R_T = 100 Ω	0.7	TBD	TBD	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	600	mV
ΔV_{OD}	Change in VOD Between High and Low	TBD	TBD	TBD	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.000	1.250	1.425	V
ΔV_{OS}	Change in VOS Between High and Low	TBD	TBD	TBD	TBD	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	TBD	12	TBD	mA

3.4 AC Switching Characteristics

3.4.1 CFU Switching Characteristics

Table 3-13 CFU Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	-	ns
t_{SR_CFU}	Set/Reset to Register output	-	-	ns
t_{CO_CFU}	Clock to Register output	-	-	ns

3.4.2 BSRAM Switching Characteristics

Table 3-14 BSRAM Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	-	ns
t_{COOR_BSRAM}	Clock to output from output register	-	-	ns

3.4.3 DSP Switching Characteristics

Table 3-15 DSP Timing Parameters

Name	Description	Speed Grade	Unit

		Min	Max	
t_{COIR_DSP}	Clock to output from input register	-	-	ns
t_{COPR_DSP}	Clock to output from pipeline register	-	-	ns
t_{COOR_DSP}	Clock to output from output register	-	-	ns

3.4.4 Clock and I/O Switching Characteristic

Table 3-16 External Switching Characteristics

Name	Description	Device	-8		-7		Unit
			Min	Max	Min	Max	
Pin-LUT-Pin Delay(1)	Pin(IOxA) to Pin(IOxB) delay	GW5AST-138	-	-	-	-	ns
$T_{HCLKdly}$	HCLK tree delay	GW5AST-138	-	-	-	-	ns
$T_{GCLKdly}$	GCLK tree delay	GW5AST-138	-	-	-	-	ns

3.4.5 On chip Oscillator Switching Characteristics

Table 3-17 On chip Oscillator Switching Characteristics

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to + 85° C)	199.5 MHz	210 MHz	220.5 MHz
	Output Frequency (-40 to +100° C)	189 MHz	210 MHz	231 MHz
t_{DT}	Output Clock Duty Cycle	-	50%	-
t_{OPJIT}	Output Clock Period Jitter	TBD	TBD	TBD

3.4.6 PLL Switching Characteristics

Table 3-18 PLL Switching Characteristic

Device	Name	Min.	Max.
GW5AST-138	CLKIN	10 MHz	400 MHz
	PFD	10 MHz	400 MHz
	VCO	800 MHz	2 GHz
	CLKOUT	6.25MHz[1]	1 GHz

Note!

6.25MHz is the minimum frequency of CLKOUT in non-cascaded mode.

3.5 Gigabit Transceiver Performance

3.5.1 Transceiver Performance

Table 3-19 Transmitter and Receiver Data Rate Perfromance

Name/Description	Condition	Transceiver Speed Grade			Unit
		1	2	3	
	Max. data rate(typical Voltage)	–	12.5	–	Gbps

Name/Description	Condition	Transceiver Speed Grade			Unit
		1	2	3	
On board application(chip to chip)[1]	Min. data rate[3]	–	125	–	Mbps
Backplane[2]	Max. data rate(typical Voltage)	–	8	–	Gbps
	Min. data rate[4]	–	125	–	Mbps

Note!

- [1] Less channel loss for chip-chip applications.
- [2] For backplance applications, the maximum channel loss should be within PCIE 3.0 standard.
- [3] [4] The oversampling logic should be enabled.

3.5.2 Transceiver PLL Performance

Table 3-20 Transceiver PLL Performance

Name/Description	Condition	SpeedGrade-2		Unit
		Min	Max	
Quad PLL 0	Working range	1.25	6.5	GHz
Quad PLL 1	Working range	3.8	6.5	GHz
Channel PLL	Working range	1.25	6.5	GHz

3.6 Configuration Interface Timing Specification

The GW5AST series of FPGA Products support multiple GowinCONFIG modes: SSPI, MSPI, SERIAL and CPU. For further detailed information, please refer to *UG704, Arora V FPGA Products Programming and Configuration Guide*.

4 Ordering Information

4.1 Part Name

Figure 4-1 Part Naming Examples–ES

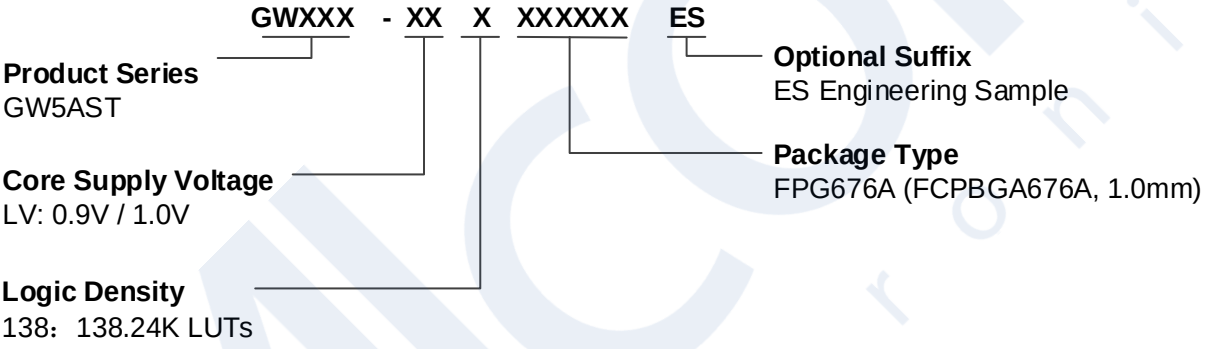
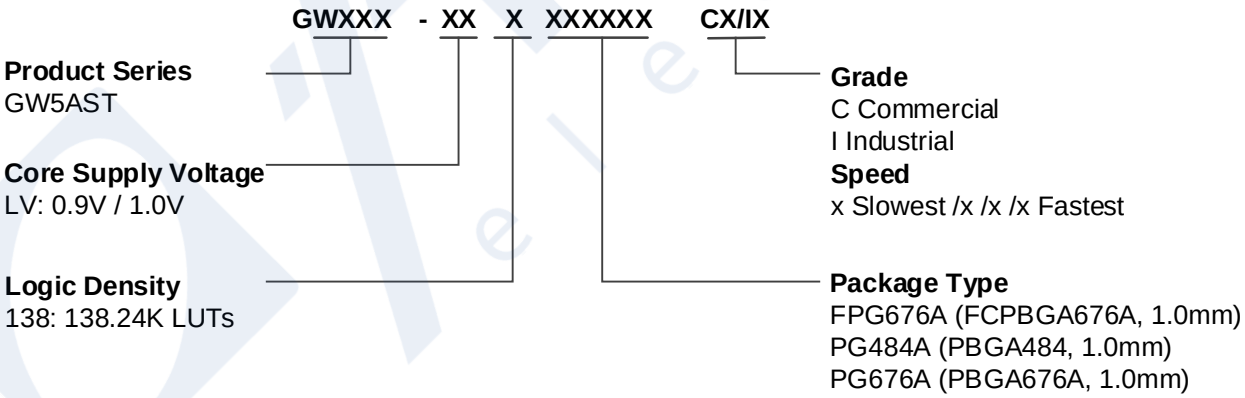


Figure 4-2 Part Naming Examples–Production



Note!

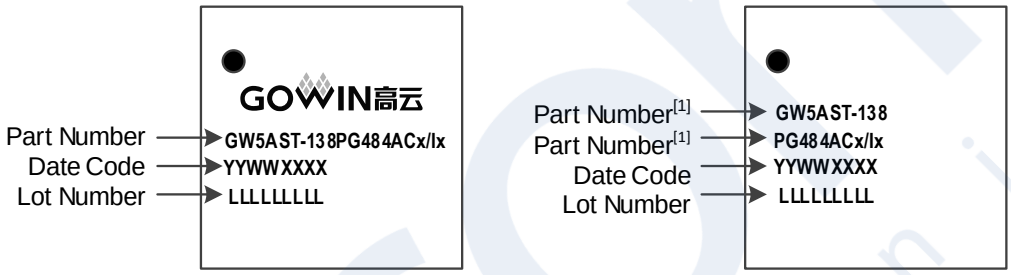
- For the further detailed information about the package information, please refer to 1.2 Product Resources > Table 1-2 Package Information and Maximum Number of User I/Os.
- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.

- Both “C” and “I” are used in GOWIN part name marking for one device, such as C8/I7, C6/I5, etc. GOWIN devices are screened using industrial standards, so one same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the same chip meets the speed grade 8 in the commercial grade application, the speed grade is 7 in the industrial grade application.

4.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in .

Figure 4-3 Package Mark Examples



Note!

[1] The first two lines in the right figure above are the “Part Number”.

5 About This Guide

5.1 Purpose

This data sheet describes the features, product resources, structure, AC/DC characteristics, and the ordering information of the GW5AST series of FPGA Products, making it easier to understand the GW5AST series of FPGA Products and select and use our devices.

5.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- UG704, Arora V FPGA Products Programming and Configuration User Guide
- UG983, GW5AST series of FPGA Products Package and Pinout Manual
- UG982, GW5AST-138 Pinout
- UG984, Arora V FPGA Products Schematic Manual

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ADC	Analog to Digital Converter
AER	Advanced Error Reporting
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CMSER	Configuration Memory Soft Error Recovery
CRU	Configurable Routing Unit

Terminology and Abbreviations	Full Name
CSI	Camera Serial Interface
CTC	Clock Tolerance Compensation
CTLE	Continuous Time Linear Equalizer
DCS	Dynamic Clock Selector
DFF	D Flip-floor
DNA	Device Identifier
DP	True Dual Port 16K BSRAM
DSI	Display Serial Interface
DSP	Digital Signal Processing
ECC	Error Correction Code
ECRC	End-to-End Cyclic Redundancy Check
ESD	Electro-Static Discharge
FIFO	First In First Out
FPG	FCPBGA
FPGAs	Field Programmable Gate Array
GCLK	Global Clock
GPIO	Gowin Programmable IO
GSR	Global Set/Reset
HCLK	High Speed Clock
IOB	Input/Output Block
LUT	Look-up Table
LW	Long Wire
MIPI	Mobile Industry Processor Interface
OTP	One Time Programmable
PCIe	Peripheral Component Interface Express
PCS	Physical Coding Sublayer
PLL	Phase-locked Loop
PMA	Physical Medium Attachment Sublayer
REG	Register
SDP	Semi Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com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