CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS

SG-8200CJ

Product Number
X1G006211xxxx16

- Frequency range : 1.2 MHz to 170 MHz
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance, operating temperature:
  ±50 × 10^{-6} (-40 ºC to +125 ºC)
- External dimensions : 2.0 × 1.6 × 0.6 (mm)
- PLL technology to enable setting any output frequency

Specifications (characteristics)

Item	Symbol	Specifications			Conditions/Remarks
Supply voltage	V_{CC}	1.80 V Typ.	2.50 V Typ.	3.30 V Typ.	
		1.62 V to 1.98 V	2.25 V to 2.75 V	2.97 V to 3.63 V	
Output frequency range	f_O	1.2 MHz to 170 MHz			
Storage temperature	T_stg	-55 °C to +125 °C			Storage as single product.
Operating temperature	T_use	J: -40 °C to +125 °C			
Frequency tolerance[*1]	f_tol	J: ±50 × 10^{-6}			T_use = -40 °C to +125 °C
Current consumption	I_{CC}	5.2 mA Typ.	5.4 mA Typ.	5.6 mA Typ.	1.2 MHz ≤ f_O ≤ 25 MHz; No load, Rise/Fall time: Default
		7.0 mA Max.	7.2 mA Max.	7.5 mA Max.	
		5.4 mA Typ.	5.7 mA Typ.	6.1 mA Typ.	25 MHz < f_O ≤ 50 MHz
		7.3 mA Max.	7.6 mA Max.	8.1 mA Max.	
		5.7 mA Typ.	6.3 mA Typ.	7.0 mA Typ.	50 MHz < f_O ≤ 75 MHz
		7.7 mA Max.	8.2 mA Max.	9.1 mA Max.	
		6.2 mA Typ.	6.9 mA Typ.	7.9 mA Typ.	75 MHz < f_O ≤ 100 MHz
		8.2 mA Max.	9.1 mA Max.	10.4 mA Max.	
		6.9 mA Typ.	7.9 mA Typ.	9.1 mA Typ.	100 MHz < f_O ≤ 125 MHz
		9.4 mA Max.	10.7 mA Max.	12.4 mA Max.	
		7.8 mA Typ.	9.2 mA Typ.	11.2 mA Typ.	125 MHz < f_O ≤ 170 MHz
		10.4 mA Max.	12.4 mA Max.	15.0 mA Max.	
Output disable current	I_dis	5.0 mA Typ.	5.0 mA Typ.	5.1 mA Typ.	OE = GND (Active High) $\overline{OE}$ = V_{CC} (Active Low)
		7.2 mA Max.	7.3 mA Max.	7.4 mA Max.	
Standby current	I_std	0.3 µA Typ.	0.3 µA Typ.	0.5 µA Typ.	$\overline{ST}$ = GND (Active High) ST = V_{CC} (Active Low)
		15.0 µA Max.	15.0 µA Max.	15.0 µA Max.	
Symmetry	SYM	45 % to 55 %			50 % V_{CC} Level, L_CMOS ≤ 15 pF
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.			Rise/Fall time: Default 'A' Option[*2] / Other Options; I_{OH}; I_{OL} fo > 125 MHz / B: Faster / -2.0 mA / 2.0 mA 75 MHz < fo ≤ 125 MHz / C: Fast / -1.0 mA / 1.0 mA 50 MHz < fo ≤ 75 MHz / D: Slow / -0.5 mA / 0.5 mA fo ≤ 50 MHz / E: Slower / -0.2 mA / 0.2 mA
	V_{OL}	10 % V_{CC} Max.			
Output load condition	L_CMOS	15 pF Max.			
Input voltage	V_{IH}	70 % V_{CC} Min.			Pin 1
	V_{IL}	30 % V_{CC} Max.			
Rise/Fall time	tr/tf	-			Default 'A' Option[*2] / Other Options; 20 % - 80 % V_{CC}, L_CMOS = 15 pF
		2.0 ns Max.			fo > 125 MHz / B: Faster
		2.5 ns Max.			75 MHz < fo ≤ 125 MHz / C: Fast
		4.0 ns Max.			50 MHz < fo ≤ 75 MHz / D: Slow
		6.0 ns Max.			fo ≤ 50 MHz / E: Slower
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.			Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC} or measured from the time $\overline{OE}$ or ST pin crosses 70 % V_{CC}
Output enable time (OE)	tsta_oe	100 ns + 2 clock cycle Max.			Measured from the time OE pin crosses 70 % V_{CC} or measured from the time $\overline{OE}$ pin crosses 30 % V_{CC}
Output enable time (ST)	tsta_st	3 ms Max.			Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC} or measured from the time ST pin crosses 30 % V_{CC}
Start-up time	t_str	3 ms Max.			Measured from the time V_{CC} reaches its rated minimum value, 1.62 V
Phase Jitter	t_{PJ}	1.2 ps Typ.			fo = 25 MHz, Offset frequency: 12 kHz to 5 MHz
		1.2 ps Typ.			fo = 50 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 75 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 100 MHz, Offset frequency: 12 kHz to 20 MHz
		1.1 ps Typ.			fo = 125 MHz, Offset frequency: 12 kHz to 20 MHz
		1.4 ps Typ.			fo = 150 MHz, Offset frequency: 12 kHz to 20 MHz
		1.5 ps Typ.			fo = 170 MHz, Offset frequency: 12 kHz to 20 MHz
Frequency aging	f_age	This is included in frequency tolerance specification.			+25 °C, first year

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, load drift and aging (+25 °C, 1 year).
*2 Default 'A' Rise/Fall time and I_{OH}/I_{OL} are dependent on programmed frequency.

Pin description

Pin	Name	I/O type	Function		
1	OE	Input	Output Enable (Active High)	High[*1] or Open:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	$\overline{ST}$	Input	Standby (Active High)	High[*1 *2]:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
	$\overline{OE}$	Input	Output Enable (Active Low)	Low[*3] or Open:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	ST	Input	Standby (Active Low)	Low[*3 *4]:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground		
3	OUT	Output	Clock output		
4	V_{CC}	Power	Power supply		

*1 If fixing it at High, please connect to V_{CC} directly.
*2 If necessary to use Open, please select Output Enable (Active High) function.
*3 If fixing it at Low, please connect to GND directly.
*4 If necessary to use Open, please select Output Enable (Active Low) function.

Product Name

SG-8200CJ 170.000000MHz T J J P A
① ② ③ ④⑤⑥⑦⑧

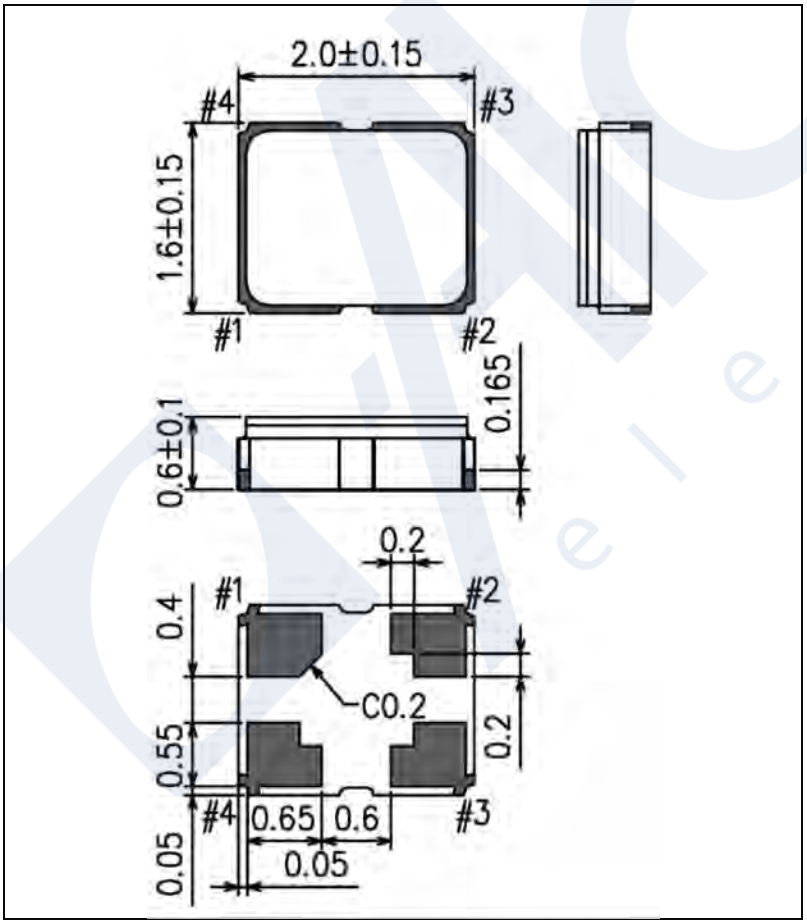
①Model ②Package type (CJ: 2.0 mm × 1.6 mm)
③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance ⑥Operating temperature
⑦Function ⑧Rise/Fall time

⑤Frequency tolerance / ⑥Operating temperature	
JJ	±50 x 10^{-6} / -40 °C to +125 °C

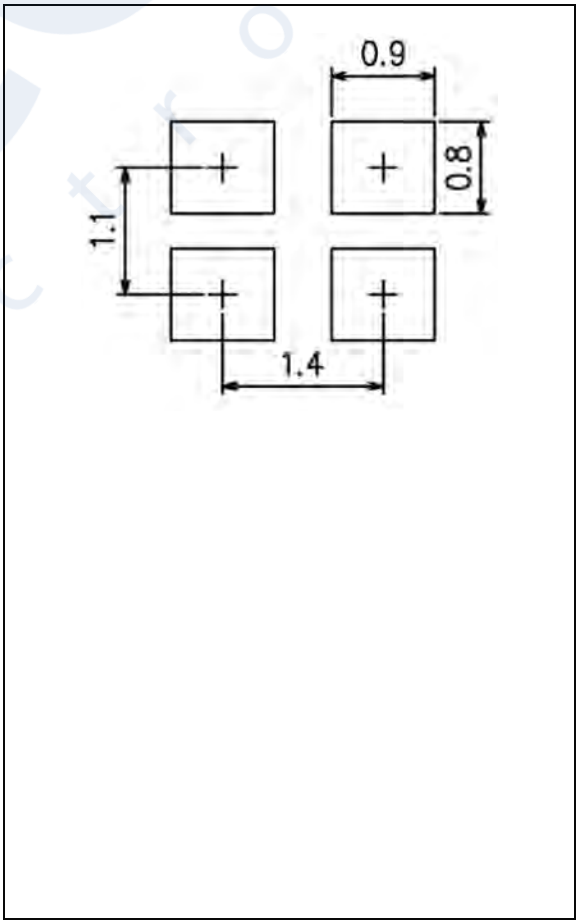
⑦Function	
P	Output Enable (OE) / Active High
S	Standby ($\overline{ST}$) / Active High
Q	Output Enable ($\overline{OE}$) / Active Low
T	Standby (ST) / Active Low

⑧Rise/Fall time	
A	Default
B	Faster
C	Fast
D	Slow
E	Slower

External dimensions (Unit: mm)



Footprint (Recommended) (Unit: mm)



■Notes:
In order to achieve optimum jitter performance, the 0.01 µF to 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS

SG-8201CJ

Product Number
X1G005981xxxx16

- Frequency range : 1.2 MHz to 170 MHz
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance, operating temperature:
  ±15 × 10^{-6} (-40 ºC to +105 ºC)
  ±25 × 10^{-6} (-40 ºC to +125 ºC)
- External dimensions : 2.0 × 1.6 × 0.6 (mm)
- PLL technology to enable setting any output frequency

Specifications (characteristics)

Item	Symbol	Specifications			Conditions/Remarks
Supply voltage	V_{CC}	1.80 V Typ. 1.62 V to 1.98 V	2.50 V Typ. 2.25 V to 2.75 V	3.30 V Typ. 2.97 V to 3.63 V	
Output frequency range	f_O	1.2 MHz to 170 MHz			
Storage temperature	T_stg	-55 °C to +125 °C			Storage as single product.
Operating temperature	T_use	H: -40 °C to +105 °C			
		J: -40 °C to +125 °C			
Frequency tolerance[*1]	f_tol	B: ±15 × 10^{-6}			T_use = -40 °C to +105 °C
		D: ±25 × 10^{-6}			T_use = -40 °C to +125 °C
Current consumption	I_{CC}	5.2 mA Typ.	5.4 mA Typ.	5.6 mA Typ.	1.2 MHz ≤ f_O ≤ 25 MHz; No load, Rise/Fall time: Default
		7.0 mA Max.	7.2 mA Max.	7.5 mA Max.	
		5.4 mA Typ.	5.7 mA Typ.	6.1 mA Typ.	25 MHz < f_O ≤ 50 MHz
		7.3 mA Max.	7.6 mA Max.	8.1 mA Max.	
		5.7 mA Typ.	6.3 mA Typ.	7.0 mA Typ.	50 MHz < f_O ≤ 75 MHz
		7.7 mA Max.	8.2 mA Max.	9.1 mA Max.	
		6.2 mA Typ.	6.9 mA Typ.	7.9 mA Typ.	75 MHz < f_O ≤ 100 MHz
		8.2 mA Max.	9.1 mA Max.	10.4 mA Max.	
		6.9 mA Typ.	7.9 mA Typ.	9.1 mA Typ.	100 MHz < f_O ≤ 125 MHz
		9.4 mA Max.	10.7 mA Max.	12.4 mA Max.	
		7.8 mA Typ.	9.2 mA Typ.	11.2 mA Typ.	125 MHz < f_O ≤ 170 MHz
		10.4 mA Max.	12.4 mA Max.	15.0 mA Max.	
Output disable current	I_dis	5.0 mA Typ.	5.0 mA Typ.	5.1 mA Typ.	OE = GND (Active High) $\overline{OE}$ = V_{CC} (Active Low)
		7.2 mA Max.	7.3 mA Max.	7.4 mA Max.	
Standby current	I_std	0.3 µA Typ.	0.3 µA Typ.	0.5 µA Typ.	$\overline{ST}$ = GND (Active High) ST = V_{CC} (Active Low)
		15.0 µA Max.	15.0 µA Max.	15.0 µA Max.	
Symmetry	SYM	45 % to 55 %			50 % V_{CC} Level, L_CMOS ≤ 15 pF
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.			Rise/Fall time: Default 'A' Option[*2] / Other Options; I_{OH} / I_{OL} fo > 125 MHz / B: Faster / -2.0 mA / 2.0 mA 75 MHz < fo ≤ 125 MHz / C: Fast / -1.0 mA / 1.0 mA 50 MHz < fo ≤ 75 MHz / D: Slow / -0.5 mA / 0.5 mA fo ≤ 50 MHz / E: Slower / -0.2 mA / 0.2 mA
	V_{OL}	10 % V_{CC} Max.			
Output load condition	L_CMOS	15 pF Max.			
Input voltage	V_{IH}	70 % V_{CC} Min.			Pin 1
	V_{IL}	30 % V_{CC} Max.			
Rise/Fall time	tr/tf	-			Default 'A' Option[*2] / Other Options; 20 % - 80 % V_{CC}, L_CMOS = 15 pF
		2.0 ns Max.			fo > 125 MHz / B: Faster
		2.5 ns Max.			75 MHz < fo ≤ 125 MHz / C: Fast
		4.0 ns Max.			50 MHz < fo ≤ 75 MHz / D: Slow
		6.0 ns Max.			fo ≤ 50 MHz / E: Slower
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.			Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC} or measured from the time $\overline{OE}$ or ST pin crosses 70 % V_{CC}
Output enable time (OE)	tsta_oe	100 ns + 2 clock cycle Max.			Measured from the time OE pin crosses 70 % V_{CC} or measured from the time $\overline{OE}$ pin crosses 30 % V_{CC}
Output enable time (ST)	tsta_st	3 ms Max.			Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC} or measured from the time ST pin crosses 30 % V_{CC}
Start-up time	t_str	3 ms Max.			Measured from the time V_{CC} reaches its rated minimum value, 1.62 V
Phase Jitter	t_{PJ}	1.2 ps Typ.			fo = 25 MHz, Offset frequency: 12 kHz to 5 MHz
		1.2 ps Typ.			fo = 50 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 75 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 100 MHz, Offset frequency: 12 kHz to 20 MHz
		1.1 ps Typ.			fo = 125 MHz, Offset frequency: 12 kHz to 20 MHz
		1.4 ps Typ.			fo = 150 MHz, Offset frequency: 12 kHz to 20 MHz
		1.5 ps Typ.			fo = 170 MHz, Offset frequency: 12 kHz to 20 MHz
Frequency aging	f_age	This is included in frequency tolerance specification.			+25 °C, first year

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, load drift and aging (+25 °C, 1 year).
*2 Default 'A' Rise/Fall time and I_{OH}/I_{OL} are dependent on programmed frequency.

Pin description

Pin	Name	I/O type	Function		
1	OE	Input	Output Enable (Active High)	High[*1] or Open:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	$\overline{ST}$	Input	Standby (Active High)	High[*1 *2]:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
	$\overline{OE}$	Input	Output Enable (Active Low)	Low[*3] or Open:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	ST	Input	Standby (Active Low)	Low[*3 *4]:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground		
3	OUT	Output	Clock output		
4	V_{CC}	Power	Power supply		

*1 If fixing it at High, please connect to V_{CC} directly.
*2 If necessary to use Open, please select Output Enable (Active High) function.
*3 If fixing it at Low, please connect to GND directly.
*4 If necessary to use Open, please select Output Enable (Active Low) function.

Product Name

SG-8201CJ 170.000000MHz T D J P A
① ② ③ ④⑤⑥⑦⑧

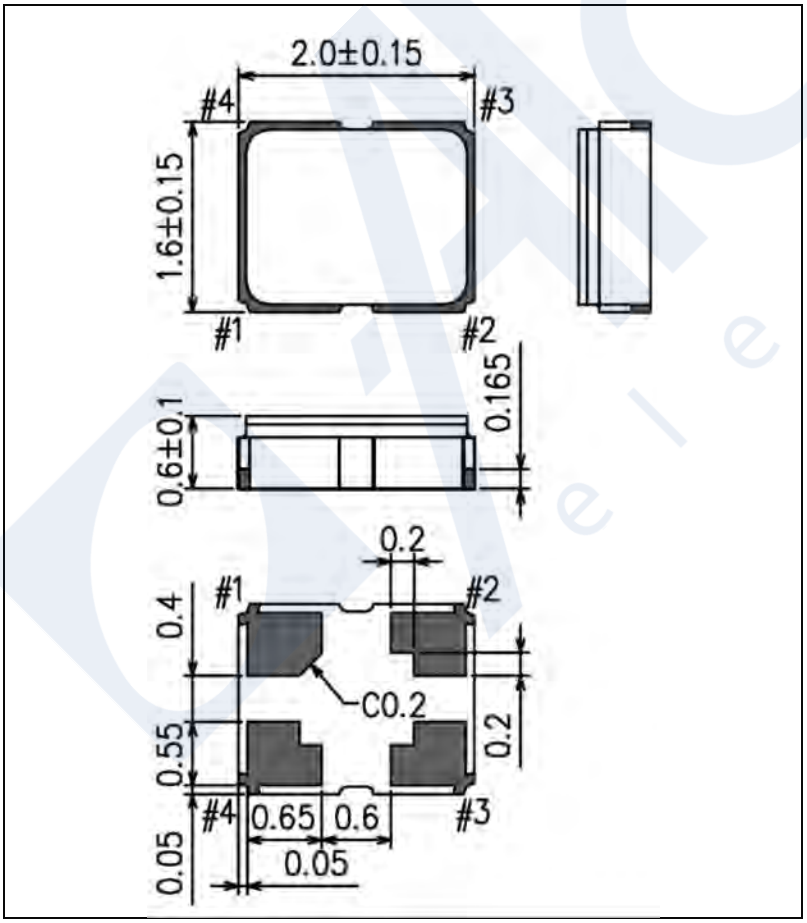
①Model ②Package type (CJ: 2.0 mm × 1.6 mm)
③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance ⑥Operating temperature
⑦Function ⑧Rise/Fall time

⑤Frequency tolerance / ⑥Operating temperature	
BH	±15 × 10^{-6} / -40 °C to +105 °C
DJ	±25 x 10^{-6} / -40 °C to +125 °C

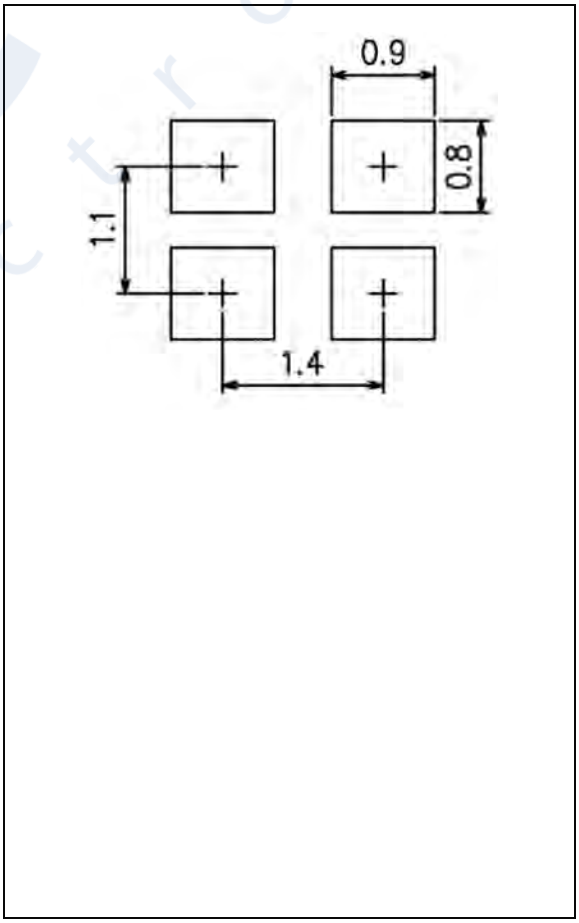
⑦Function	
P	Output Enable (OE) / Active High
S	Standby ($\overline{ST}$) / Active High
Q	Output Enable ($\overline{OE}$) / Active Low
T	Standby (ST) / Active Low

⑧Rise/Fall time	
A	Default
B	Faster
C	Fast
D	Slow
E	Slower

External dimensions (Unit: mm)



Footprint (Recommended) (Unit: mm)



■Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS

SG-8018 series

- Frequency range : 0.67 MHz to 170 MHz (1 ppm Step)
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance : ±50 ppm (-40 ºC to +105 ºC)
  Including frequency aging(+25 ºC, 10 years)
- PLL technology to enable short lead time
- Available field oscillator programmer “SG-Writer II”

Product Number
SG-8018CG: X1G005601xxxx00
SG-8018CE: X1G005591xxxx00
SG-8018CB: X1G005581xxxx00
SG-8018CA: X1G005571xxxx00

CG 2.5 × 2.0 mm | CE 3.2 × 2.5 mm | CB 5.0 × 3.2 mm | CA 7.0 × 5.0 mm

Specifications (characteristics)

Item	Symbol	Specifications				Conditions/Remarks	
Supply voltage	V_{CC}	1.80 V Typ.		2.50 V Typ.	3.30 V Typ.	-	
		1.62 V to 1.98 V	1.98 V to 2.20 V	2.20 V to 2.80 V	2.70 V to 3.63 V		
Output frequency range	f_O	0.67 MHz to 170 MHz					
Storage temperature	T_stg	-40 °C to +125 °C				Storage as single product.	
Operating temperature	T_use	-40 °C to +105 °C				-	
Frequency tolerance*1	f_tol	J: ±50 × 10^{-6}				T_use = -40 °C to +105 °C	
Current consumption	I_{CC}	3.2 mA Max.	3.3 mA Max.	3.4 mA Max.	3.5 mA Max.	T_use = +105 °C	No load, f_O = 20 MHz
		2.7 mA Typ.		2.9 mA Typ.	3.0 mA Typ.	T_use = +25 °C	
		5.5 mA Max.	5.8 mA Max.	6.7 mA Max.	8.1 mA Max.	T_use = +105 °C	No load, f_O = 170 MHz
		4.7 mA Typ.		5.7 mA Typ.	6.8 mA Typ.	T_use = +25 °C	
Output disable current	I_dis	3.2 mA Max.	3.2 mA Max.	3.3 mA Max.	3.5 mA Max.	OE = GND, f_O = 170 MHz	
Standby current	I_std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	$\overline{ST}$ = GND
		0.3 µA Typ.	0.4 µA Typ.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C	
Symmetry	SYM	45 % to 55 %				50 % V_{CC} Level	
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.				I_{OH}/I_{OL} Conditions [mA]	
	V_{OL}	10 % V_{CC} Max.				*A: 1.62 V to 1.98 V, *B: 1.98 V to 2.20 V, *C: 2.20 V to 2.80 V, *D: 2.70 V to 3.63 V	
Output load condition	L_CMOS	15 pF Max.				-	
Input voltage	V_{IH}	70 % V_{CC} Min.				OE or $\overline{ST}$	
	V_{IL}	30 % V_{CC} Max.					
Rise time /Fall time	Default	tr/tf	3.0 ns Max.			f_O > 40 MHz	20 % - 80 % V_{CC}, L_CMOS = 15 pF
			6.0 ns Max.			f_O ≤ 40 MHz	
	Fast		3.0 ns Max.			f_O = 0.67 MHz to 170 MHz	
	Slow		10.0 ns Max.			f_O = 0.67 MHz to 20 MHz	
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.				Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC}	
Output enable time (OE)	tsta_oe	1 µs Max.				Measured from the time OE pin crosses 70 % V_{CC}	
Output enable time (ST)	tsta_st	3 ms Max.				Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC}	
Start-up time	t_str	3 ms Max.				Measured from the time V_{CC} reaches its rated minimum value, 1.62 V	
Frequency aging	f_age	This is included in frequency tolerance specification.				+25 °C, 10 years	

I_{OH}/I_{OL} Conditions					
Rise/Fall time	V_{CC}	*A	*B	*C	*D
Default (f_O > 40 MHz), Fast	I_{OH}	-2.5	-3.5	-4.0	-5.0
	I_{OL}	2.5	3.5	4.0	5.0
Default (f_O ≤ 40 MHz)	I_{OH}	-1.5	-2.0	-2.5	-3.0
	I_{OL}	1.5	2.0	2.5	3.0
Slow	I_{OH}	-1.0	-1.5	-2.0	-2.5
	I_{OL}	1.0	1.5	2.0	2.5

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 10 years).

Pin description

Pin	Name	I/O type	Function	
1	OE	Input	Output enable	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), only output driver is disabled.
	$\overline{ST}$	Input	Standby	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground	
3	OUT	Output	Clock output	
4	V_{CC}	Power	Power supply	

*2 Please do not use the OE/$\overline{ST}$ terminal in the open state.

Product Name

SG-8018CG 25.000000MHz T J H P A
① ② ③ ④⑤⑥⑦⑧

①Model ②Package type ③Frequency
④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance (J: ±50 × 10^{-6})
⑥Operating temperature (H: -40 °C to +105 °C)
⑦Function ⑧Rise/Fall time

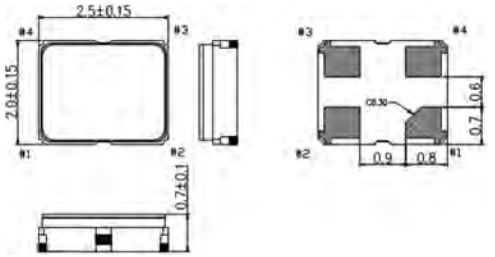
②Package type	
CG	2.5 mm × 2.0 mm
CE	3.2 mm × 2.5 mm
CB	5.0 mm × 3.2 mm
CA	7.0 mm × 5.0 mm

⑦Function	
P	Output enable
S	Standby

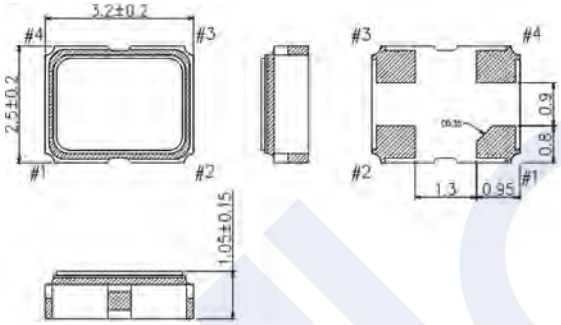
⑧Rise time/Fall time	
A	Default
B	Fast
C	Slow

External dimensions (Unit: mm)

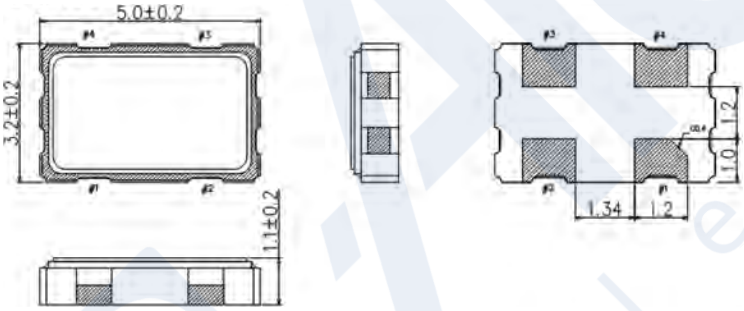
SG-8018CG



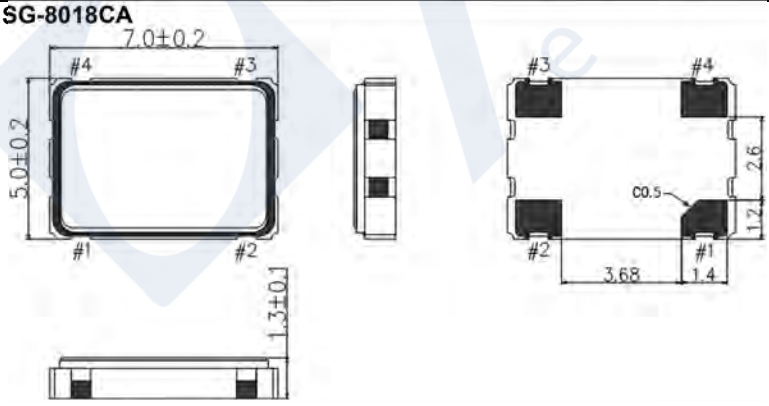
SG-8018CE



SG-8018CB

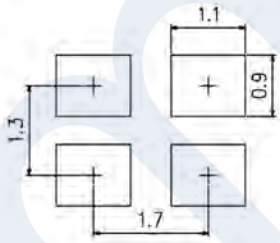


SG-8018CA

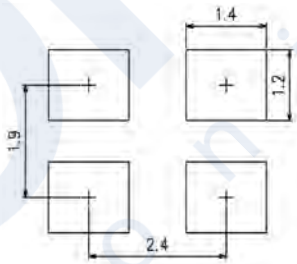


Footprint (Recommended) (Unit: mm)

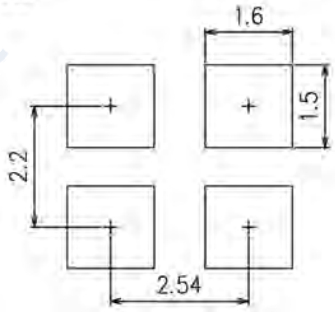
SG-8018CG



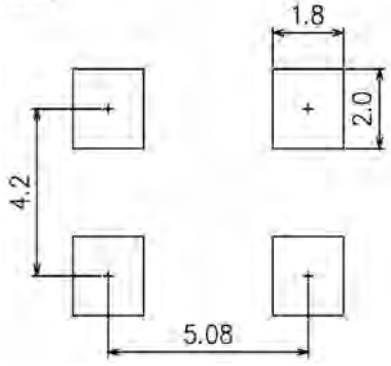
SG-8018CE



SG-8018CB



SG-8018CA



■Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS
SG-8101 series

Product Number
SG-8101CG: X1G005181xxxx00
SG-8101CE: X1G005211xxxx00
SG-8101CB: X1G005201xxxx00
SG-8101CA: X1G005191xxxx00

- Frequency range : 0.67 MHz to 170 MHz (1 × 10^{-6} Step)
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance : ±15 × 10^{-6} (-40 ºC to +85 ºC)
  ±20 × 10^{-6}, ±50 × 10^{-6} (-40 ºC to +105 ºC)
- PLL technology to enable short lead time
- Available field oscillator programmer "SG-Writer II"

CG 2.5 × 2.0 mm | CE 3.2 × 2.5 mm | CB 5.0 × 3.2 mm | CA 7.0 × 5.0 mm

Specifications (characteristics)

Item	Symbol	Specifications				Conditions/Remarks	
Supply voltage	V_{CC}	1.80 V Typ.		2.50 V Typ.	3.30 V Typ.	-	
		1.62 V to 1.98 V	1.98 V to 2.20 V	2.20 V to 2.80 V	2.70 V to 3.63 V		
Output frequency range	f_O	0.67 MHz to 170 MHz					
Storage temperature	T_stg	-40 °C to +125 °C				Storage as single product.	
Operating temperature	T_use	-40 °C to +85 °C				-	
		-40 °C to +105 °C					
Frequency tolerance*1	f_tol	B: ±15 × 10^{-6}				T_use = -40 ºC to +85 °C	
		C: ±20 × 10^{-6}				T_use = -40 ºC to +105 °C	
		J: ±50 × 10^{-6}				T_use = -40 ºC to +105 °C	
Current consumption	I_{CC}	3.2 mA Max.	3.3 mA Max.	3.4 mA Max.	3.5 mA Max.	T_use = +105 °C	No load, f_O = 20 MHz
		2.7 mA Typ.		2.9 mA Typ.	3.0 mA Typ.	T_use = +25 °C	
		5.5 mA Max.	5.8 mA Max.	6.7 mA Max.	8.1 mA Max.	T_use = +105 °C	No load, f_O = 170 MHz
		4.7 mA Typ.		5.7 mA Typ.	6.8 mA Typ.	T_use = +25 °C	
Output disable current	I_dis	3.2 mA Max.	3.2 mA Max.	3.3 mA Max.	3.5 mA Max.	OE = GND, f_O = 170 MHz	
Standby current	I_std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	$\overline{ST}$ = GND
		0.3 µA Typ.	0.4 µA Typ.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C	
Symmetry	SYM	45 % to 55 %				50 % V_{CC} Level	
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.				[mA]	
	V_{OL}	10 % V_{CC} Max.					

Rise/Fall time		V_{CC}	*A	*B	*C	*D
Default (f_O > 40 MHz), Fast		I_{OH}	-2.5	-3.5	-4.0	-5.0
		I_{OL}	2.5	3.5	4.0	5.0
Default (f_O ≤ 40 MHz)		I_{OH}	-1.5	-2.0	-2.5	-3.0
		I_{OL}	1.5	2.0	2.5	3.0
Slow		I_{OH}	-1.0	-1.5	-2.0	-2.5
		I_{OL}	1.0	1.5	2.0	2.5

*A: 1.62 V to 1.98 V, *B: 1.98 V to 2.20 V,
*C: 2.20 V to 2.80 V, *D: 2.70 V to 3.63 V

Output load condition		L_CMOS	15 pF Max.	-
Input voltage		V_{IH}	70 % V_{CC} Min.	OE or $\overline{ST}$
		V_{IL}	30 % V_{CC} Max.	
Rise time /Fall time	Default	tr/tf	3.0 ns Max.	f_O > 40 MHz; 20 % - 80 % V_{CC}, L_CMOS = 15 pF
			6.0 ns Max.	f_O ≤ 40 MHz
	Fast		3.0 ns Max.	f_O = 0.67 MHz to 170 MHz
	Slow		10.0 ns Max.	f_O = 0.67 MHz to 20 MHz
Output disable time (OE) Output disable time (ST)		tstp_oe tstp_st	1 µs Max.	Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC}
Output enable time (OE)		tsta_oe	1 µs Max.	Measured from the time OE pin crosses 70 % V_{CC}
Output enable time (ST)		tsta_st	3 ms Max.	Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC}
Start-up time		t_str	3 ms Max.	Measured from the time V_{CC} reaches its rated minimum value, 1.62 V
Frequency aging		f_age	This is included in frequency tolerance specification.	+25 °C, first year

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 1 year).

Pin description

Pin	Name	I/O type	Function	
1	OE	Input	Output enable	High*2: Specified frequency output from OUT pin
				Low: Out pin is low (weak pull down), only output driver is disabled.
	$\overline{ST}$	Input	Standby	High*2: Specified frequency output from OUT pin
				Low: Out pin is low (weak pull down), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground	
3	OUT	Output	Clock output	
4	V_{CC}	Power	Power supply	

*2 Please do not use the OE/$\overline{ST}$ terminal in the open state.

Product Name

SG-8101CG 25.000000MHz TCHPA
① ② ③ ④⑤⑥⑦⑧

①Model ②Package type
③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance ⑥Operating temperature
⑦Function ⑧Rise/Fall time

②Package type	
CG	2.5 mm × 2.0 mm
CE	3.2 mm × 2.5 mm
CB	5.0 mm × 3.2 mm
CA	7.0 mm × 5.0 mm

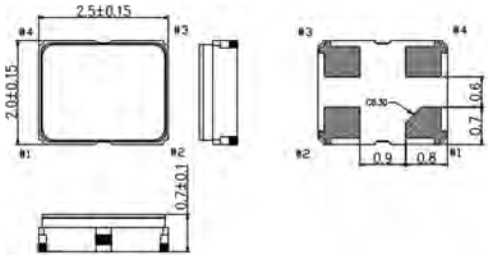
⑤Frequency tolerance / ⑥Operating temperature	
BG	±15 × 10^{-6} / -40 °C to +85 °C
CH	±20 × 10^{-6} / -40 °C to +105 °C
JH	±50 × 10^{-6} / -40 °C to +105 °C

⑦Function	
P	Output enable
S	Standby

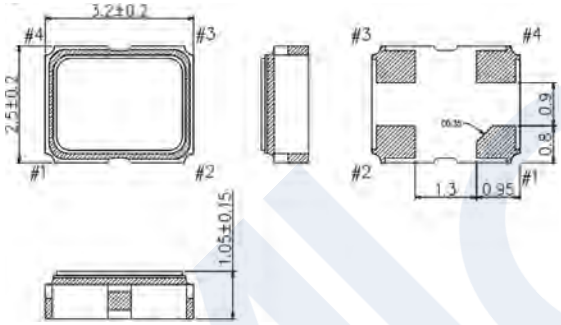
⑧Rise time/Fall time	
A	Default
B	Fast
C	Slow

External dimensions (Unit: mm)

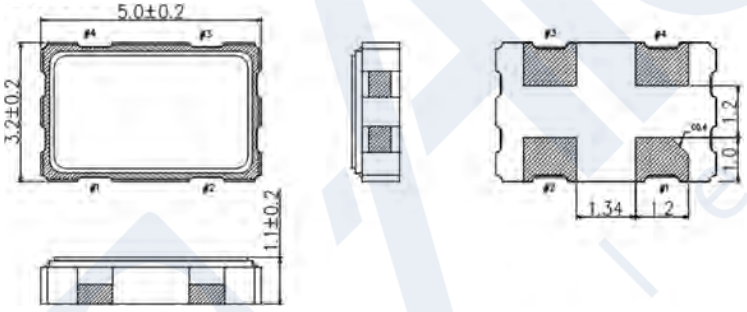
SG-8101CG



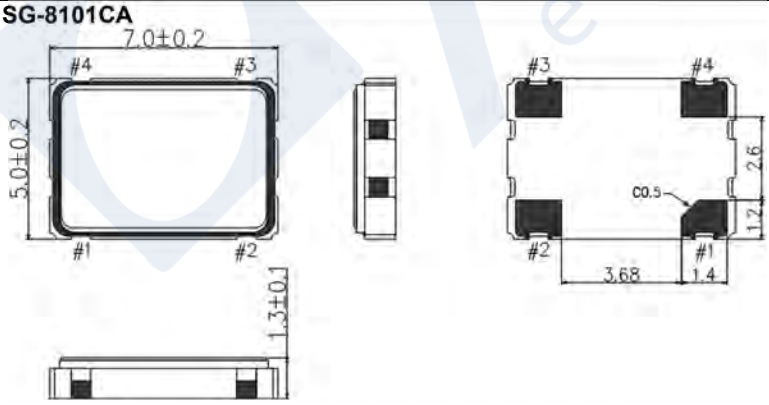
SG-8101CE



SG-8101CB

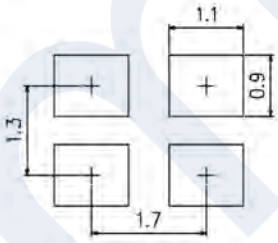


SG-8101CA

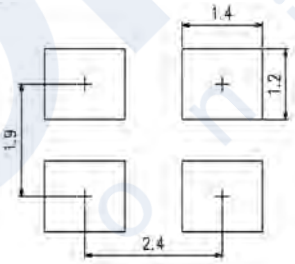


Footprint (Recommended) (Unit: mm)

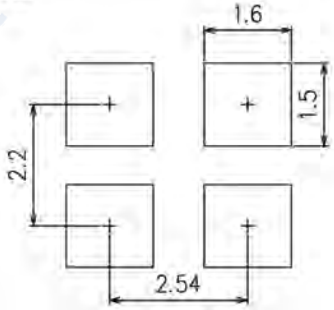
SG-8101CG



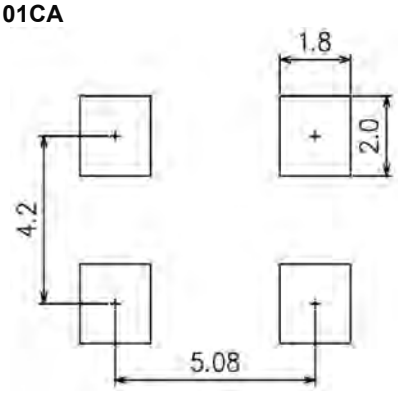
SG-8101CE



SG-8101CB



SG-8101CA



■Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

CRYSTAL OSCILLATOR (Programmable)
SPREAD SPECTRUM
OUTPUT: CMOS

SG-9101 series

Product Number
SG-9101CA: X1G005301xxxx00
SG-9101CB: X1G005311xxxx00
SG-9101CE: X1G005321xxxx00
SG-9101CG: X1G005291xxxx00

- Frequency range : 0.67 MHz to 170 MHz (1 ppm Step)
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Configurable spread spectrum settings:
  2 kinds of spread type, 6 kinds of spread width
  4 kinds of modulation frequency, 3 kinds of spread profile
- PLL technology to enable short lead time
- Available field oscillator programmer "SG-Writer II"

CG 2.5 × 2.0 mm | CE 3.2 × 2.5 mm | CB 5.0 × 3.2 mm | CA 7.0 × 5.0 mm

Specifications (characteristics)

Item	Symbol	Specifications				Conditions/Remarks	
Supply voltage	V_{CC}	1.80 V Typ.		2.50 V Typ.	3.30 V Typ.	-	
		1.62 V to 1.98 V	1.98 V to 2.20 V	2.20 V to 2.80 V	2.70 V to 3.63 V		
Output frequency range	f_O	0.67 MHz to 170 MHz					
Storage temperature	T_stg	-40 °C to +125 °C				Storage as single product.	
Operating temperature	T_use	-40 °C to +85 °C					
		-40 °C to +105 °C					
Frequency tolerance*1	f_tol	±50 × 10^{-6}				Average frequency of 1s gate time.	
Current consumption	I_{CC}	3.4 mA Max.	3.5 mA Max.	3.6 mA Max.	3.7 mA Max.	T_use = +105 °C	No load, f_O = 20 MHz
		2.9 mA Typ.		3.0 mA Typ.	3.2 mA Typ.	T_use = +25 °C	
		5.7 mA Max.	6.0 mA Max.	6.9 mA Max.	8.3 mA Max.	T_use = +105 °C	No load, f_O = 170 MHz
		4.9 mA Typ.		5.9 mA Typ.	7.0 mA Typ.	T_use = +25 °C	
Output disable current	I_dis	3.4 mA Max.	3.4 mA Max.	3.5 mA Max.	3.7 mA Max.	OE = GND, f_O = 170 MHz	
Standby current	I_std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	$\overline{ST}$ = GND
		0.3 µA Typ.	0.4 µA Typ.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C	
Symmetry	SYM	45 % to 55 %				50 % V_{CC} Level	
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.				I_{OH}/I_{OL} Conditions [mA]	
	V_{OL}	10 % V_{CC} Max.				*A : 1.62 V to 1.98 V, *B : 1.98 V to 2.20 V, *C : 2.20 V to 2.80 V, *D : 2.70 V to 3.63 V	
Output load condition	L_CMOS	15 pF Max.				-	
Input voltage	V_{IH}	70 % V_{CC} Min.				OE or $\overline{ST}$	
	V_{IL}	30 % V_{CC} Max.					
Rise time /Fall time	Default	tr/tf	3.0 ns Max.			f_O > 40 MHz	20 % - 80 % V_{CC}, L_CMOS = 15 pF
			6.0 ns Max.			f_O ≤ 40 MHz	
	Fast		3.0 ns Max.			f_O = 0.67 MHz to 170 MHz	
	Slow		10.0 ns Max.			f_O = 0.67 MHz to 20 MHz	
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.				Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC}	
Output enable time (OE)	tsta_oe	1 µs Max.				Measured from the time OE pin crosses 70 % V_{CC}	
Output enable time (ST)	tsta_st	3 ms Max.				Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC}	
Start-up time	t_str	3 ms Max.				Measured from the time V_{CC} reaches its rated minimum value, 1.62 V	
Frequency aging	f_age	This is included in frequency tolerance specification.				+25 °C, first year	

I_{OH}/I_{OL} Conditions					[mA]
Rise/Fall time	Vcc	*A	*B	*C	*D
Default (f_O > 40 MHz), Fast	I_{OH}	-2.5	-3.5	-4.0	-5.0
	I_{OL}	2.5	3.5	4.0	5.0
Default (f_O ≤ 40 MHz)	I_{OH}	-1.5	-2.0	-2.5	-3.0
	I_{OL}	1.5	2.0	2.5	3.0
Slow	I_{OH}	-1.0	-1.5	-2.0	-2.5
	I_{OL}	1.0	1.5	2.0	2.5

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 1 year).

Pin description

Pin	Name	I/O type	Function	
1	OE	Input	Output enable	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), only output driver is disabled.
	$\overline{ST}$	Input	Standby	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground	
3	OUT	Output	Clock output	
4	V_{CC}	Power	Power supply	

*2 Please do not use the OE/$\overline{ST}$ terminal in the open state.

Product Name

SG-9101CG 170.000000MHz C 20 P H A A A
① ② ③ ④⑤⑥⑦⑧⑨⑩

①Model ②Package type ③Frequency
④Spread type ⑤Spread width
⑥Function ⑦Operating temperature
⑧Modulation frequency ⑨Spread profile
⑩Rise/Fall time

②Package type	
CG	2.5 mm × 2.0 mm
CE	3.2 mm × 2.5 mm
CB	5.0 mm × 3.2 mm
CA	7.0 mm × 5.0 mm

④Spread type	
C	Center spread
D	Down spread

⑤Spread width	Center spread	Down spread
02	±0.25 %	
05	±0.5 %	-0.5 %
07	±0.75 %	
10	±1.0 %	-1.0 %
15	±1.5 %	-1.5 %
20	±2.0 %	-2.0 %
30		-3.0 %
40		-4.0 %

⑥Function	
P	Output enable
S	Standby

⑦Operating temperature	
G	-40 °C to +85 °C
H	-40 °C to +105 °C

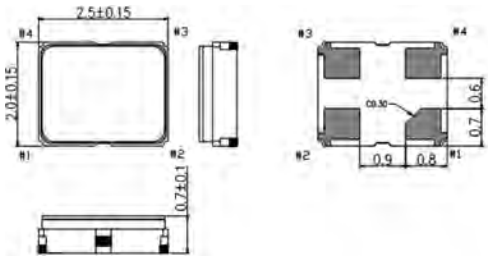
⑧Modulation frequency	
A	25.4 kHz (Default)
B	12.7 kHz
C	8.5 kHz
D	6.3 kHz

⑨Spread profile	
A	Hershey-kiss (Default)
B	Sine-wave
C	Triangle

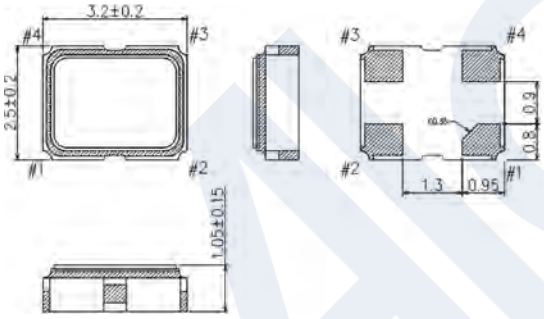
⑩Rise/Fall time	
A	Default
B	Fast
C	Slow

External dimensions (Unit: mm)

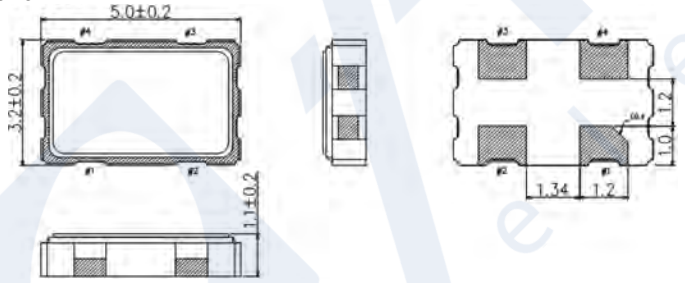
SG-9101CG



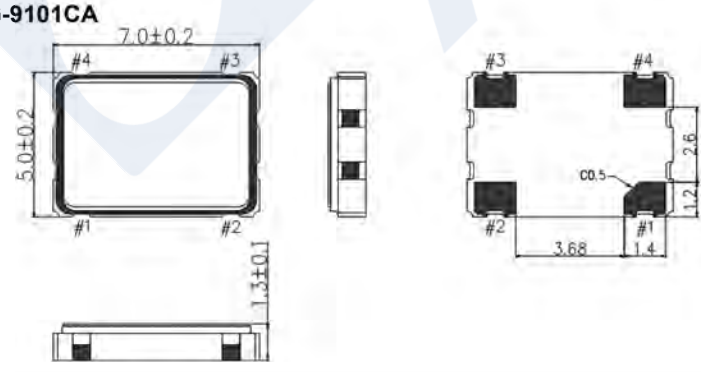
SG-9101CE



SG-9101CB

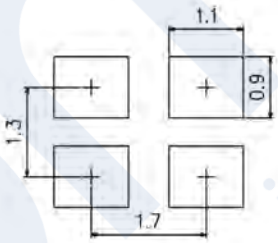


SG-9101CA

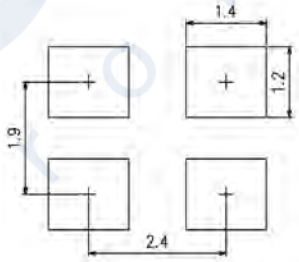


Footprint (Recommended) (Unit: mm)

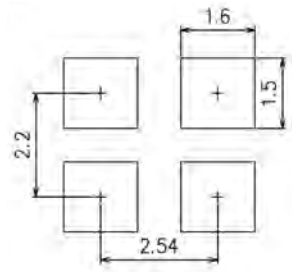
SG-9101CG



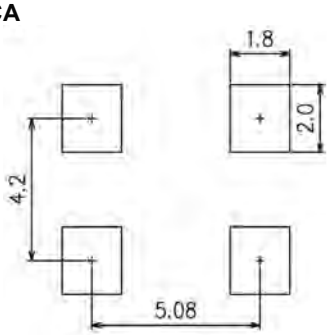
SG-9101CE



SG-9101CB



SG-9101CA



■Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.