CRYSTAL OSCILLATOR (SPXO)

OUTPUT : CMOS

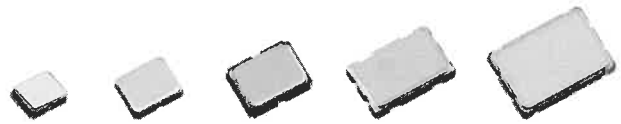
Pb Free

RoHS Compliant

Product Number (please contact us)
SG2016CAN: X1G004801xxxx00
SG-210STF: X1G004171xxxx00
SG3225CAN: X1G005961xxxx15
SG5032CAN: X1G004451xxxx00
SG7050CAN: X1G004481xxxx00

SG2016 / 3225 / 5032 / 7050CAN
SG-210STF

- Frequency : 20 standard frequencies
- Supply voltage : 1.8 V to 3.3 V Typ.
- Function : Standby($\overline{ST}$)
- Operating temperature : -40 °C to +105 °C



SG2016CAN (2.0 x 1.6 mm) | SG-210STF (2.5 x 2.0 mm) | SG3225CAN (3.2 x 2.5 mm) | SG5032CAN (5.0 x 3.2 mm) | SG7050CAN (7.0 x 5.0 mm)

Specifications (characteristics)

Item	Symbol	Specifications			Conditions / Remarks
Output frequency	fo	4 MHz, 8 MHz, 10 MHz, 12 MHz, 12.288 MHz, 14.7456 MHz, 16 MHz, 20 MHz, 24 MHz, 24.576 MHz, 25 MHz, 26 MHz, 27 MHz, 32 MHz, 33.33 MHz, 33.3333 MHz, 40 MHz, 48 MHz, 50 MHz, 72 MHz			
Supply voltage	Vcc	1.60 V to 3.63 V			4 MHz ≤ fo ≤ 50 MHz, T_use = +105 °C Max. (Refer to Figure 1)
		1.71 V to 3.63 V			fo = 72 MHz, T_use = +85 °C Max. (Refer to Figure 1)
		2.25 V to 3.63 V			fo = 72 MHz, T_use = +105 °C Max. (Refer to Figure 1)
Storage temperature	T_stg	-55 °C to +125 °C			SG2016CAN, SG3225CAN
		-40 °C to +125 °C			All others
Operating temperature	T_use	-20 °C to +70 °C, -40 °C to +85 °C, -40 °C to +105 °C			See of figure *1
Frequency tolerance	f_tol	±25 × 10^{-6}			-20 °C to +70 °C
		±50 × 10^{-6}			-40 °C to +85 °C, -40 °C to +105 °C
Current consumption	Icc	Vcc = 1.8 V ± 10 %	Vcc = 2.5 V ± 10 %	Vcc = 3.3 V ± 10 %	
		1.5 mA Max.	1.6 mA Max.	1.8 mA Max.	No load condition, 4 MHz ≤ fo ≤ 20 MHz
		1.8 mA Max.	2.0 mA Max.	2.2 mA Max.	No load condition, 20 MHz < fo ≤ 40 MHz
		2.1 mA Max.	2.4 mA Max.	2.6 mA Max.	No load condition, 40 MHz < fo ≤ 50 MHz
		2.4 mA Max.	2.8 mA Max.	3.0 mA Max.	No load condition, fo = 72 MHz
Stand-by current	I_std	2.1 µA Max.	2.5 µA Max.	2.7 µA Max.	$\overline{ST}$ =GND
Symmetry	SYM	45 % to 55 %			50 % Vcc level, L_CMOS ≤ 15 pF
Output voltage	VOH	90 % Vcc Min.			1.8 V ± 10 %: IOH -1.5 mA, IOL 1.5 mA; 2.5 V ± 10 %: IOH -3 mA, IOL 3 mA; 3.3 V ± 10 %: IOH -4 mA, IOL 4 mA
	VOL	10 % Vcc Max.			
	VOH-2	Vcc - 0.4 V Min.			1.8 V±10 %: IOH -3 mA, IOL 3 mA; 2.5 V±10 %: IOH -4 mA, IOL 4 mA; 3.3 V±10 %: IOH -6 mA, IOL 6 mA
	VOL-2	0.4 V Max.			
Output load condition (CMOS)	L_CMOS	15 pF Max.			
Input voltage	VIH	80 % Vcc Min.			$\overline{ST}$ terminal
	VIL	20 % Vcc Max.			
Rise time and Fall time	tr / tf	3 ns Max. 3.5 ns Max. (@1.8 V±10 %)			20 % Vcc to 80 % Vcc level, L_CMOS = 15 pF
Start-up time	t_str	3 ms Max.			T = 0 at 90 % Vcc
Frequency aging	f_age	±3 × 10^{-6} / year Max.			+25 °C, First year

[Model : SG2016 / 3225 / 5032 / 7050CAN]

Product name (Standard form): SG2016 C AN 25.000000MHz T J H A
① ② ③ ④⑤⑥⑦

①Model ②Output(C: CMOS) ③Frequency ④Supply voltage
⑤Frequency tolerance ⑥Operating temperature range
⑦Internal identification code("A" is default)

④Supply voltage *See Figure 1	
T	1.8 V to 3.3 V Typ.
K	2.5 V to 3.3 V Typ.

⑤Frequency tolerance / ⑥Operating temperature range	
DB*	±25 × 10^{-6} / -20 °C to +70 °C
JG	±50 × 10^{-6} / -40 °C to +85 °C
JH	±50 × 10^{-6} / -40 °C to +105 °C

* Please refer to Product number list on Full Data Sheet for available frequencies

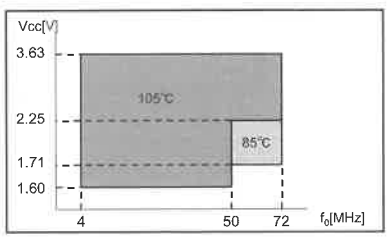


Figure 1 : The upper limit of Operating temperature and the related conditions

Please note that Supply voltage range (Vcc) depends on Output frequency (fo) and upper limit of Operationg temperature (T_use Max.).

[Model : SG-210STF]

Product name (Standard form): SG-210 S T F 25.000000MHz Y
① ②③ ④ ⑤

①Model ②Function(S:Standby) ③Supply voltage
④Frequency ⑤Frequency tolerance

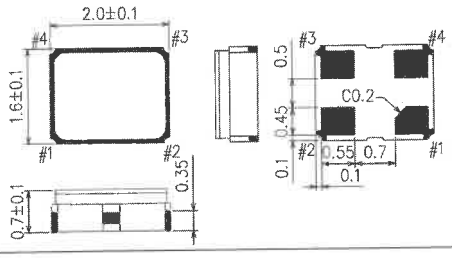
③Supply voltage *See Figure 1	
T	1.8 V to 3.3 V Typ.

⑤Frequency tolerance	
S*	±25 × 10^{-6} / -20 °C to +70 °C
L	±50 × 10^{-6} / -40 °C to +85 °C
Y	±50 × 10^{-6} / -40 °C to +105 °C

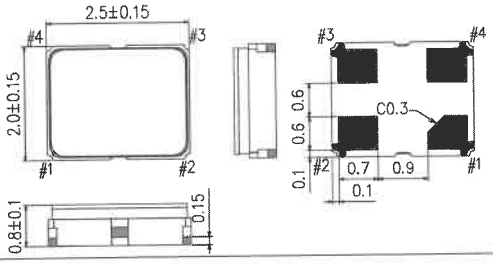
* Please refer to Product number list on Full Data Sheet for available frequencies

External dimensions (Unit:mm)

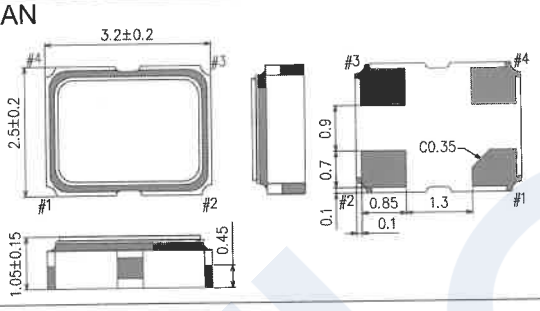
SG2016CAN



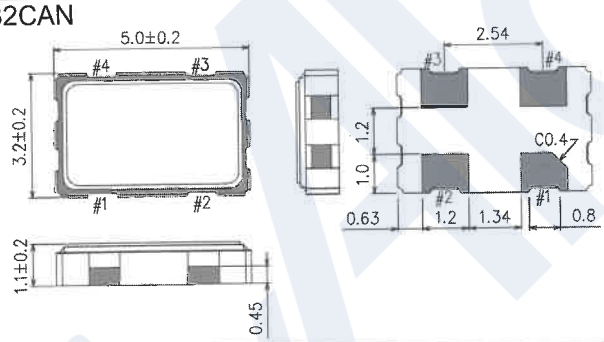
SG-210STF



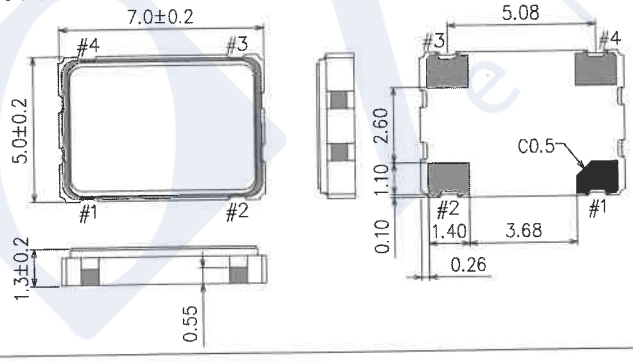
SG3225CAN



SG5032CAN

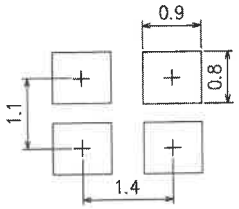


SG7050CAN

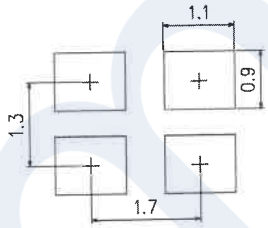


Footprint (Recommended) (Unit:mm)

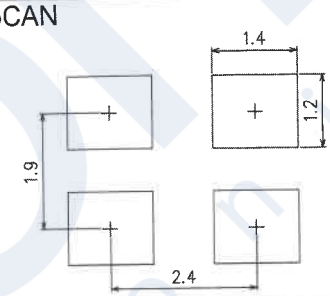
SG2016CAN



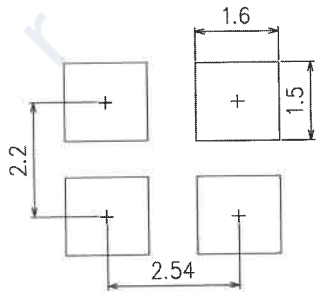
SG-210STF



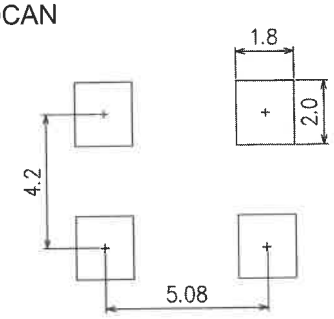
SG3225CAN



SG5032CAN



SG7050CAN



Pin Map

Pin	Connection	Function
1	$\overline{ST}$	$\overline{ST}$ terminal $\overline{ST}$ function: HIGH or "open" → Oscillator circuit: Oscillation → Output: Specified frequency: Enable $\overline{ST}$ function: LOW → Oscillator circuit: Oscillation stop → Output: High impedance: Disable
2	GND	Ground
3	OUT	Clock output
4	V_{CC}	Power supply

■**Notes:** To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS

SG-8200CJ

Product Number
X1G006211xxxx16

- Frequency range : 1.2 MHz to 170 MHz
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance, operating temperature:
  ±50 × 10^{-6} (-40 °C to +125 °C)
- External dimensions : 2.0 × 1.6 × 0.6 (mm)
- PLL technology to enable setting any output frequency

Specifications (characteristics)

Item	Symbol	Specifications			Conditions/Remarks
Supply voltage	V_{CC}	1.80 V Typ.	2.50 V Typ.	3.30 V Typ.	
		1.62 V to 1.98 V	2.25 V to 2.75 V	2.97 V to 3.63 V	
Output frequency range	f_O	1.2 MHz to 170 MHz			
Storage temperature	T_stg	-55 °C to +125 °C			Storage as single product.
Operating temperature	T_use	J: -40 °C to +125 °C			
Frequency tolerance*1	f_tol	J: ±50 × 10^{-6}			T_use = -40 °C to +125 °C
Current consumption	I_{CC}	5.2 mA Typ.	5.4 mA Typ.	5.6 mA Typ.	1.2 MHz ≤ f_O ≤ 25 MHz; No load, Rise/Fall time: Default
		7.0 mA Max.	7.2 mA Max.	7.5 mA Max.	
		5.4 mA Typ.	5.7 mA Typ.	6.1 mA Typ.	25 MHz < f_O ≤ 50 MHz
		7.3 mA Max.	7.6 mA Max.	8.1 mA Max.	
		5.7 mA Typ.	6.3 mA Typ.	7.0 mA Typ.	50 MHz < f_O ≤ 75 MHz
		7.7 mA Max.	8.2 mA Max.	9.1 mA Max.	
		6.2 mA Typ.	6.9 mA Typ.	7.9 mA Typ.	75 MHz < f_O ≤ 100 MHz
		8.2 mA Max.	9.1 mA Max.	10.4 mA Max.	
		6.9 mA Typ.	7.9 mA Typ.	9.1 mA Typ.	100 MHz < f_O ≤ 125 MHz
		9.4 mA Max.	10.7 mA Max.	12.4 mA Max.	
		7.8 mA Typ.	9.2 mA Typ.	11.2 mA Typ.	125 MHz < f_O ≤ 170 MHz
		10.4 mA Max.	12.4 mA Max.	15.0 mA Max.	
Output disable current	I_dis	5.0 mA Typ.	5.0 mA Typ.	5.1 mA Typ.	OE = GND (Active High) $\overline{OE}$ = V_{CC} (Active Low)
		7.2 mA Max.	7.3 mA Max.	7.4 mA Max.	
Standby current	I_std	0.3 µA Typ.	0.3 µA Typ.	0.5 µA Typ.	$\overline{ST}$ = GND (Active High) ST = V_{CC} (Active Low)
		15.0 µA Max.	15.0 µA Max.	15.0 µA Max.	
Symmetry	SYM	45 % to 55 %			50 % V_{CC} Level, L_CMOS ≤ 15 pF
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.			Rise/Fall time: Default 'A' Option*2 / Other Options; I_{OH} / I_{OL} fo > 125 MHz / B: Faster / -2.0 mA / 2.0 mA 75 MHz < fo ≤ 125 MHz / C: Fast / -1.0 mA / 1.0 mA 50 MHz < fo ≤ 75 MHz / D: Slow / -0.5 mA / 0.5 mA fo ≤ 50 MHz / E: Slower / -0.2 mA / 0.2 mA
	V_{OL}	10 % V_{CC} Max.			
Output load condition	L_CMOS	15 pF Max.			
Input voltage	V_{IH}	70 % V_{CC} Min.			Pin 1
	V_{IL}	30 % V_{CC} Max.			
Rise/Fall time	tr/tf	-			Default 'A' Option*2 / Other Options; 20 % - 80 % V_{CC}, L_CMOS = 15 pF fo > 125 MHz / B: Faster
		2.0 ns Max.			75 MHz < fo ≤ 125 MHz / C: Fast
		2.5 ns Max.			50 MHz < fo ≤ 75 MHz / D: Slow
		4.0 ns Max.			fo ≤ 50 MHz / E: Slower
		6.0 ns Max.			
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.			Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC} or measured from the time $\overline{OE}$ or ST pin crosses 70 % V_{CC}
Output enable time (OE)	tsta_oe	100 ns + 2 clock cycle Max.			Measured from the time OE pin crosses 70 % V_{CC} or measured from the time $\overline{OE}$ pin crosses 30 % V_{CC}
Output enable time (ST)	tsta_st	3 ms Max.			Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC} or measured from the time ST pin crosses 30 % V_{CC}
Start-up time	t_str	3 ms Max.			Measured from the time V_{CC} reaches its rated minimum value, 1.62 V
Phase Jitter	t_{PJ}	1.2 ps Typ.			fo = 25 MHz, Offset frequency: 12 kHz to 5 MHz
		1.2 ps Typ.			fo = 50 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 75 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 100 MHz, Offset frequency: 12 kHz to 20 MHz
		1.1 ps Typ.			fo = 125 MHz, Offset frequency: 12 kHz to 20 MHz
		1.4 ps Typ.			fo = 150 MHz, Offset frequency: 12 kHz to 20 MHz
		1.5 ps Typ.			fo = 170 MHz, Offset frequency: 12 kHz to 20 MHz
Frequency aging	f_age	This is included in frequency tolerance specification.			+25 °C, first year

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, load drift and aging (+25 °C, 1 year).
*2 Default 'A' Rise/Fall time and I_{OH}/I_{OL} are dependent on programmed frequency.

Pin description

Pin	Name	I/O type	Function		
1	OE	Input	Output Enable (Active High)	High[*1] or Open:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	$\overline{ST}$	Input	Standby (Active High)	High[*1 *2]:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
	$\overline{OE}$	Input	Output Enable (Active Low)	Low[*3] or Open:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	ST	Input	Standby (Active Low)	Low[*3 *4]:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground		
3	OUT	Output	Clock output		
4	V_{CC}	Power	Power supply		

*1 If fixing it at High, please connect to V_{CC} directly.
*2 If necessary to use Open, please select Output Enable (Active High) function.
*3 If fixing it at Low, please connect to GND directly.
*4 If necessary to use Open, please select Output Enable (Active Low) function.

Product Name

SG-8200CJ 170.000000MHz T J J P A
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

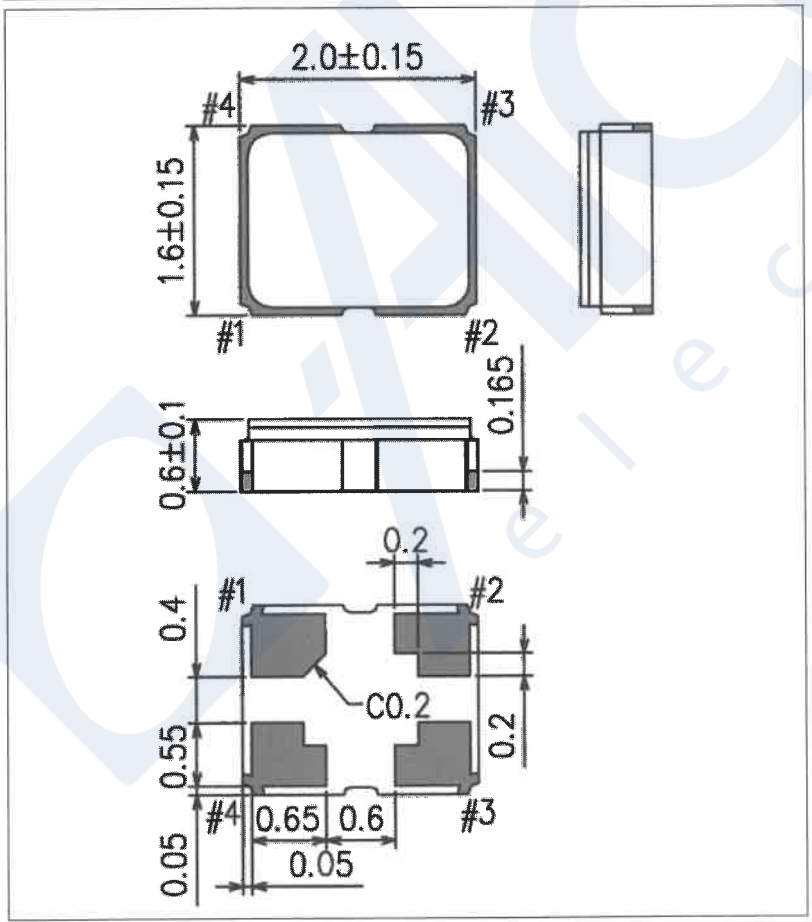
①Model ②Package type (CJ: 2.0 mm × 1.6 mm)
③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance ⑥Operating temperature
⑦Function ⑧Rise/Fall time

⑤Frequency tolerance / ⑥Operating temperature	
JJ	±50 x 10^{-6} / -40 °C to +125 °C

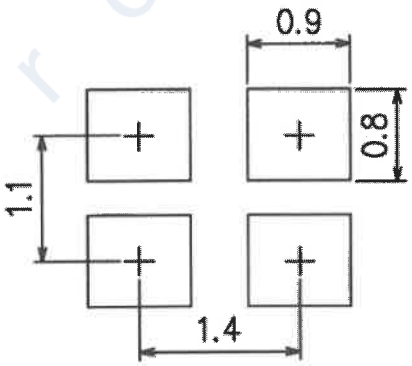
⑦Function	
P	Output Enable (OE) / Active High
S	Standby ($\overline{ST}$) / Active High
Q	Output Enable ($\overline{OE}$) / Active Low
T	Standby (ST) / Active Low

⑧Rise/Fall time	
A	Default
B	Faster
C	Fast
D	Slow
E	Slower

External dimensions (Unit: mm)



Footprint (Recommended) (Unit: mm)



■Notes:
In order to achieve optimum jitter performance, the 0.01 µF to 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS

SG-8201CJ

Product Number
X1G005981xxxx16

- Frequency range : 1.2 MHz to 170 MHz
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance, operating temperature:
  ±15 × 10^{-6} (-40 °C to +105 °C)
  ±25 × 10^{-6} (-40 °C to +125 °C)
- External dimensions : 2.0 × 1.6 × 0.6 (mm)
- PLL technology to enable setting any output frequency

Specifications (characteristics)

Item	Symbol	Specifications			Conditions/Remarks
Supply voltage	V_{CC}	1.80 V Typ.	2.50 V Typ.	3.30 V Typ.	
		1.62 V to 1.98 V	2.25 V to 2.75 V	2.97 V to 3.63 V	
Output frequency range	f_O	1.2 MHz to 170 MHz			
Storage temperature	T_stg	-55 °C to +125 °C			Storage as single product.
Operating temperature	T_use	H: -40 °C to +105 °C			
		J: -40 °C to +125 °C			
Frequency tolerance*1	f_tol	B: ±15 × 10^{-6}			T_use = -40 °C to +105 °C
		D: ±25 × 10^{-6}			T_use = -40 °C to +125 °C
Current consumption	I_{CC}	5.2 mA Typ.	5.4 mA Typ.	5.6 mA Typ.	1.2 MHz ≤ f_O ≤ 25 MHz; No load, Rise/Fall time: Default
		7.0 mA Max.	7.2 mA Max.	7.5 mA Max.	
		5.4 mA Typ.	5.7 mA Typ.	6.1 mA Typ.	25 MHz < f_O ≤ 50 MHz
		7.3 mA Max.	7.6 mA Max.	8.1 mA Max.	
		5.7 mA Typ.	6.3 mA Typ.	7.0 mA Typ.	50 MHz < f_O ≤ 75 MHz
		7.7 mA Max.	8.2 mA Max.	9.1 mA Max.	
		6.2 mA Typ.	6.9 mA Typ.	7.9 mA Typ.	75 MHz < f_O ≤ 100 MHz
		8.2 mA Max.	9.1 mA Max.	10.4 mA Max.	
		6.9 mA Typ.	7.9 mA Typ.	9.1 mA Typ.	100 MHz < f_O ≤ 125 MHz
		9.4 mA Max.	10.7 mA Max.	12.4 mA Max.	
		7.8 mA Typ.	9.2 mA Typ.	11.2 mA Typ.	125 MHz < f_O ≤ 170 MHz
		10.4 mA Max.	12.4 mA Max.	15.0 mA Max.	
Output disable current	I_dis	5.0 mA Typ.	5.0 mA Typ.	5.1 mA Typ.	OE = GND (Active High) $\overline{OE}$ = V_{CC} (Active Low)
		7.2 mA Max.	7.3 mA Max.	7.4 mA Max.	
Standby current	I_std	0.3 µA Typ.	0.3 µA Typ.	0.5 µA Typ.	$\overline{ST}$ = GND (Active High) ST = V_{CC} (Active Low)
		15.0 µA Max.	15.0 µA Max.	15.0 µA Max.	
Symmetry	SYM	45 % to 55 %			50 % V_{CC} Level, L_CMOS ≤ 15 pF
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.			Rise/Fall time: Default 'A' Option*2 / Other Options; I_{OH} / I_{OL} fo > 125 MHz / B: Faster / -2.0 mA / 2.0 mA 75 MHz < fo ≤ 125 MHz / C: Fast / -1.0 mA / 1.0 mA 50 MHz < fo ≤ 75 MHz / D: Slow / -0.5 mA / 0.5 mA fo ≤ 50 MHz / E: Slower / -0.2 mA / 0.2 mA
	V_{OL}	10 % V_{CC} Max.			
Output load condition	L_CMOS	15 pF Max.			
Input voltage	V_{IH}	70 % V_{CC} Min.			Pin 1
	V_{IL}	30 % V_{CC} Max.			
Rise/Fall time	tr/tf	-			Default 'A' Option*2 / Other Options; 20 % - 80 % V_{CC}, L_CMOS = 15 pF fo > 125 MHz / B: Faster
		2.0 ns Max.			75 MHz < fo ≤ 125 MHz / C: Fast
		2.5 ns Max.			50 MHz < fo ≤ 75 MHz / D: Slow
		4.0 ns Max.			fo ≤ 50 MHz / E: Slower
		6.0 ns Max.			
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.			Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC} or measured from the time $\overline{OE}$ or ST pin crosses 70 % V_{CC}
Output enable time (OE)	tsta_oe	100 ns + 2 clock cycle Max.			Measured from the time OE pin crosses 70 % V_{CC} or measured from the time $\overline{OE}$ pin crosses 30 % V_{CC}
Output enable time (ST)	tsta_st	3 ms Max.			Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC} or measured from the time ST pin crosses 30 % V_{CC}
Start-up time	t_str	3 ms Max.			Measured from the time V_{CC} reaches its rated minimum value, 1.62 V
Phase Jitter	t_{PJ}	1.2 ps Typ.			fo = 25 MHz, Offset frequency: 12 kHz to 5 MHz
		1.2 ps Typ.			fo = 50 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 75 MHz, Offset frequency: 12 kHz to 20 MHz
		1.2 ps Typ.			fo = 100 MHz, Offset frequency: 12 kHz to 20 MHz
		1.1 ps Typ.			fo = 125 MHz, Offset frequency: 12 kHz to 20 MHz
		1.4 ps Typ.			fo = 150 MHz, Offset frequency: 12 kHz to 20 MHz
		1.5 ps Typ.			fo = 170 MHz, Offset frequency: 12 kHz to 20 MHz
Frequency aging	f_age	This is included in frequency tolerance specification.			+25 °C, first year

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, load drift and aging (+25 °C, 1 year).
*2 Default 'A' Rise/Fall time and I_{OH}/I_{OL} are dependent on programmed frequency.

Pin description

Pin	Name	I/O type	Function		
1	OE	Input	Output Enable (Active High)	High[*1] or Open:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	$\overline{ST}$	Input	Standby (Active High)	High[*1 *2]:	Specified frequency output from OUT pin
				Low:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
	$\overline{OE}$	Input	Output Enable (Active Low)	Low[*3] or Open:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	ST	Input	Standby (Active Low)	Low[*3 *4]:	Specified frequency output from OUT pin
				High:	OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground		
3	OUT	Output	Clock output		
4	V_{CC}	Power	Power supply		

*1 If fixing it at High, please connect to V_{CC} directly.
*2 If necessary to use Open, please select Output Enable (Active High) function.
*3 If fixing it at Low, please connect to GND directly.
*4 If necessary to use Open, please select Output Enable (Active Low) function.

Product Name

SG-8201CJ 170.000000MHz T D J P A
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

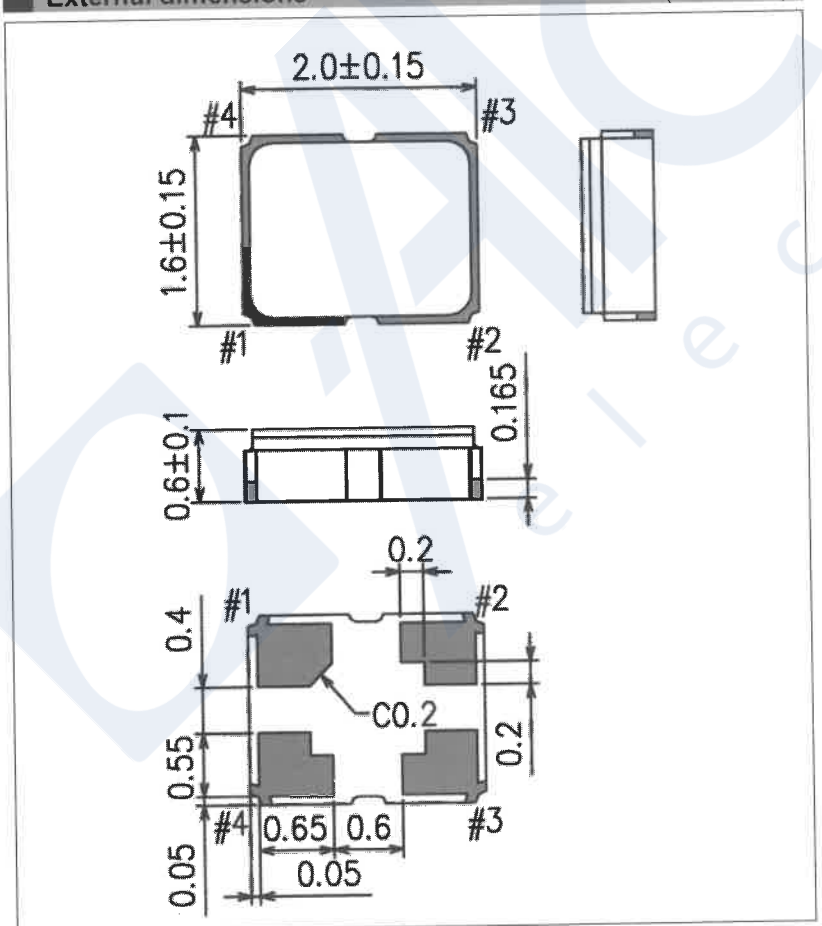
①Model ②Package type (CJ: 2.0 mm × 1.6 mm)
③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance ⑥Operating temperature
⑦Function ⑧Rise/Fall time

⑤Frequency tolerance / ⑥Operating temperature	
BH	±15 × 10^{-6} / -40 °C to +105 °C
DJ	±25 x 10^{-6} / -40 °C to +125 °C

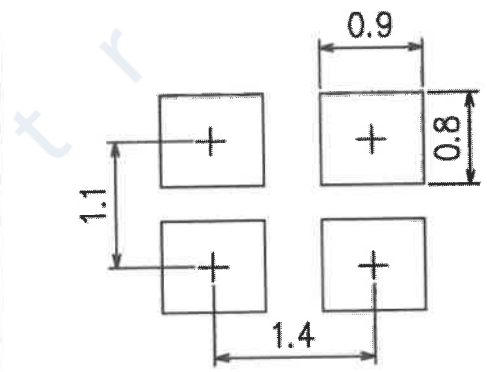
⑦Function	
P	Output Enable (OE) / Active High
S	Standby ($\overline{ST}$) / Active High
Q	Output Enable ($\overline{OE}$) / Active Low
T	Standby (ST) / Active Low

⑧Rise/Fall time	
A	Default
B	Faster
C	Fast
D	Slow
E	Slower

External dimensions (Unit: mm)



Footprint (Recommended) (Unit: mm)



Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS
SG-8018 series

Pb Free
RoHS Compliant

Product Number
SG-8018CG: X1G005601xxxx00
SG-8018CE: X1G005591xxxx00
SG-8018CB: X1G005581xxxx00
SG-8018CA: X1G005571xxxx00

- Frequency range : 0.67 MHz to 170 MHz (1 ppm Step)
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance : ±50 ppm (-40 °C to +105 °C)
  Including frequency aging(+25 °C, 10 years)
- PLL technology to enable short lead time
- Available field oscillator programmer "SG-Writer II"

CG 2.5 × 2.0 mm | CE 3.2 × 2.5 mm | CB 5.0 × 3.2 mm | CA 7.0 × 5.0 mm

Specifications (characteristics)

Item	Symbol	Specifications				Conditions/Remarks	
Supply voltage	V_{CC}	1.80 V Typ.		2.50 V Typ.	3.30 V Typ.	-	
		1.62 V to 1.98 V	1.98 V to 2.20 V	2.20 V to 2.80 V	2.70 V to 3.63 V		
Output frequency range	f_O	0.67 MHz to 170 MHz					
Storage temperature	T_stg	-40 °C to +125 °C				Storage as single product.	
Operating temperature	T_use	-40 °C to +105 °C[*1]				-	
Frequency tolerance[*1]	f_tol	J: ±50 × 10^{-6}				T_use = -40 °C to +105 °C	
Current consumption	I_{CC}	3.2 mA Max.	3.3 mA Max.	3.4 mA Max.	3.5 mA Max.	T_use = +105 °C	No load, f_O = 20 MHz
		2.7 mA Typ.		2.9 mA Typ.	3.0 mA Typ.	T_use = +25 °C	
		5.5 mA Max.	5.8 mA Max.	6.7 mA Max.	8.1 mA Max.	T_use = +105 °C	No load, f_O = 170 MHz
		4.7 mA Typ.		5.7 mA Typ.	6.8 mA Typ.	T_use = +25 °C	
Output disable current	I_dis	3.2 mA Max.	3.2 mA Max.	3.3 mA Max.	3.5 mA Max.	OE = GND, f_O = 170 MHz	
Standby current	I_std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	$\overline{ST}$ = GND
		0.3 µA Typ.	0.4 µA Typ.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C	
Symmetry	SYM	45 % to 55 %				50 % V_{CC} Level	
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.				I_{OH}/I_{OL} Conditions [mA]	
	V_{OL}	10 % V_{CC} Max.				Rise/Fall time / V_{CC} / *A / *B / *C / *D Default (f_O > 40 MHz), Fast: I_{OH} -2.5 -3.5 -4.0 -5.0; I_{OL} 2.5 3.5 4.0 5.0 Default (f_O ≤ 40 MHz): I_{OH} -1.5 -2.0 -2.5 -3.0; I_{OL} 1.5 2.0 2.5 3.0 Slow: I_{OH} -1.0 -1.5 -2.0 -2.5; I_{OL} 1.0 1.5 2.0 2.5 *A: 1.62 V to 1.98 V, *B: 1.98 V to 2.20 V, *C: 2.20 V to 2.80 V, *D: 2.70 V to 3.63 V	
Output load condition	L_CMOS	15 pF Max.				-	
Input voltage	V_{IH}	70 % V_{CC} Min.				OE or $\overline{ST}$	
	V_{IL}	30 % V_{CC} Max.					
Rise time /Fall time	Default	tr/tf	3.0 ns Max.			f_O > 40 MHz	20 % - 80 % V_{CC}, L_CMOS = 15 pF
			6.0 ns Max.			f_O ≤ 40 MHz	
	Fast		3.0 ns Max.			f_O = 0.67 MHz to 170 MHz	
	Slow		10.0 ns Max.			f_O = 0.67 MHz to 20 MHz	
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.				Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC}	
Output enable time (OE)	tsta_oe	1 µs Max.				Measured from the time OE pin crosses 70 % V_{CC}	
Output enable time (ST)	tsta_st	3 ms Max.				Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC}	
Start-up time	t_str	3 ms Max.				Measured from the time V_{CC} reaches its rated minimum value, 1.62 V	
Frequency aging	f_age	This is included in frequency tolerance specification.				+25 °C, 10 years	

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 10 years).

Pin description

Pin	Name	I/O type	Function	
1	OE	Input	Output enable	High[*2]: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), only output driver is disabled.
	$\overline{ST}$	Input	Standby	High[*2]: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground	
3	OUT	Output	Clock output	
4	V_{CC}	Power	Power supply	

*2 Please do not use the OE/$\overline{ST}$ terminal in the open state.

Product Name

SG-8018CG 25.000000MHz T J H P A
① ② ③ ④⑤⑥⑦⑧

①Model ②Package type ③Frequency
④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance (J: ±50 × 10^{-6})
⑥Operating temperature (H: -40 °C to +105 °C)
⑦Function ⑧Rise/Fall time

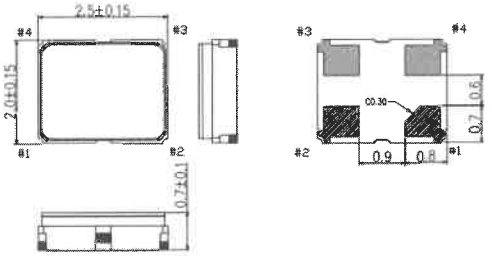
②Package type	
CG	2.5 mm × 2.0 mm
CE	3.2 mm × 2.5 mm
CB	5.0 mm × 3.2 mm
CA	7.0 mm × 5.0 mm

⑦Function	
P	Output enable
S	Standby

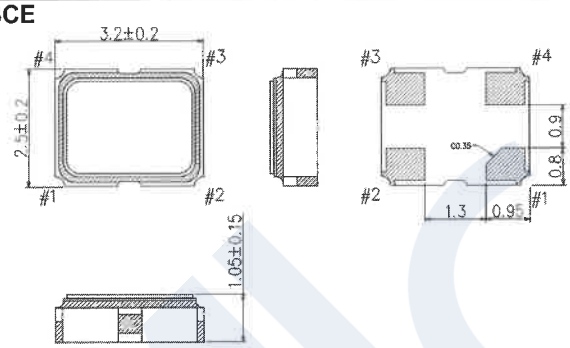
⑧Rise time/Fall time	
A	Default
B	Fast
C	Slow

External dimensions (Unit: mm)

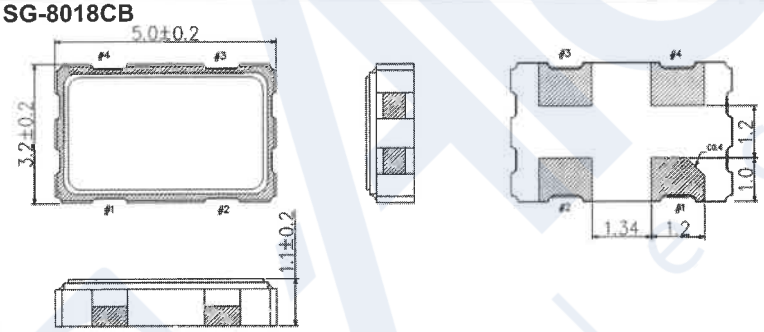
SG-8018CG



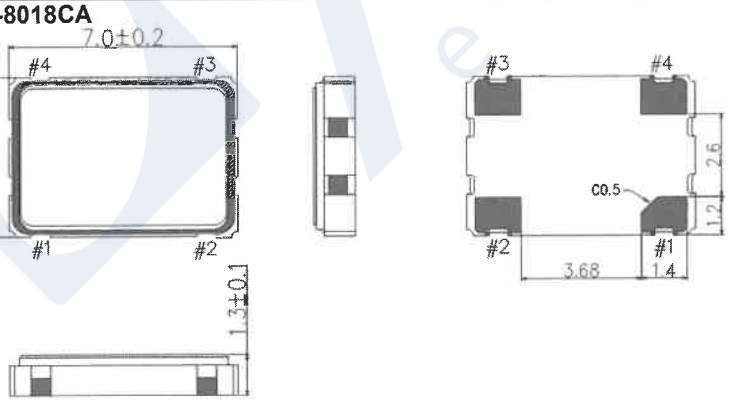
SG-8018CE



SG-8018CB

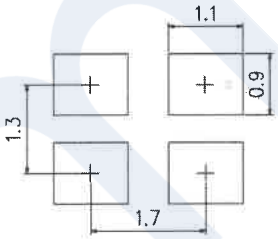


SG-8018CA

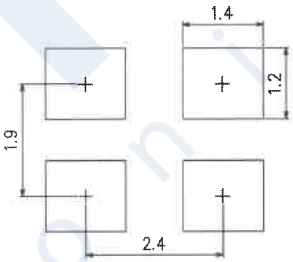


Footprint (Recommended) (Unit: mm)

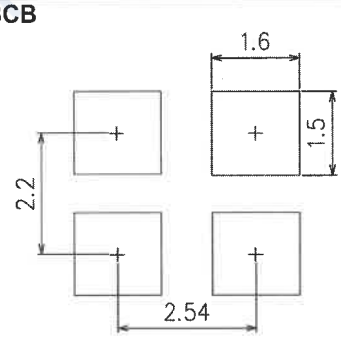
SG-8018CG



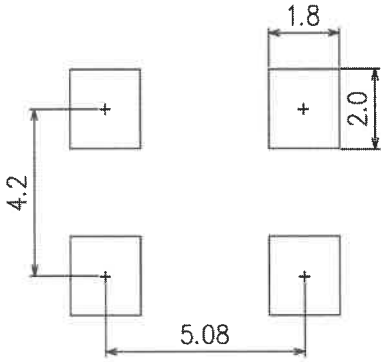
SG-8018CE



SG-8018CB



SG-8018CA



Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

SEIKO EPSON CORPORATION

CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS
SG-8101 series

Pb Free / RoHS Compliant

Product Number
SG-8101CG: X1G005181xxxx00
SG-8101CE: X1G005211xxxx00
SG-8101CB: X1G005201xxxx00
SG-8101CA: X1G005191xxxx00

- Frequency range : 0.67 MHz to 170 MHz (1 × 10^{-6} Step)
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Frequency tolerance : ±15 × 10^{-6} (-40 °C to +85 °C)
  ±20 × 10^{-6}, ±50 × 10^{-6} (-40 °C to +105 °C)
- PLL technology to enable short lead time
- Available field oscillator programmer "SG-Writer II"

CG 2.5 × 2.0 mm | CE 3.2 × 2.5 mm | CB 5.0 × 3.2 mm | CA 7.0 × 5.0 mm

Specifications (characteristics)

Item	Symbol	Specifications				Conditions/Remarks	
Supply voltage	V_{CC}	1.80 V Typ.		2.50 V Typ.	3.30 V Typ.	-	
		1.62 V to 1.98 V	1.98 V to 2.20 V	2.20 V to 2.80 V	2.70 V to 3.63 V		
Output frequency range	f_O	0.67 MHz to 170 MHz					
Storage temperature	T_stg	-40 °C to +125 °C				Storage as single product.	
Operating temperature	T_use	-40 °C to +85 °C				-	
		-40 °C to +105 °C					
Frequency tolerance*1	f_tol	B: ±15 × 10^{-6}				T_use = -40 °C to +85 °C	
		C: ±20 × 10^{-6}				T_use = -40 °C to +105 °C	
		J: ±50 × 10^{-6}				T_use = -40 °C to +105 °C	
Current consumption	I_{CC}	3.2 mA Max.	3.3 mA Max.	3.4 mA Max.	3.5 mA Max.	T_use = +105 °C	No load, f_O = 20 MHz
		2.7 mA Typ.		2.9 mA Typ.	3.0 mA Typ.	T_use = +25 °C	
		5.5 mA Max.	5.8 mA Max.	6.7 mA Max.	8.1 mA Max.	T_use = +105 °C	No load, f_O = 170 MHz
		4.7 mA Typ.		5.7 mA Typ.	6.8 mA Typ.	T_use = +25 °C	
Output disable current	I_dis	3.2 mA Max.	3.2 mA Max.	3.3 mA Max.	3.5 mA Max.	OE = GND, f_O = 170 MHz	
Standby current	I_std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	$\overline{ST}$ = GND
		0.3 µA Typ.	0.4 µA Typ.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C	
Symmetry	SYM	45 % to 55 %				50 % V_{CC} Level	
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.				[mA]	

Rise/Fall time		*A	*B	*C	*D
Default (f_O > 40 MHz), Fast	I_{OH}	-2.5	-3.5	-4.0	-5.0
	I_{OL}	2.5	3.5	4.0	5.0
Default (f_O ≤ 40 MHz)	I_{OH}	-1.5	-2.0	-2.5	-3.0
	I_{OL}	1.5	2.0	2.5	3.0
Slow	I_{OH}	-1.0	-1.5	-2.0	-2.5
	I_{OL}	1.0	1.5	2.0	2.5

*A: 1.62 V to 1.98 V, *B: 1.98 V to 2.20 V,
*C: 2.20 V to 2.80 V, *D: 2.70 V to 3.63 V

Output voltage (DC characteristics)	V_{OL}	10 % V_{CC} Max.		
Output load condition	L_CMOS	15 pF Max.	-	
Input voltage	V_{IH}	70 % V_{CC} Min.	OE or $\overline{ST}$	
	V_{IL}	30 % V_{CC} Max.		
Rise time /Fall time Default	tr/tf	3.0 ns Max.	f_O > 40 MHz	20 % - 80 % V_{CC}, L_CMOS = 15 pF
Default		6.0 ns Max.	f_O ≤ 40 MHz	
Fast		3.0 ns Max.	f_O = 0.67 MHz to 170 MHz	
Slow		10.0 ns Max.	f_O = 0.67 MHz to 20 MHz	
Output disable time (OE) Output disable time (ST)	tstp_oe tstp_st	1 µs Max.	Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC}	
Output enable time (OE)	tsta_oe	1 µs Max.	Measured from the time OE pin crosses 70 % V_{CC}	
Output enable time (ST)	tsta_st	3 ms Max.	Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC}	
Start-up time	t_str	3 ms Max.	Measured from the time V_{CC} reaches its rated minimum value, 1.62 V	
Frequency aging	f_age	This is included in frequency tolerance specification.	+25 °C, first year	

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 1 year).

Pin description

Pin	Name	I/O type	Function	
1	OE	Input	Output enable	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), only output driver is disabled.
	$\overline{ST}$	Input	Standby	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground	
3	OUT	Output	Clock output	
4	V_{CC}	Power	Power supply	

*2 Please do not use the OE/$\overline{ST}$ terminal in the open state.

Product Name

SG-8101CG 25.000000MHz TCHPA
① ② ③ ④⑤⑥⑦⑧

①Model ②Package type
③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance ⑥Operating temperature
⑦Function ⑧Rise/Fall time

②Package type	
CG	2.5 mm × 2.0 mm
CE	3.2 mm × 2.5 mm
CB	5.0 mm × 3.2 mm
CA	7.0 mm × 5.0 mm

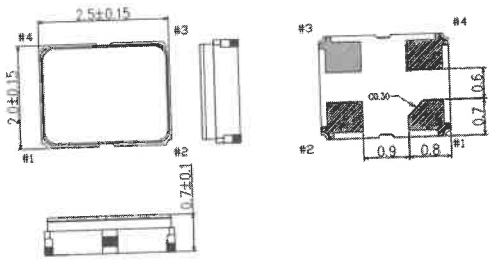
⑤Frequency tolerance / ⑥Operating temperature	
BG	±15 × 10^{-6} / -40 °C to +85 °C
CH	±20 × 10^{-6} / -40 °C to +105 °C
JH	±50 × 10^{-6} / -40 °C to +105 °C

⑦Function	
P	Output enable
S	Standby

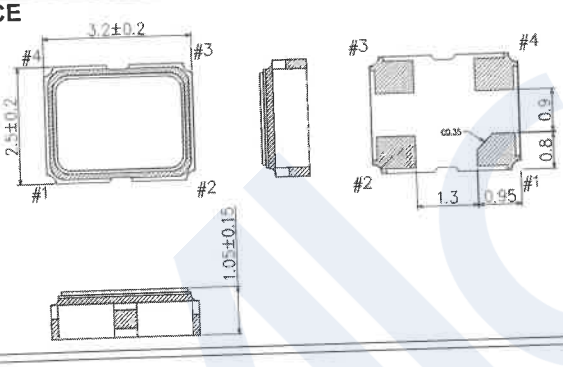
⑧Rise time/Fall time	
A	Default
B	Fast
C	Slow

External dimensions (Unit: mm)

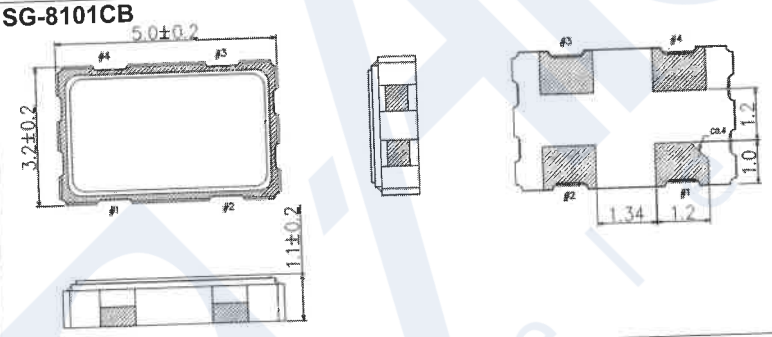
SG-8101CG



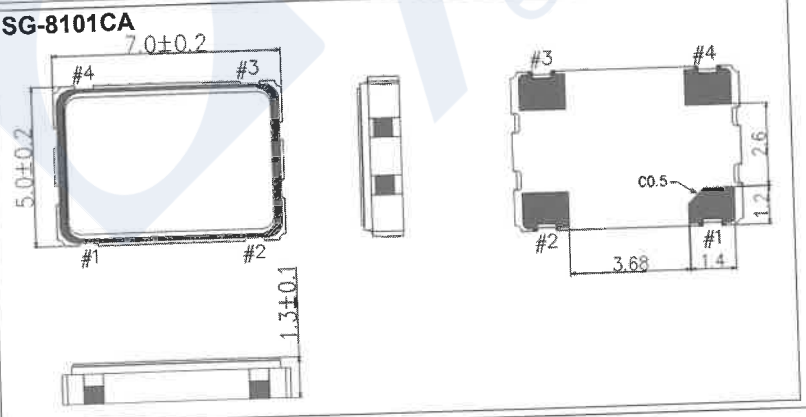
SG-8101CE



SG-8101CB

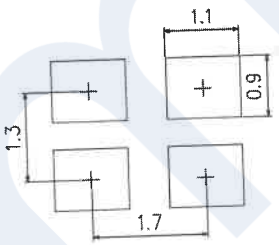


SG-8101CA

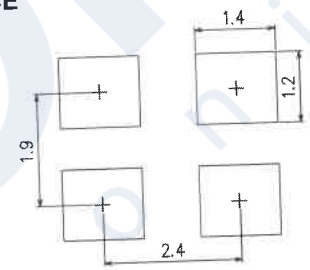


Footprint (Recommended) (Unit: mm)

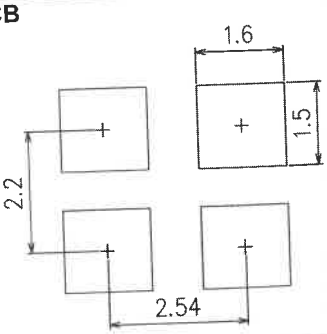
SG-8101CG



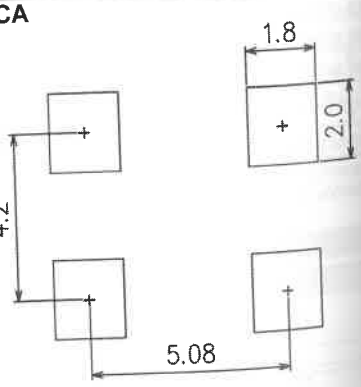
SG-8101CE



SG-8101CB



SG-8101CA



Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

CRYSTAL OSCILLATOR (Programmable)
SPREAD SPECTRUM
OUTPUT: CMOS
SG-9101 series

Pb Free

RoHS Compliant

Product Number
SG-9101CA: X1G005301xxxx00
SG-9101CB: X1G005311xxxx00
SG-9101CE: X1G005321xxxx00
SG-9101CG: X1G005291xxxx00

- Frequency range : 0.67 MHz to 170 MHz (1 ppm Step)
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Configurable spread spectrum settings:
  2 kinds of spread type, 6 kinds of spread width
  4 kinds of modulation frequency, 3 kinds of spread profile
- PLL technology to enable short lead time
- Available field oscillator programmer "SG-Writer II"

CG 2.5 × 2.0 mm | CE 3.2 × 2.5 mm | CB 5.0 × 3.2 mm | CA 7.0 × 5.0 mm

Specifications (characteristics)

Item	Symbol	Specifications				Conditions/Remarks	
Supply voltage	V_{CC}	1.80 V Typ.		2.50 V Typ.	3.30 V Typ.	-	
		1.62 V to 1.98 V	1.98 V to 2.20 V	2.20 V to 2.80 V	2.70 V to 3.63 V		
Output frequency range	f_O	0.67 MHz to 170 MHz					
Storage temperature	T_stg	-40 °C to +125 °C				Storage as single product.	
Operating temperature	T_use	-40 °C to +85 °C					
		-40 °C to +105 °C					
Frequency tolerance*1	f_tol	±50 × 10^{-6}				Average frequency of 1s gate time.	
Current consumption	I_{CC}	3.4 mA Max.	3.5 mA Max.	3.6 mA Max.	3.7 mA Max.	T_use = +105 °C	No load, f_O = 20 MHz
		2.9 mA Typ.		3.0 mA Typ.	3.2 mA Typ.	T_use = +25 °C	
		5.7 mA Max.	6.0 mA Max.	6.9 mA Max.	8.3 mA Max.	T_use = +105 °C	No load, f_O = 170 MHz
		4.9 mA Typ.		5.9 mA Typ.	7.0 mA Typ.	T_use = +25 °C	
Output disable current	I_dis	3.4 mA Max.	3.4 mA Max.	3.5 mA Max.	3.7 mA Max.	OE = GND, f_O = 170 MHz	
Standby current	I_std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	$\overline{ST}$ = GND
		0.3 µA Typ.	0.4 µA Typ.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C	
Symmetry	SYM	45 % to 55 %				50 % V_{CC} Level	
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.				I_{OH}/I_{OL} Conditions [mA]	
	V_{OL}	10 % V_{CC} Max.					

Rise/Fall time	Vcc	*A	*B	*C	*D
Default (f_O > 40 MHz), Fast	I_{OH}	-2.5	-3.5	-4.0	-5.0
	I_{OL}	2.5	3.5	4.0	5.0
Default (f_O ≤ 40 MHz)	I_{OH}	-1.5	-2.0	-2.5	-3.0
	I_{OL}	1.5	2.0	2.5	3.0
Slow	I_{OH}	-1.0	-1.5	-2.0	-2.5
	I_{OL}	1.0	1.5	2.0	2.5

*A : 1.62 V to 1.98 V, *B : 1.98 V to 2.20 V,
*C : 2.20 V to 2.80 V, *D : 2.70 V to 3.63 V

Output load condition		L_CMOS	15 pF Max.	-	
Input voltage		V_{IH}	70 % V_{CC} Min.	OE or $\overline{ST}$	
		V_{IL}	30 % V_{CC} Max.		
Rise time /Fall time	Default	tr/tf	3.0 ns Max.	f_O > 40 MHz	20 % - 80 % V_{CC}, L_CMOS = 15 pF
			6.0 ns Max.	f_O ≤ 40 MHz	
	Fast		3.0 ns Max.	f_O = 0.67 MHz to 170 MHz	
	Slow		10.0 ns Max.	f_O = 0.67 MHz to 20 MHz	
Output disable time (OE) Output disable time (ST)		tstp_oe tstp_st	1 µs Max.	Measured from the time OE or $\overline{ST}$ pin crosses 30 % V_{CC}	
Output enable time (OE)		tsta_oe	1 µs Max.	Measured from the time OE pin crosses 70 % V_{CC}	
Output enable time (ST)		tsta_st	3 ms Max.	Measured from the time $\overline{ST}$ pin crosses 70 % V_{CC}	
Start-up time		t_str	3 ms Max.	Measured from the time V_{CC} reaches its rated minimum value, 1.62 V	
Frequency aging		f_age	This is included in frequency tolerance specification.	+25 °C, first year	

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 1 year).

Pin description

Pin	Name	I/O type	Function	
1	OE	Input	Output enable	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), only output driver is disabled.
	$\overline{ST}$	Input	Standby	High*2: Specified frequency output from OUT pin Low: Out pin is low (weak pull down), Device goes to standby mode. Supply current reduces to the least as I_std.
2	GND	Power	Ground	
3	OUT	Output	Clock output	
4	V_{CC}	Power	Power supply	

*2 Please do not use the OE/$\overline{ST}$ terminal in the open state.

Product Name

SG-9101CG 170.000000MHz C 20 P H A A A
① ② ③ ④⑤⑥⑦⑧⑨⑩

①Model ②Package type ③Frequency
④Spread type ⑤Spread width
⑥Function ⑦Operating temperature
⑧Modulation frequency ⑨Spread profile
⑩Rise/Fall time

②Package type	
CG	2.5 mm × 2.0 mm
CE	3.2 mm × 2.5 mm
CB	5.0 mm × 3.2 mm
CA	7.0 mm × 5.0 mm

④Spread type	
C	Center spread
D	Down spread

⑤Spread width	Center spread	Down spread
02	±0.25 %	
05	±0.5 %	-0.5 %
07	±0.75 %	
10	±1.0 %	-1.0 %
15	±1.5 %	-1.5 %
20	±2.0 %	-2.0 %
30		-3.0 %
40		-4.0 %

⑥Function	
P	Output enable
S	Standby

⑦Operating temperature	
G	-40 °C to +85 °C
H	-40 °C to +105 °C

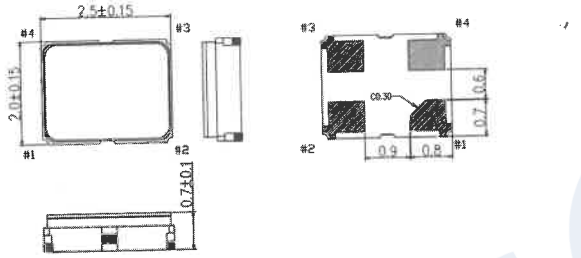
⑧Modulation frequency	
A	25.4 kHz (Default)
B	12.7 kHz
C	8.5 kHz
D	6.3 kHz

⑨Spread profile	
A	Hershey-kiss (Default)
B	Sine-wave
C	Triangle

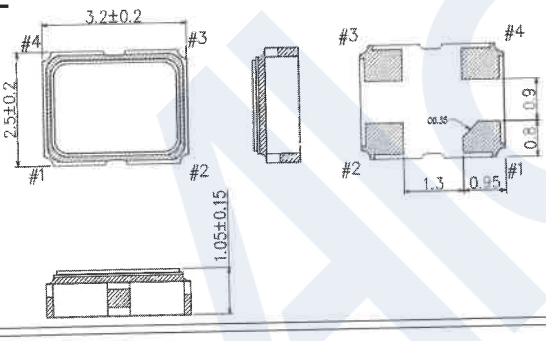
⑩Rise/Fall time	
A	Default
B	Fast
C	Slow

External dimensions (Unit: mm)

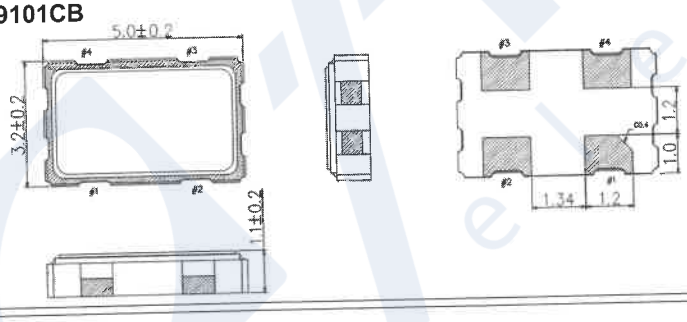
SG-9101CG



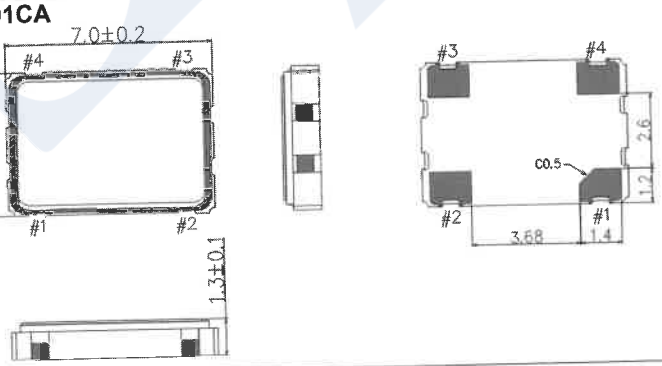
SG-9101CE



SG-9101CB

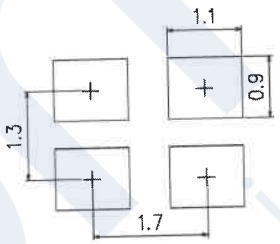


SG-9101CA

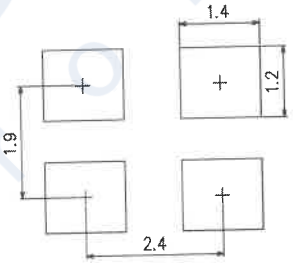


Footprint (Recommended) (Unit: mm)

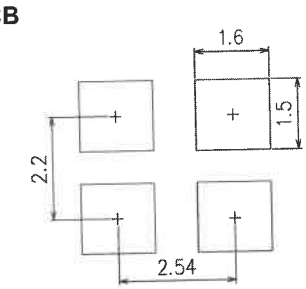
SG-9101CG



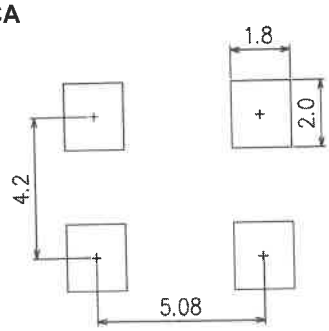
SG-9101CE



SG-9101CB



SG-9101CA

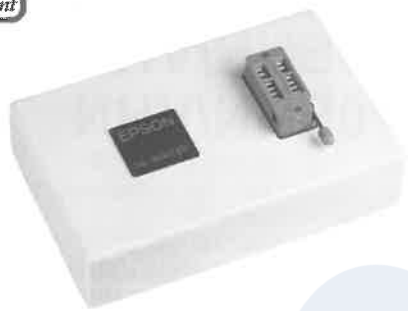


■Notes:
In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

Programming tool for Programmable Crystal Oscillator
SG-Writer II

RoHS Compliant

Product Number
Q91PR20W1102000



- Programming tool for programmable oscillator: SG-8018, SG-8101, SG-9101, SG-8503, SG-8504 and SG-8506 series (Blank sample)
- Able to program required frequency at customer side
- External power supply by USB cable
- Available PC OS: Windows 10, etc
- Small body and easy carry

Main Body Specifications

Name	SG-Writer II for programmable oscillator: SG-8018, SG-8101, SG-9101,-SG-8503, SG-8504 and SG-8506 series
Operating Temperature	+10 °C to +40 °C Writing (+25 °C ±5 °C)
Electric Power Supply	Via USB
Standard Interface	USB 2.0 (mini-B)
Accessories	SG-Writer II, Instruction manual (Documents: English, Japanese)
Software	SG-Writer II

Option
SG-Writer IC socket
*1

Model	Product number
SG-8018CA, SG-8101CA, SG-9101CA	Q91PR10W00021
SG-8018CB, SG-8101CB, SG-9101CB	Q91PR10W00025
SG-8018CE, SG-8101CE, SG-9101CE	Q91PR10W00018
SG-8018CG, SG-8101CG, SG-9101CG	Q91PR10W00024
SG-8503CA	Q91PR10W00026
SG-8504CA	Q91PR10W00027
SG-8506CA	Q91PR10W00028

Option
Blank sample

Model	Product number
SG-8018CA	X1G0055710001
SG-8018CB	X1G0055810001
SG-8018CE	X1G0055910001
SG-8018CG	X1G0056010001
SG-8101CB	X1G0052010001
SG-8101CE	X1G0052110001
SG-8101CG	X1G0051810001
SG-9101CA	X1G0053010001
SG-9101CB	X1G0053110001
SG-9101CE	X1G0053210001
SG-9101CG	X1G0052910001

Model	Product number
SG-8503CA	X1G0050111001
SG-8504CA	X1G0050211001
SG-8506CA	X1G0050311001

*1 If you have IC socket of either SG-8002CA/CE it can use for both SG-8018CA/CE, SG-8101CA/CE and SG- 9101CA/CE.

Recommend PC Specifications (You need to connect the SG-Writer II to a PC when you are writing.)

Available PC OS	Windows 7 (32 bit, 64 bit), Windows Vista (32 bit), Windows XP (32 bit) Windows 10 (32 bit, 64 bit)
Recommend CPU	Over Pentium 4 1.4 GHz or equivalent Processor
Recommend memory Capacity	Windows XP : Over 512 MB Windows Vista, Windows7 32 bit : Over 1 GB Windows 7 64 bit : Over 2 GB Windows 10 : Over 2 GB
Other	USB cable (Type A ↔ mini-B) Need SMD *2 socket when you write SG-8000 SMD products. (Sold separately)

*2 Conventional IC socket for PROM Writer or SG-Writer (the previous model) can be used for SG-Writer II.

Precautions

- The Blank sample of each series can be identified by marking
- The firmware update is required to program SG-8018, SG-8101, SG-9101, SG-8503, SG-8504 and SG-8506 series. For details please contact your supplier.

CRYSTAL OSCILLATOR (SPXO)

OUTPUT : LV-PECL, LVDS

Pb Free
RoHS Compliant

Product Number
SG2016EHN: X1G006141xxxx15
SG2016VHN: X1G006121xxxx15
SG2520EHN: X1G005921xxxx15
SG2520VHN: X1G005941xxxx15

SG2016EHN/VHN
SG2520EHN/VHN

- Frequency range : 25 MHz to 500 MHz
- Supply voltage : 1.8 V Typ. (LVDS only) / 2.5 V Typ. / 3.3 V Typ.
- Frequency tolerance : ±20 × 10^{-6}
- Operating temperature : -40 °C to +85 °C, -40 °C to +105 °C
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Phase jitter : 50 fs Max. (391 MHz < fo ≤ 500 MHz, V_{CC} = 2.5 V, 3.3 V)

SG2016EHN
SG2016VHN
(2.0 × 1.6 × 0.63 mm)

SG2520EHN
SG2520VHN
(2.5 × 2.0 × 0.74 mm)

Specifications (characteristics)

Item	Symbol	Specifications LV-PECL SG2016EHN / SG2520EHN	Specifications LVDS SG2016VHN / SG2520VHN		Conditions / Remarks	
Output frequency range	fo	25 MHz to 500 MHz			Please contact us for available frequencies.	
Supply voltage	V_{CC}	C: 3.3 V ± 5 % D: 2.5 V ± 5 %	, E: 1.8 V ± 5 %			
Storage temperature	T_stg	-55 °C to +125 °C				
Operating temperature	T_use	G: -40 °C to +85 °C, H: -40 °C to +105 °C				
Frequency tolerance	f_tol	C: ±20 × 10^{-6} Max.			Includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient and 10 years aging (+25 °C)	
Current consumption	I_{CC}	60 mA Max.	–		OE or $\overline{ST}$ = V_{CC}, L_ECL = 50 Ω	
		–	25 mA / 30 mA / 25 mA Max.	25 mA / – / 25 mA Max.	25 MHz ≤ fo < 212 MHz	OE or $\overline{ST}$ = V_{CC}, Output option: A / B / C
			28 mA / 35 mA / 28 mA Max.		212 MHz ≤ fo < 392 MHz	
			28 mA / 35 mA / 30 mA Max.		392 MHz ≤ fo ≤ 500 MHz	
Disable current	I_dis	35 mA Max.	20 mA Max.		OE = GND	
Stand-by current	I_std	30 µA Max.			$\overline{ST}$ = GND, T_use Max. = +85 °C	
		60 µA Max.			$\overline{ST}$ = GND, T_use Max. = +105 °C	
Symmetry	SYM	45 % to 55 %			At output crossing point	
Output voltage (LV-PECL)	V_{OH}	V_{CC} - 1.1 V Min.	–		Output option: A, DC characteristic	
	V_{OL}	V_{CC} - 1.5 V Max.				
Differential swing	V_{SW}	0.8 V to 2.0 V	500 mV to 900 mV	500 mV to 900 mV	Output option: A	
		–	800 mV to 1 600 mV	–	Output option: B	
		–	600 mV to 1 200 mV	600 mV to 1 200 mV	Output option: C	
Output voltage (LVDS)	V_{OD}	–	250 mV to 450 mV	250 mV to 450 mV	Output option: A	Differential output voltage, V_{OD1}, V_{OD2}
			400 mV to 800 mV	–	Output option: B	
			300 mV to 600 mV	300 mV to 600 mV	Output option: C	
	dV_{OD}	–	50 mV Max.		dV_{OD} = | V_{OD1} - V_{OD2} |	
	V_{OS}	–	1.15 V to 1.35 V	0.65 V to 0.85 V	Offset voltage, V_{OS1}, V_{OS2}	
	dV_{OS}	–	50 mV Max.		dV_{OS} = | V_{OS1} - V_{OS2} |	
Output load condition	L_ECL	50 Ω	–		Terminated to V_{CC} - 2.0 V	
	L_LVDS	–	100 Ω		Connected between OUT and $\overline{OUT}$	
Input voltage	V_{IH}	70 % V_{CC} Min.			OE or $\overline{ST}$ terminal	
	V_{IL}	30 % V_{CC} Max.				
Rise/Fall times	tr/tf	0.35 ns Max.			LV-PECL: 20 % - 80 % (V_{OH} - V_{OL}) LVDS: 20 % - 80 % differential output peak to peak	
Start-up time	t_str	10 ms Max.			t = 0 at 90 % V_{CC}	
Phase jitter	t_{PJ}	250 fs Max.	250 fs Max.	400 fs Max.	25 MHz ≤ fo < 100 MHz	Offset frequency fo < 50 MHz: 12 kHz to 5 MHz fo ≥ 50 MHz: 12 kHz to 20 MHz
		90 fs Max.	100 fs Max.	130 fs Max.	100 MHz ≤ fo ≤ 156 MHz	
		70 fs Max.	60 fs Max.	70 fs Max.	156 MHz < fo ≤ 212 MHz	
		60 fs Max.	50 fs Max.	60 fs Max.	212 MHz < fo ≤ 391 MHz	
		50 fs Max.			391 MHz < fo ≤ 500 MHz	

Product Name (Standard form)

SG2016 EHN 156.250000MHz C C H P Z A
① ② ③ ④⑤⑥⑦⑧⑨

①Model ②Output (E: LV-PECL, V: LVDS) ③Frequency ④Supply voltage ⑤Frequency tolerance
⑥Operating temperature ⑦Function ⑧Output disable type (Z: High impedance) ⑨Output option

④Supply voltage	
C	3.3 V Typ.
D	2.5 V Typ.
E*	1.8 V Typ.

* "E" is only for SG2016VHN and SG2520VHN

⑤Freq. tolerance	
C	±20 × 10^{-6}

⑥Operating temp.	
G	-40 °C to +85 °C
H	-40 °C to +105 °C

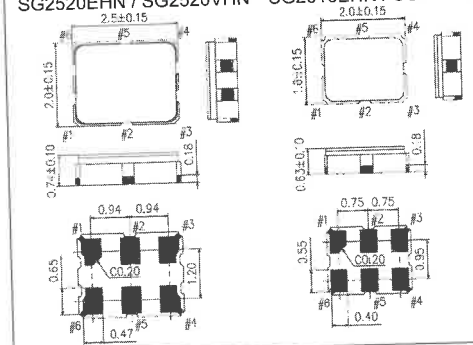
⑦Function	
P	OE
S	$\overline{ST}$

⑨Output option	SG2016EHN / SG2520EHN	SG2016VHN / SG2520VHN
A	Default	V_{OD} = 250 mV to 450 mV
B*	–	V_{OD} = 400 mV to 800 mV
C	–	V_{OD} = 300 mV to 600 mV

*Not available for V_{CC} = 1.8 V Typ.

External dimensions (Unit:mm)

SG2520EHN / SG2520VHN SG2016EHN / SG2016VHN

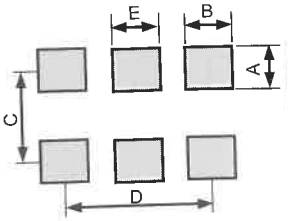


Pin map

Pin	Connection
1	OE or $\overline{ST}$
2	N.C. (Open or V_{CC})
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

Note:
OE or $\overline{ST}$ pin = HIGH or "Open":
Specified frequency output.
OE or $\overline{ST}$ pin = LOW:
Output is high impedance

Footprint (Recommended) (Unit:mm)



	SG2520EHN SG2520VHN	SG2016EHN SG2016VHN
A	0.88	0.85
B	0.76	0.574
C	1.38	1.15
D	1.99	1.564
E	0.63	0.574

In order to achieve optimum jitter performance, it is recommended that 0.1 µF and 10 µF bypass capacitors should be connected between V_{CC} and GND and placed as close to the V_{CC} pin as possible.

CRYSTAL OSCILLATOR (SPXO)
OUTPUT : LV-PECL, LVDS

SG2016EGN/VGN
SG2520EGN/VGN

Product Number
SG2016EGN: X1G006131xxxx15
SG2016VGN: X1G006111xxxx15
SG2520EGN: X1G005881xxxx15
SG2520VGN: X1G005901xxxx15

- Frequency range : 25 MHz to 500 MHz
- Supply voltage : 1.8 V Typ. (LVDS only) / 2.5 V Typ. / 3.3 V Typ.
- Frequency tolerance : ±25 × 10^{-6}, ±50 × 10^{-6}
- Operating temperature : -40 °C to +85 °C, -40 °C to +105 °C
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Phase jitter : 50 fs Max. (391 MHz < fo ≤ 500 MHz, V_{CC} = 2.5 V, 3.3 V)

SG2016EGN
SG2016VGN
(2.0 × 1.6 × 0.63 mm)

SG2520EGN
SG2520VGN
(2.5 × 2.0 × 0.74 mm)

Specifications (characteristics)

Item	Symbol	Specifications			Conditions / Remarks	
		LV-PECL	LVDS			
		SG2016EGN / SG2520EGN	SG2016VGN / SG2520VGN			
Output frequency range	fo	25 MHz to 500 MHz			Please contact us for available frequencies.	
Supply voltage	V_{CC}	C: 3.3 V ± 5 % D: 2.5 V ± 5 %		E: 1.8 V ± 5 %		
Storage temperature	T_stg	-55 °C to +125 °C				
Operating temperature	T_use	G: -40 °C to +85 °C, H: -40 °C to +105 °C				
Frequency tolerance	f_tol	D: ±25 × 10^{-6} Max. J: ±50 × 10^{-6} Max.			Includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient and 10 years aging (+25 °C)	
Current consumption	I_{CC}	60 mA Max.	–		OE or $\overline{ST}$ = V_{CC}, L_ECL = 50 Ω	
		–	25 mA / 30 mA / 25 mA Max.	25 mA / – / 25 mA Max.	25 MHz ≤ fo < 212 MHz	OE or $\overline{ST}$ = V_{CC}, Output option: A / B / C
			28 mA / 35 mA / 28 mA Max.		212 MHz ≤ fo < 392 MHz	
			28 mA / 35 mA / 30 mA Max.		392 MHz ≤ fo ≤ 500 MHz	
Disable current	I_dis	35 mA Max.	20 mA Max.		OE = GND	
Stand-by current	I_std	30 µA Max.			$\overline{ST}$ = GND, T_use Max. = +85 °C	
		60 µA Max.			$\overline{ST}$ = GND, T_use Max. = +105 °C	
Symmetry	SYM	45 % to 55 %			At output crossing point	
Output voltage (LV-PECL)	V_{OH}	V_{CC} - 1.1 V Min.	–		Output option: A, DC characteristic	
	V_{OL}	V_{CC} - 1.5 V Max.				
Differential swing	V_{SW}	0.8 V to 2.0 V	500 mV to 900 mV	500 mV to 900 mV	Output option: A	
		–	800 mV to 1 600 mV	–	Output option: B	
		–	600 mV to 1 200 mV	600 mV to 1 200 mV	Output option: C	
Output voltage (LVDS)	V_{OD}	–	250 mV to 450 mV	250 mV to 450 mV	Output option: A	Differential output voltage, V_{OD1}, V_{OD2}
			400 mV to 800 mV	–	Output option: B	
			300 mV to 600 mV	300 mV to 600 mV	Output option: C	
	dV_{OD}	–	50 mV Max.		dV_{OD} = | V_{OD1} - V_{OD2} |	
	V_{OS}	–	1.15 V to 1.35 V	0.65 V to 0.85 V	Offset voltage, V_{OS1}, V_{OS2}	
	dV_{OS}	–	50 mV Max.		dV_{OS} = | V_{OS1} - V_{OS2} |	
Output load condition	L_ECL	50 Ω	–		Terminated to V_{CC} - 2.0 V	
	L_LVDS	–	100 Ω		Connected between OUT and $\overline{OUT}$	
Input voltage	V_{IH}	70 % V_{CC} Min.			OE or $\overline{ST}$ terminal	
	V_{IL}	30 % V_{CC} Max.				
Rise/Fall times	tr/tf	0.35 ns Max.			LV-PECL: 20 % - 80 % (V_{OH} - V_{OL}) LVDS: 20 % - 80 % differential output peak to peak	
Start-up time	t_str	10 ms Max.			t = 0 at 90 % V_{CC}	
Phase jitter	t_{PJ}	250 fs Max.	250 fs Max.	400 fs Max.	25 MHz ≤ fo < 100 MHz	Offset frequency fo < 50 MHz: 12 kHz to 5 MHz fo ≥ 50 MHz: 12 kHz to 20 MHz
		90 fs Max.	100 fs Max.	130 fs Max.	100 MHz ≤ fo ≤ 156 MHz	
		70 fs Max.	60 fs Max.	70 fs Max.	156 MHz < fo ≤ 212 MHz	
		60 fs Max.	50 fs Max.	60 fs Max.	212 MHz < fo ≤ 391 MHz	
		50 fs Max.			391 MHz < fo ≤ 500 MHz	

Product Name (Standard form): SG2016 EGN 156.250000MHz C D H P Z A
① ② ③ ④⑤⑥⑦⑧⑨

①Model ②Output (E: LV-PECL, V: LVDS) ③Frequency ④Supply voltage ⑤Frequency tolerance
⑥Operating temperature ⑦Function ⑧Output disable type (Z: High impedance) ⑨Output option

④Supply voltage	
C	3.3 V Typ.
D	2.5 V Typ.
E*	1.8 V Typ.

* "E" is only for SG2016VGN and SG2520VGN

⑤Freq. tolerance	
D	±25 × 10^{-6}
J	±50 × 10^{-6}

⑥Operating temp.	
G	-40 °C to +85 °C
H	-40 °C to +105 °C

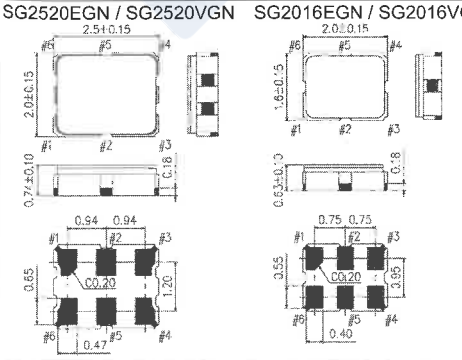
⑦Function	
P	OE
S	$\overline{ST}$

⑨Output option		
	SG2016EGN / SG2520EGN	SG2016VGN / SG2520VGN
A	Default	V_{OD} = 250 mV to 450 mV
B*	–	V_{OD} = 400 mV to 800 mV
C	–	V_{OD} = 300 mV to 600 mV

*Not available for V_{CC} = 1.8 V Typ.

External dimensions (Unit mm)

SG2520EGN / SG2520VGN SG2016EGN / SG2016VGN

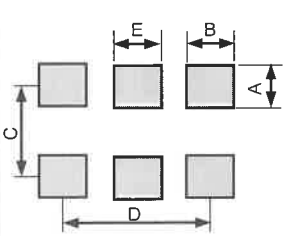


Pin map

Pin	Connection
1	OE or $\overline{ST}$
2	N.C. (Open or V_{CC})
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

Note:
OE or $\overline{ST}$ pin = HIGH or "Open": Specified frequency output.
OE or $\overline{ST}$ pin = LOW: Output is high impedance

Footprint (Recommended) (Unit.mm)



	SG2520EGN SG2520VGN	SG2016EGN SG2016VGN
A	0.88	0.85
B	0.76	0.574
C	1.38	1.15
D	1.99	1.564
E	0.63	0.574

In order to achieve optimum jitter performance, it is recommended that 0.1 µF and 10 µF bypass capacitors should be connected between V_{CC} and GND and placed as close to the V_{CC} pin as possible.

CRYSTAL OSCILLATOR (SPXO)

OUTPUT : LV-PECL, LVDS

Pb Free
RoHS Compliant

Product Number
SG3225EEN: X1G005221xxxx00 (fo ≤ 200 MHz)
X1G005511xxxx00 (fo > 200 MHz)
SG5032EEN: X1G005531xxxx00
SG7050EEN: X1G005131xxxx00 (fo ≤ 200 MHz)
X1G005551xxxx00 (fo > 200 MHz)
SG3225VEN: X1G005351xxxx00 (fo ≤ 200 MHz)
X1G005521xxxx00 (fo > 200 MHz)
SG5032VEN: X1G005541xxxx00
SG7050VEN: X1G005331xxxx00 (fo ≤ 200 MHz)
X1G005561xxxx00 (fo > 200 MHz)

SG3225 / 5032 / 7050EEN
SG3225 / 5032 / 7050VEN

- Frequency range : 25 MHz to 500 MHz
- Supply voltage : 2.5 V Typ. / 3.3 V Typ.
- Output : LV-PECL or LVDS
- Function : Output enable (OE)
- Phase jitter : 50 fs Typ. (fo = 156.25 MHz, LV-PECL)
- Operating temperature : -40 °C to +105 °C


SG3225EEN
SG3225VEN
(3.2 × 2.5 × 1.05 mm)


SG5032EEN
SG5032VEN
(5.0 × 3.2 × 1.3 mm)


SG7050EEN
SG7050VEN
(7.0 × 5.0 × 1.5 mm)

Specifications (characteristics)

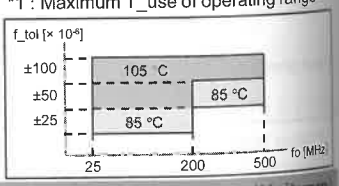
Item	Symbol	Specifications LV-PECL: SG3225EEN / SG5032EEN / SG7050EEN	Specifications LVDS: SG3225VEN / SG5032VEN / SG7050VEN	Conditions / Remarks		
Output frequency range	fo	25 MHz to 500 MHz		Except for SG5032EEN / SG5032VEN	Please contact us for available frequencies.	
		200.1 MHz to 500 MHz		SG5032EEN / SG5032VEN		
Supply voltage	V_{CC}	D: 2.5 V ± 0.125 V, C: 3.3 V ± 0.165 V				
Storage temperature	T_stg	-55 °C to +125 °C				
Operating temperature	T_use	G: -40 °C to +85 °C, H: -40 °C to +105 °C				
Frequency tolerance	f_tol	D: ±25 × 10^{-6} Max.		Includes initial frequency tolerance, temperature variation, supply voltage change and 5 years aging (+25 °C)		Refer to figure *1
		J: ±50 × 10^{-6} Max.		Includes initial frequency tolerance, temperature variation, supply voltage change and 10 years aging (+25 °C)		
		L: ±100 × 10^{-6} Max.				
Current consumption	I_{CC}	60 mA Max.	25 mA Max.	OE = V_{CC}, L_ECL = 50 Ω or L_LVDS = 100 Ω		
Disable current	I_dis	25 mA Max.	15 mA Max.	OE = GND		
Symmetry	SYM	45 % to 55 %		At output crossing point		
Output voltage (LV-PECL)	V_{OH}	V_{CC} - 1.1 V Min.	–	DC characteristics		
	V_{OL}	V_{CC} - 1.5 V Max.	–			
Output voltage (LVDS)	V_{OD}	–	250 mV to 450 mV	Differential output voltage, V_{OD1}, V_{OD2}	DC characteristics	
	dV_{OD}	–	50 mV Max.	dV_{OD} = | V_{OD1} - V_{OD2} |		
	V_{OS}	–	1.15 V to 1.35 V	Offset voltage, V_{OS1}, V_{OS2}		
	dV_{OS}	–	50 mV Max.	dV_{OS} = | V_{OS1} - V_{OS2} |		
Output load condition	L_ECL	50 Ω	–	Terminated to V_{CC} - 2.0 V		
	L_LVDS	–	100 Ω	Connected between OUT to $\overline{OUT}$		
Input voltage	V_{IH}	70 % V_{CC} Min.		OE terminal		
	V_{IL}	30 % V_{CC} Max.				
Rise/Fall times	tr / tf	0.3 ns Max.	0.3 ns Max.	V_{CC} = 3.3 V, 25 MHz ≤ fo ≤ 200 MHz	LV-PECL: Between 20 % and 80 % of (V_{OH} - V_{OL}) LVDS: Between 20 % and 80 % of Differential Output peak to peak voltage	
		0.35 ns Max.		All other		
Startup time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s		

Phase Jitter

Product Name	100 MHz	125 MHz	156.25 MHz	200 MHz	312.5 MHz	491.52 MHz	Conditions
SG3225EEN / SG5032EEN / SG7050EEN	75 fs Typ.	60 fs Typ.	50 fs Typ.	40 fs Typ.	30 fs Typ.	20 fs Typ.	Offset frequency:
SG3225VEN / SG5032VEN / SG7050VEN	90 fs Typ.	70 fs Typ.	60 fs Typ.	50 fs Typ.	40 fs Typ.	30 fs Typ.	12 kHz to 20 MHz

Product Name (Standard form): SG3225 EEN 156.250000MHz C D G A (⑤⑥: Unavailable code DH, DG and JH at fo > 200 MHz, Refer to figure *1)
① ② ③ ④⑤⑥⑦
①Model ②Output (E: LV-PECL, V: LVDS) ③Frequency ④Supply voltage
⑤Frequency tolerance ⑥Operating temperature ⑦Internal identification code("A" is default)

*1 : Maximum T_use of operating range



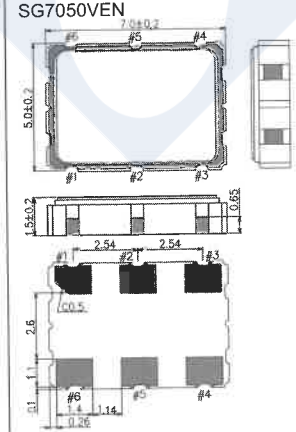
④Supply voltage	
C	3.3 V Typ.
D	2.5 V Typ.

⑤Frequency tolerance	
D	±25 × 10^{-6}
J	±50 × 10^{-6}
L	±100 × 10^{-6}

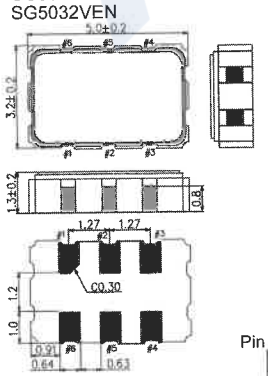
⑥Operating temperature	
G	-40 to +85 °C
H	-40 to +105 °C

External dimensions (Unit:mm)

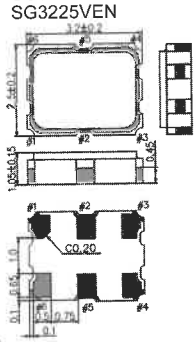
SG7050EEN
SG7050VEN



SG5032EEN
SG5032VEN



SG3225EEN
SG3225VEN

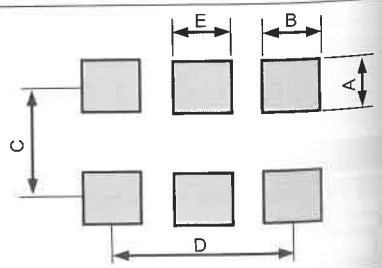


Pin map

Pin	Connection
1	OE
2	N.C. (Open or V_{CC})
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

Note:
OE pin = HIGH or "Open": Specified frequency output.
OE pin = LOW: Output is high impedance

Footprint (Recommended) (Unit:mm)



	SG3225EEN SG3225VEN	SG5032EEN SG5032VEN	SG7050EEN SG7050VEN
A	1.05	1.60	2.00
B	0.92	0.89	1.80
C	1.85	2.60	4.20
D	2.58	2.54	5.08
E	0.80	0.89	1.80

In order to achieve optimum jitter performance, it is recommended that 0.1 µF and 10 µF bypass capacitors should be connected between V_{CC} and GND and placed as close to the V_{CC} pin as possible.

CRYSTAL OSCILLATOR (SPXO)
OUTPUT : LV-PECL, LVDS

SG3225EAN / VAN
SG5032EAN / VAN
SG7050EAN / VAN

- Achieved wide frequency range by PLL technology and Fundamental AT crystal units
- Frequency range : 73.5 MHz to 700 MHz
- Supply voltage : 2.5 V to 3.3 V
- Function : Output enable (OE)
- Output : LV-PECL or LVDS

Product Number
SG3225EAN: X1G004251xxxx00
SG3225VAN: X1G004241xxxx00
SG5032EAN: X1G004271xxxx00
SG5032VAN: X1G004261xxxx00
SG7050EAN: X1G004291xxxx00
SG7050VAN: X1G004281xxxx00


SG3225EAN/VAN
(3.2 × 2.5 × 1.05 mm)


SG5032EAN/VAN
(5.0 × 3.2 × 1.0 mm)


SG7050EAN/VAN
(7.0 × 5.0 × 1.4 mm)

Specifications (characteristics)

Item	Symbol	Specifications LV-PECL: SG3225EAN / SG5032EAN / SG7050EAN	Specifications LVDS: SG3225VAN / SG5032VAN / SG7050VAN	Conditions / Remarks
Output frequency range	f_0	73.5 MHz to 700 MHz		Please contact us about available frequencies.
Supply voltage	V_{CC}	K: 2.5 V - 10 % to 3.3 V + 10 %		
Storage temperature	T_stg	-40 °C to +125 °C		Storage as single product.
Operating temperature	T_use	B: -20 °C to +70 °C, G: -40 °C to +85 °C		
Frequency tolerance	f_tol	J: ± 50 × 10^{-6}, E: ± 30 × 10^{-6}, C: ± 20 × 10^{-6}		
Current consumption	Icc	65 mA Max.	30 mA Max.	OE = Vcc, L_ECL = 50 Ω or L_LVDS = 100 Ω
Disable current	I_dis	20 mA Max.		OE = GND
Symmetry	SYM	45 % to 55 %		At outputs crossing point
Output voltage (LV-PECL)	V_{OH}	Vcc - 1.0 V to Vcc - 0.8 V	–	DC characteristics
	V_{OL}	Vcc - 1.78 V to Vcc - 1.62 V	–	
Output voltage (LVDS)	V_{OD}	–	250 mV to 450 mV	V_{OD1}, V_{OD2} / DC characteristics
	dVOD	–	50 mV Max.	dVOD = | V_{OD1}-V_{OD2} |
	V_{OS}	–	1.15 V to 1.35 V	V_{OS1}, V_{OS2}
	dVOS	–	150 mV Max.	dVOS = | V_{OS1}-V_{OS2} |
Output load condition (ECL) / (LVDS)	L_ECL	50 Ω	–	Terminated to Vcc -2.0 V
	L_LVDS	–	100 Ω	Connected between OUT to $\overline{OUT}$
Input voltage	V_{IH}	70 % Vcc Min.		OE terminal
	V_{IL}	30 % Vcc Max.		
Rise time / Fall time	t_r / t_f	350 ps Max.	300 ps Max.	LV-PECL: Between 20 % and 80 % of (VOH-VOL). LVDS: Between 20 % and 80 %of Differential Output peak to peak voltage
Start-up time	t_str	3 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	t_{PJ}	0.6 ps Max.*1		Offset frequency: 12 kHz to 20 MHz
Frequency aging	f_age	± 5 × 10^{-6} / year Max.		+25 °C, First year, Vcc = 2.5 V, 3.3 V

*1 0.9 ps Max. (f_0 = 243 MHz ~ 250 MHz, 486 MHz ~ 500 MHz)

Product Name (Standard form): SG3225 E AN 156.250000MHz K J G A (⑤⑥: CG is not available)
① ② ③ ④⑤⑥⑦

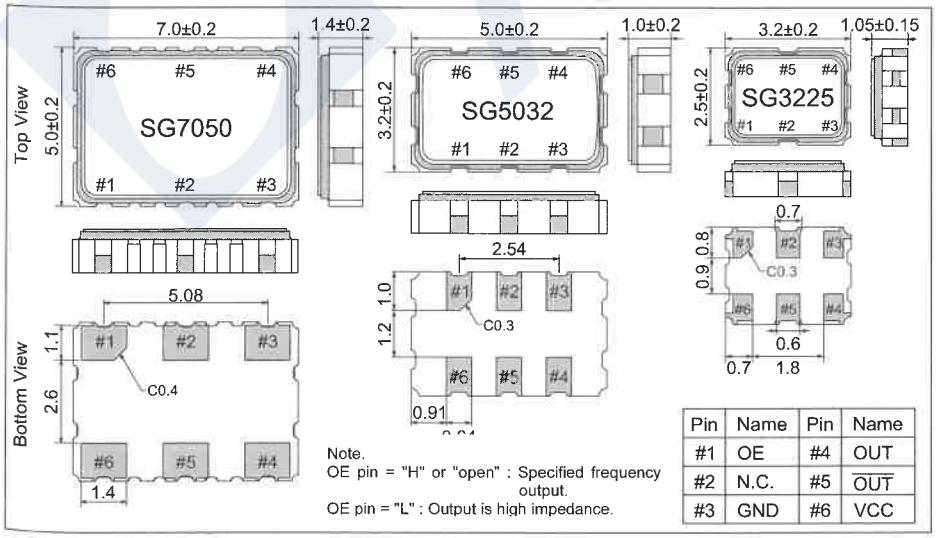
①Model ②Output (E: LV-PECL, V: LVDS) ③Frequency ④Supply voltage ⑤Frequency tolerance
⑥Operating temperature ⑦Internal identification code ("A" is default)

④Supply voltage	
K	2.5 V ~ 3.3 V

⑤Frequency tolerance	
J	±50 × 10^{-6}
E	±30 × 10^{-6}
C	±20 × 10^{-6}

⑥Operating temperature	
B	-20 °C ~ +70 °C
G	-40 °C ~ +85 °C

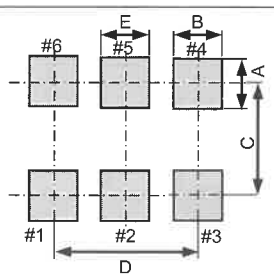
External dimensions (Unit: mm)



Pin	Name	Pin	Name
#1	OE	#4	OUT
#2	N.C.	#5	$\overline{OUT}$
#3	GND	#6	VCC

Note.
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.

Footprint (Recommended) (Unit: mm)



Size

	SG3225 type	SG5032 type	SG7050 type
A	1.05	1.60	2.00
B	0.86	0.89	1.80
C	1.85	2.60	4.20
D	2.58	2.54	5.08
E	0.82	0.89	1.80

To maintain stable operation, provide a 0.01 µF to 0.1 µF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

CRYSTAL OSCILLATOR (SPXO)
OUTPUT : HCSL

Pb Free
RoHS Compliant

Product Number
X1G005141xxxx00

SG3225HBN

- •Frequency range : 100 MHz to 325 MHz
- •Supply voltage : 2.5V, 3.3 V
- •Output : HCSL
- •Function : Output enable (OE)
- •External dimensions : 3.2 × 2.5 × 1.05 mm
- •Phase jitter : 85 fs Typ (fo = 156.25MHz)

Specifications (characteristics)

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	fo	100 MHz to 325 MHz	Please contact us for inquiries regarding available frequencies.
Supply voltage	V_{CC}	D : 2.5 V ± 0.125 V , C : 3.3 V ± 0.165 V	
Storage temperature	T_stg	-55 °C to +125 °C	Store as bare product.
Operating temperature	T_use	G: -40 °C to +85 °C, H: -40 °C to +105 °C	
Frequency tolerance	f_tol	J: ± 50 × 10^{-6} (Not available H : -40 °C to +105 °C)	Includes initial frequency tolerance, temperature variation, supply voltage change and 10 years aging(+25 °C)
		L: ± 100 × 10^{-6}	
Current consumption	I_{CC}	25 mA Typ. 35 mA Max.	OE= V_{CC}, with output load
Disable current	I_dis	15 mA Max.	OE=GND
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V_{OH}	0.75 V Typ., 0.66 V to 0.85 V	DC characteristics, single output
	V_{OL}	0 V Typ., -0.15 V to 0.15 V	
Crossing voltage	V_{CR}	0.25 V to 0.55 V	
Output load condition	L_HCSL	50 Ω	
	R_S	33 Ω	
Input voltage	V_{IH}	70 % V_{CC} Min.	OE terminal
	V_{IL}	30 % V_{CC} Max.	
differential output rise slew rate/ fall slew rate	Rr / Rf	1 V/ns to 4 V/ns	Between -0.15 V and 0.15 V of differential output
Start-up time	t_str	10 ms Max.	Time at minimum supply voltage to be 0 s

Phase Jitter

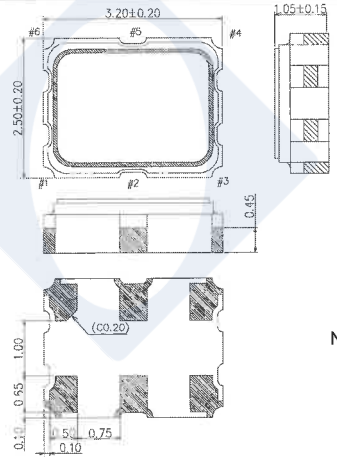
	Output frequency	100 MHz	125 MHz	156.25 MHz	200 MHz	322.265625 MHz	Supply voltage
Phase Jitter [fs] (Offset Frequency 12k to 20MHz)	Typ.	110	95	85	75	65	V_{CC}=3.3V±0.165V
	Max.	180	160	140	125	110	

Product Name (Standard form)

SG3225 HBN 156.250000MHz C J G A (⑤⑥: Not Available code JH)
① ② ③ ④⑤⑥⑦

①Model ②Output (H: HCSL) ③Frequency ④Supply voltage (D: 2.5 V Typ. , C: 3.3 V Typ.)
⑤Frequency tolerance (J: ±50 × 10^{-6} L: ±100 × 10^{-6})
⑥Operating temperature (G:-40 to +85°C, H:-40 to +105°C) ⑦Internal identification code("A" is default)

External dimensions (Unit:mm)

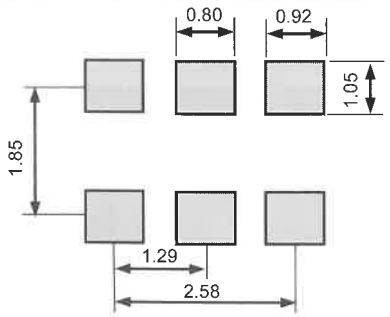


Pin map

Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

Note:
OE pin = HIGH or "Open" : Specified frequency output.
OE pin = LOW : Output is high impedance

Footprint (Recommended) (Unit:mm)



In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 µF + 10 µF) between V_{CC} and GND pin should be placed as close to the V_{CC} pin as possible.

I²C-Bus Programmable Crystal Oscillator (SPXO)

Output: LV-PECL

SG-8506CA

Pb Free
RoHS Compliant

Product Number
X1G005031xxxx00


- Frequency range : 50 MHz to 800 MHz
- Supply voltage : 2.5 V to 3.3 V
- External dimensions : 7.0 × 5.0 × 1.5 mm (8 pins)

Features
- User-specified one startup frequency, 7-bit I²C
- User Programming: I²C Interface
- High frequency fundamental tone crystal, Low jitter PLL technology
- Available field oscillator programmer "SG-Writer II"

Application
- OTN, BTS, Test Instrument

*The I2C-Bus is a trademark of NXP Semiconductors

Specifications (characteristics)

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	fo	50 MHz to 800 MHz	It can be changed by I²C
Supply voltage	V_{CC}	2.5 V - 0.125 V to 3.3 V + 0.33 V	-
Storage temperature	T_stg	-55 °C to +125 °C	Store as bare product after packing
Operating temperature	T_use	-40 °C to +85 °C	-
Frequency tolerance *1	f_tol	K : ±31.5 × 10^{-6}	Customized Product (Option)
		L : ±50 × 10^{-6}	
Current consumption	I_{CC}	90 mA Max.	OE Active, L_ECL=50 Ω
Disable current	I_dis	40 mA Max.	OE Inactive, Output Standby: Hi-Z mode
		70 mA Max.	OE Inactive, Output Standby: Fix mode
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V_{OH}	Vcc - 1.025 V Min.	DC characteristics
	V_{OL}	Vcc - 1.62 V Max.	
Output load condition	L_ECL	50 Ω	Termination to Vcc - 2.0 V
Input voltage	V_{IH}	70% Vcc Min.	OE, SDA and SCL
	V_{IL}	30% Vcc Max.	
Rise time / Fall time	tr / tf	400 ps Max.	Between 20% and 80% of (V_{OH} - V_{OL})
Start-up time	t_str	10 ms Max.	Time at minimum supply voltage to be 0 s
Setting time for frequency change	t_{SET1}	1.5 ms Max.	From setting NEW_FREQ bit to output new frequency

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

Product Name (Standard form): SG-8506 ① CA ② 156.2MHz ③ 0x37 ④ A ⑤ P ⑥ R ⑦ L ⑧ Z ⑨

① Model, ② Package type,
③ Power-on default output frequency (50 ~ 800 MHz), ④ I²C slave address, ⑤ Internal crystal frequency,
⑥ Output enable pin Polarity, ⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

⑤ Internal crystal frequency	
A	114.1444 MHz

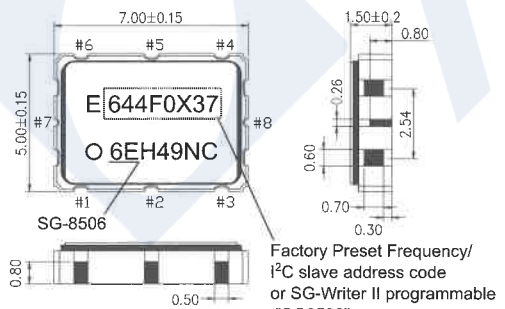
⑥ Output enable pin Polarity	
P	Active High
Q	Active Low

⑦ Supply voltage/ Output format	
R	2.5 V ~ 3.3 V/LVPECL

⑧ Frequency tolerance/ Operating temperature	
K	±31.5 × 10^{-6}/-40 to +85 °C
L	±50 × 10^{-6}/-40 to +85 °C

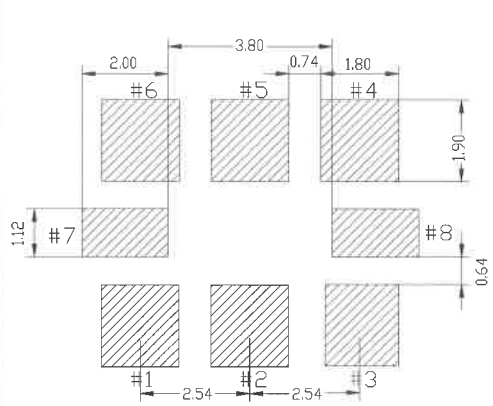
⑨ Output standby type	
F	Fix (OUT="L", OUTN="H")
Z	High-Z

External dimensions (Unit: mm)



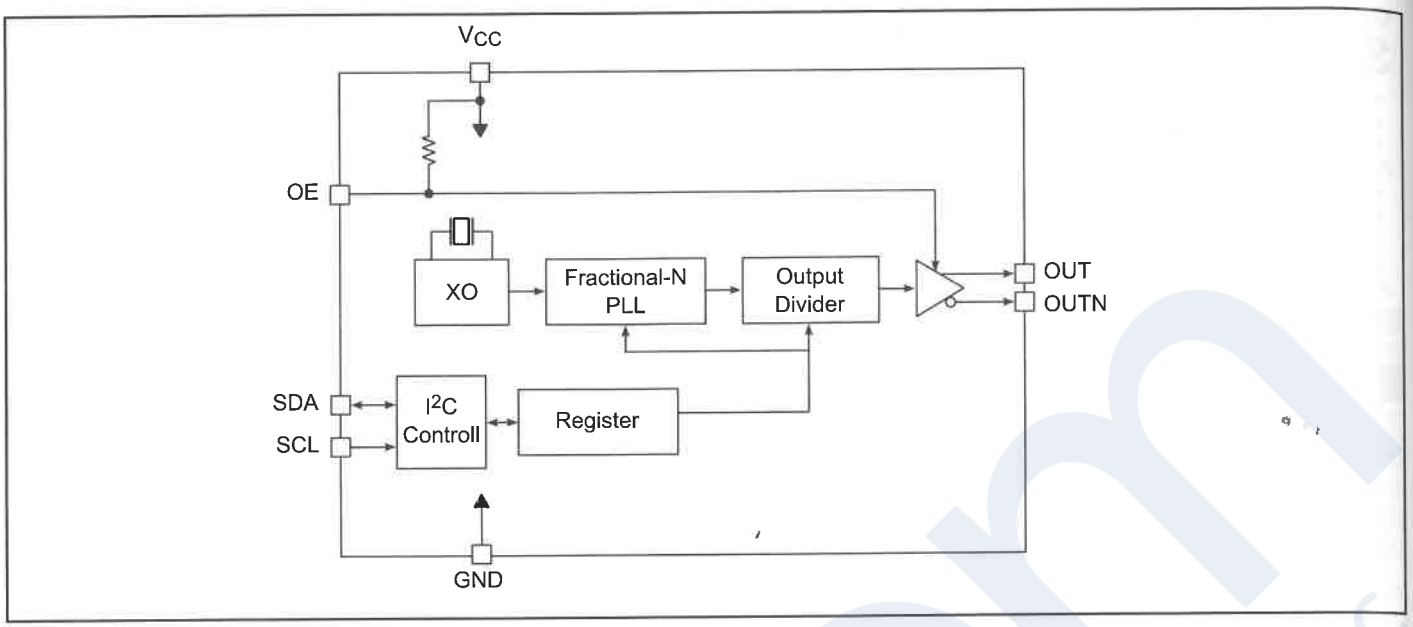
Pin	Connection
1	NC
2	OE
3	GND
4	OUT
5	OUTN
6	Vcc
7	SDA
8	SCL

Footprint (Recommended) (Unit: mm)

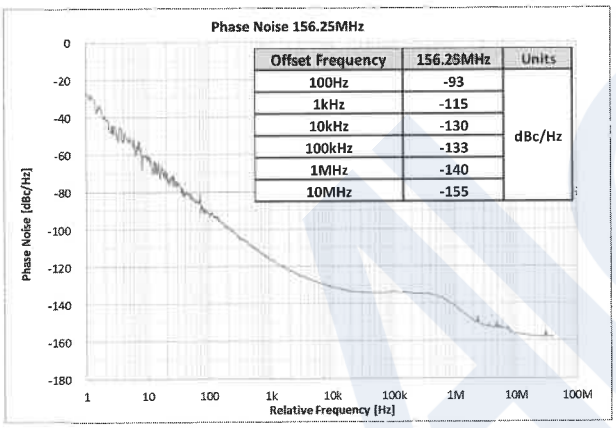


In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 µF + 10 µF) between Vcc and GND pin should be placed as close to the Vcc pin as possible.

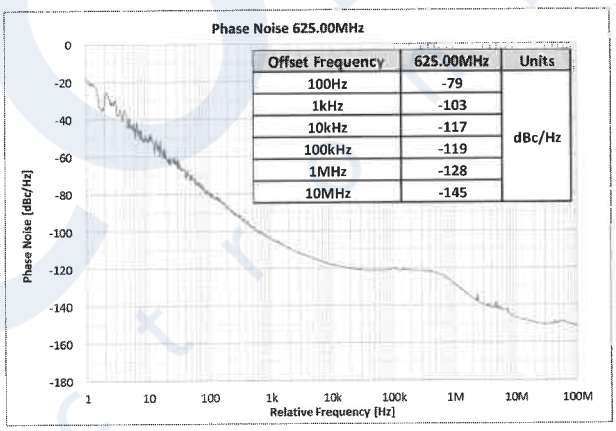
Block diagram



Phase Noise



Offset Frequency	156.25MHz	Units
100Hz	-93	dBc/Hz
1kHz	-115	
10kHz	-130	
100kHz	-133	
1MHz	-140	
10MHz	-155	



Offset Frequency	625.00MHz	Units
100Hz	-79	dBc/Hz
1kHz	-103	
10kHz	-117	
100kHz	-119	
1MHz	-128	
10MHz	-145	

Phase Jitter

	Offset Frequency	100.00 MHz	125.00 MHz	156.25 MHz	250.00 MHz	312.50 MHz	500.00 MHz	625.00 MHz
Phase jitter *2 Typ.	12 kHz to 20 MHz	0.31 ps	0.30 ps	0.26 ps	0.26 ps	0.29 ps	0.28 ps	0.29 ps

*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 µF + 10 µF) between V_{CC} and GND pin should be placed as close to the V_{CC} pin as possible.

Dual or Quad Selectable Programmable Crystal Oscillator
Output: LV-PECL

SG-8503CA / SG-8504CA

Product Number
SG-8503CA : X1G005011xxxx00
SG-8504CA : X1G005021xxxx00


- Dual frequency Selectable: SG-8503CA, 7.0 × 5.0 × 1.5 mm (6 pins)
- Quad frequency Selectable: SG-8504CA, 7.0 × 5.0 × 1.5 mm (8 pins)
- Frequency range: 50 MHz to 800 MHz
- Supply voltage: 2.5 V to 3.3 V

Features
- User-specified two (FSEL) or four (FSEL0, FSEL1) startup frequencies
- High frequency fundamental tone crystal, Low jitter PLL technology
- Available field oscillator programmer "SG-Writer II"

Application
- OTN, BTS, Test Instrument

Specifications (characteristics)

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	fo	50 MHz to 800 MHz	-
Supply voltage	V_{CC}	2.5 V - 0.125 V to 3.3 V + 0.33 V	-
Storage temperature	T_stg	-55 °C to +125 °C	Store as bare product after packing
Operating temperature	T_use	-40 °C to +85 °C	-
Frequency tolerance *1	f_tol	K : ±31.5 × 10^{-6}	Customized Product (Option)
		L : ±50 × 10^{-6}	
Current consumption	I_{CC}	90 mA Max.	OE Active, L_ECL = 50 Ω
Disable current	I_dis	40 mA Max.	OE Inactive, Output Standby: Hi-Z mode
		70 mA Max.	OE Inactive, Output Standby: Fix mode
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V_{OH}	Vcc - 1.025 V Min.	DC characteristics
	V_{OL}	Vcc - 1.62 V Max.	
Output load condition	L_ECL	50 Ω	Termination to Vcc - 2.0 V
Input voltage	V_{IH}	70% Vcc Min.	SG-8503CA : OE, FSEL
	V_{IL}	30% Vcc Max.	SG-8504CA : OE, FSEL0, FSEL1
Rise time / Fall time	tr / tf	400 ps Max.	Between 20% and 80% of (V_{OH} - V_{OL})
Start-up time	t_str	10 ms Max.	Time at minimum supply voltage to be 0 s
Setting time for frequency change	t_{SET1}	1.5 ms Max.	SG-8503CA : From setting FSEL pin to output new frequency SG-8504CA : From setting FSEL0 / FSEL1 pin to output new frequency

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

Product Name (Standard form) SG-8503 CA 156MHz 625MHz A P R L Z
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨
① Model, ② Package type,
③ Frequeny-0 (50 ~ 800 MHz), ④ Frequency-1 (50 ~ 800 MHz), ⑤ Internal crystal frequency, ⑥ Output enable pin Polarity,
⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

Product Name (Standard form) SG-8504 CA 156.2MHz nnnn A P R L Z
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨
① Model, ② Package type,
③ Frequeny-0 (50 ~ 800 MHz), ④ Parameter identifier, ⑤ Internal crystal frequency, ⑥ Output enable pin Polarity,
⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

⑤ Internal crystal frequency	
A	114.1444 MHz

⑥ Output enable pin Polarity	
P	Active High
Q	Active Low

⑦ Supply voltage/ Output format	
R	2.5 V ~ 3.3 V/LVPECL

⑧ Frequency tolerance/ Operating temperature	
K	±31.5 × 10^{-6}/-40 to +85 °C
L	±50 × 10^{-6}/-40 to +85 °C

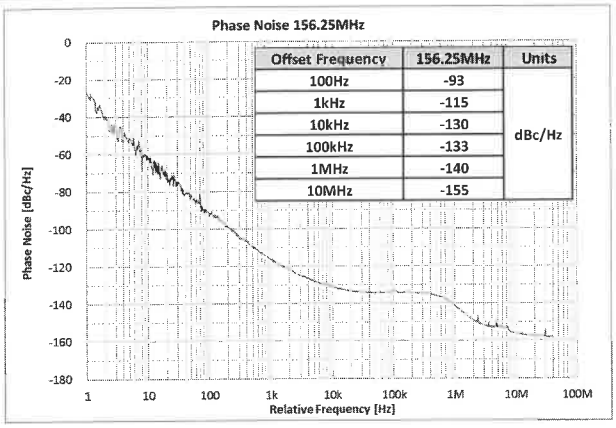
⑨ Output standby type	
F	Fix (OUT="L", OUTN="H")
Z	High-Z

Phase Jitter

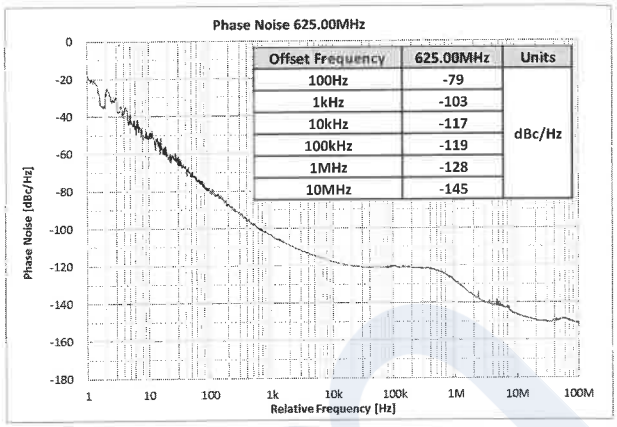
	Offset Frequency	100.00 MHz	125.00 MHz	156.25 MHz	250.00 MHz	312.50 MHz	500.00 MHz	625.00 MHz
Phase jitter *2 Typ.	12 kHz to 20 MHz	0.31 ps	0.30 ps	0.26 ps	0.26 ps	0.29 ps	0.28 ps	0.29 ps

*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 µF + 10 µF) between Vcc and GND pin should be placed as close to the Vcc pin as possible.

Phase Noise



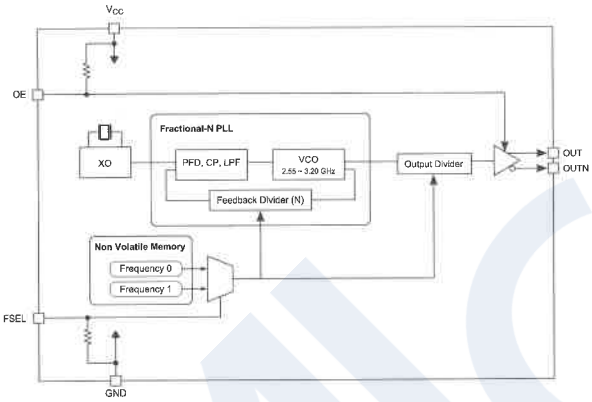
Offset Frequency	156.25MHz	Units
100Hz	-93	dBc/Hz
1kHz	-115	
10kHz	-130	
100kHz	-133	
1MHz	-140	
10MHz	-155	



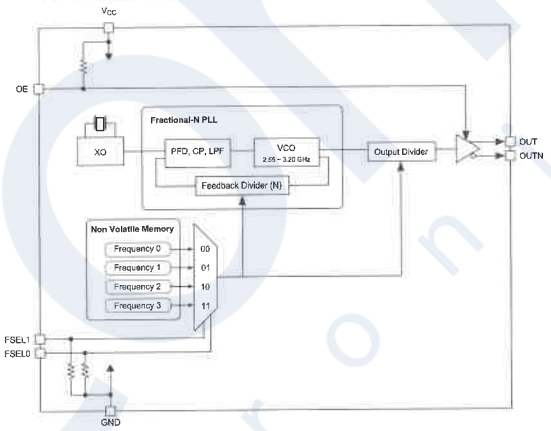
Offset Frequency	625.00MHz	Units
100Hz	-79	dBc/Hz
1kHz	-103	
10kHz	-117	
100kHz	-119	
1MHz	-128	
10MHz	-145	

Block diagram

SG-8503CA

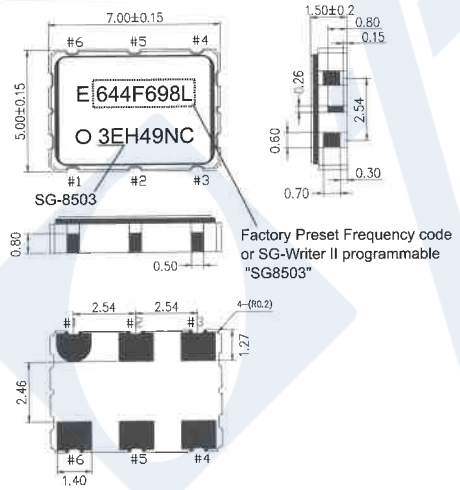


SG-8504CA



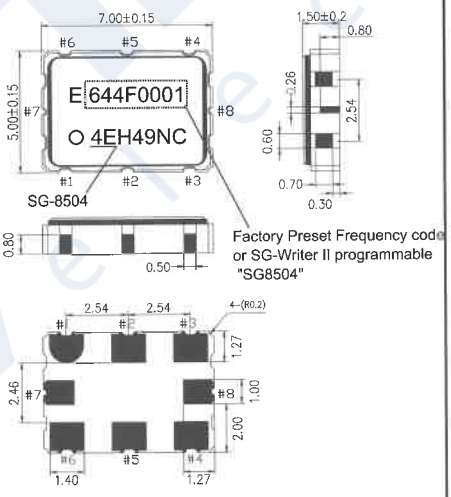
External dimensions (Unit: mm)

SG-8503CA



Pin	Connection
1	OE
2	FSEL (L = Frequency-0, H = Frequency-1)
3	GND
4	OUT
5	OUTN
6	Vcc

SG-8504CA

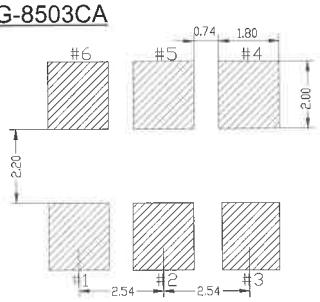


Pin	Connection	Pin	Connection
1	NC	5	OUTN
2	OE	6	Vcc
3	GND	7	FSEL0
4	OUT	8	FSEL1

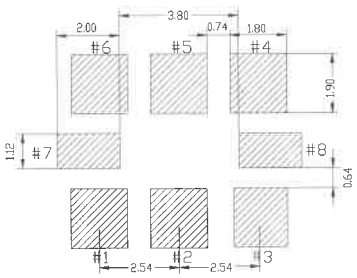
FSEL1, FSEL0	Output Frequency
LL	Frequency-0
LH	Frequency-1
HL	Frequency-2
HH	Frequency-3

Footprint (Recommended)(Unit: mm)

SG-8503CA



SG-8504CA



In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 µF + 10 µF) between Vcc and GND pin should be placed as close to the Vcc pin as possible.